THE COMPLETE LINEAR BOOK

	PAGES
Introduction and Product Index	iii–v
Selection Guides	vi–x
Competitive Cross Reference	xi–xvi
Data Sheets	1–393
Application Reports and Briefs	394–641
Most Recent Linear Circuits and Data Briegs	642–673
Planned Linear Products	675–684
Dice	685
Hi Rel Unique 38510	686
Ordering Information	688
Glossary	693

Application Reports and Briefs

	PAGE
APPLICATIONS BRIEF 44, GATED PULSE RATE FUNCTION MULTIPLIER	394
APPLICATIONS BRIEF 50, MULTI-SIGNAL PROCESSING CIRCUIT	396
APPLICATIONS BRIEF 51, ANALOG TO PULSE WIDTH CONVERTOR	399
APPLICATIONS BRIEF 54, FOUR QUADRANT ANALOG MULTIPLIER	402
APPLICATIONS BRIEF 66, FM STEREO MULTIPLEX DECODER	406
APPLICATIONS BRIEF 85, SOME USEFUL SIGNAL PROCESSING CIRCUITS USING FET's AND OPERATIONAL AMPLIFIERS	410
AN ECONOMICAL D/A OR STAIRCASE GENERATOR USING THE μA739	423
μA733 OSCILLATORS	428
THE μA715, A VERSATILE HIGH SPEED OPERATIONAL AMPLIFIER	430
A MICROPOWER MONOLITHIC OPERATIONAL AMPLIFIER	436
THE μA746E COLOUR TV CHROMA DEMODULATOR IC	440
APPLICATIONS OF THE μA749 DUAL OPERATIONAL AMPLIFIER	445
THE μA749 DUAL OPERATIONAL AMPLIFIER	448
A TRAPEZOIDAL DEFLECTION CIRCUIT FOR USE WITH THE 3250 NUMERIC CHARACTER GENERATOR USING THE μA715	460
A HIGH SPEED SAMPLE AND HOLD USING THE μA715	462
LOW-PASS ACTIVE FILTER FOR ELECTRONIC IMAGING USING THE μA715	464
μA725 AGC AMPLIFIER	467
AN ARITHMETIC ANALOG COMPUTER USING μA735 LOGARITHMIC AMPLIFIERS	470
ACTIVE FILTERS WITH GAIN USING THE μA725	474
MORE VOLTAGE REGULATOR APPLICATIONS USING THE μA723	477
THE FREQUENCY DIVISION MULTIPLEX CHANNEL AMPLIFIER WITH THE μA748	481
PERFORMANCE OF THE μA703 IN 100-MHz AND 200-MHz AMPLIFIERS AND 100-MHz HARMONIC MIXERS	484
A LOW-DRIFT, LOW-NOISE MONOLITHIC OPERATIONAL AMPLIFIER FOR LOW LEVEL SIGNAL PROCESSING	489
μA725 INSTRUMENTATION APPLICATIONS	500
A MINIMUM COMPONENT μA749 VOLTAGE-TO-FREQUENCY CONVERTER WITH 1% ACCURACY	504
COLOUR TELEVISION CHROMA REFERENCE SYSTEMS USING THE μA703	507
VOLTAGE REGULATOR APPLICATIONS USING μA723 – NUMBER 2	511
CHARACTERIZATION AND APPLICATION OF THE μA703 IN A FOUR-STAGE FM-IF AMPLIFIER	513
APPLICATIONS OF THE μA757 GAIN CONTROLLED AMPLIFIER	519
THE μA729, μA732 AND μA767 INTEGRATED CIRCUIT STEREO MULTIPLEX DECODERS	522
HIGH-PERFORMANCE FM-IF AMPLIFIERS USING μA703	539
A NEW APPROACH TO LOW DRIFT AMPLIFIERS	544
DESIGNING WITH THE μA703 MONOLITHIC RF-IF AMPLIFIER	552
APPLICATION OF THE μA722 10-BIT CURRENT SOURCE	562
AN IMPROVED SAMPLE-AND-HOLD CIRCUIT USING THE μA740	588
APPLICATIONS OF THE μA777	594
THE POWER AMPLIFIER USING THE μA777	598
APPLICATIONS OF THE μA785 TV SIGNAL PROCESSING INTEGRATED CIRCUITS	601
APPLICATIONS OF THE μA739 AND μA749 DUAL PREAMPLIFIER INTEGRATED CIRCUITS IN HOME ENTERTAINMENT EQUIPMENT	609
THE μA739, A LOW-NOISE DUAL OPERATIONAL AMPLIFIER	616
A MARKER BEACON AND INDICATOR USING INTEGRATED CIRCUITS	624
THE μA795, A LOW-COST MONOLITHIC MULTIPLIER	630
THE μA776, AN OPERATIONAL AMPLIFIER WITH PROGRAMMABLE GAIN, BANDWIDTH, SLEW-RATE, AND POWER DISSIPATION	637

Introduction

This data catalog contains complete information on Fairchild's entire line of quality linear integrated circuits . . . the most comprehensive line in the industry. Some idea of just how comprehenisve our product line is can be gained quickly by referring to the chart below, which summarizes by market and by major end-equipments within each market, the types of Fairchild devices that serve their needs. There are currently 84 device types in production.

You'll find that the catalog is organized to permit quick, convenient reference to such information as specification data, connection diagrams, block diagrams and ordering information.

Also included are the following special sections devoted to:

- Selection guides to consumer products, interface elements, operational amplifiers and voltage comparators.
- A comprehensive industry-wide cross reference listing direct replacement and equivalent Fairchild products.
- Fairchild's UNIQUE 38510 high reliability program, showing process summary product screening levels and device types currently available.
- A statement on dice, summarizing electrical performance specifications, visual inspection criteria and availability.
- A planned new products listing, illustrating Fairchild's continued technological advancement in proprietary and second source devices.

PRODUCT/MARKET RELATIONSHIP

Product Classifications	COMPUTER		CONSUMER				MILITARY		INDUSTRIAL					
	Mainframe	Peripheral	Transportation	Home Entertainment	Musical Instruments	Appliance	Vehicles/Ordnance	Communications Equipment	Office Machines	Control & Processing	Test & Measuring	Communications	Medical & Scientific	
General Purpose Op Amps		▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	
Precision Op Amps							▲		▲	▲	▲	▲	▲	
Multiple Op Amps		▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	
Comparators			▲		▲			▲		▲	▲	▲	▲	
Drivers/Receivers	▲	▲					▲	▲		▲	▲	▲	▲	
TV Circuits				▲	▲			▲		▲			▲	
Voltage Regulators	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	
Sense Amps	▲	▲					▲	▲	▲	▲				
Low Level Amps								▲				▲		
RF/IF Amps				▲				▲				▲		
AC Power Control				▲		▲			▲	▲				
Ordnance							▲							

Product Index by Device Type

DEVICE	PAGE
µA101	1
µA101A	3
µ109	11
µA201	15
µA201A	3
µA209	11
µA301A	3
µA309	11
µA702	17
µA703	32
µA706 (TBA641)	675
µA709	42
µA710	54
µA711	65
µA715	71
µA716	79
µA719	83
µA722	95
µA723	103
µA725	115
µA726	133
µA727	137
µA729	143
µA730	147
µA732	155
µA733	159
µA734	171
µA735	179
µA739	185
µA740	189
µA741	193
µA742	205
µA744	209
µA745	211
µA746 NTSC	213
µA747	217
µA748	229
µA749	241
µA750	684
µA751	253
µA754	257
µA757	261
µA760	265
µA761	271
µA767	279
µA776	283
µA777	293
µA780	301
µA781	307

DEVICE	PAGE
µA782	677
µA784 (TAA640)	312
µA785 (TBA550)	316
µA786 (TAA630)	320
µA791	675
µA795	324
µA796	328
µA3018	649
µA3019	649
µA3026	336
µA3036	649
µA3039	649
µA3045	338
µA3046	649
µA3054	336
µA3064	340
µA3065	344
µA3086	649
µA7524	348
µA7525	352
µA7800 Series	642–648
µA9614	356
µA9615	360
µA9616	680
µA9617	680
µA9620	364
µA9621	370
µA9622	376
µA9624	380
µA9625	380
µA9644	390
µA9650	683
CA3018	649
CA3018A	649
CA3019	649
CA3026	649
CA3036	649
CA3039	649
CA3045	649
CA3046	649
CA3054	649
CA3066	678
CA3067	678
CA3068	679
CA3075	676
CA3076	676
CA3086	649

DEVICE	PAGE
LM108/108A	684
SN55/75107	681
SN55/75108	681
SN55/75109	681
SN55/75110	681
SN55/75325	682
SN55/75450	665
SN55/75451	682
TBA550 (formerly μA785)	670
TBA641B	675
ULN2131	677

	PAGES
Application Reports and Briefs	**394–641**
Most Recent Linear Circuits	**642–673**
Planned Linear Products	**675–684**
Dice	**685**
Hi Rel Unique 38510	**686**
Ordering Information	**688**
Glossary	**693**

Selection Guides

Consumer Products
Line Drivers/Receivers
Operational Amplifiers
Voltage Comparators

SELECTION GUIDE FOR CONSUMER TV CIRCUITS

CHROMA PROCESSING AND DEMODULATION

PARAMETER	μA780/781/746	μA3066/3067	μA782
ACC Figure of Merit	$\Delta V_{out} = -3$ dB for $\Delta V_{in} = -20$ dB	$\Delta V_{out} = 3$ dB for $\Delta V_{in} = -20$ dB	$\Delta V_{out} = 3$ dB for $\Delta V_{in} = -20$ dB
Chroma Input Resistance	2.4 kΩ	50 kΩ	1.8 kΩ
Demodulator Output Resistance	300 Ω	5 Ω	50 Ω
Max B-Y Output	10 volts	3.6 volts	7 volts
Chroma Input for Max Demodulator Output	200 mV	200 mV	20 mV
Number of External Components	77	62	42
Number of Alignment Adjustments	4	7	5

SOUND IF AND DETECTOR*

PARAMETER	μA754	TAA640**	CA3065**
Sensitivity (μV)	70	100	200
AMR (dB) at 30% AM	50	44	50
Audio Output (Volts) RMS	3.0	1.6	2.5
IF Voltage Gain (dB)	72	76	68
Detector–Recovered Audio Voltage at Detector Out (mV)	450	–	750

*Typical measurements made at 4.5 MHz for the μA754/CA3065 and 5.5 MHz for the TAA640 (formerly μA784)
**Includes DC Volume Control

SELECTION GUIDE FOR LINE DRIVERS/INTERFACE DRIVERS

Key Features		μA9614	μA9616 (1)	μA9621	μA9624 (2)	μA9644 (3, 4)	75450 (3,5)
Supply Voltages		+5.0	+12 −12	+5.0 +12	+5.0 0 to −30	+5.0	+5.0
V_{IH} (V)	51	1.7		2.0	1.9	2.1	
	59	1.8	2.0	2.0	1.9	2.1	
V_{IL} (V)	51	0.9		1.0	1.1	1.0	
	59	0.85	0.8	1.0	1.1	0.85	
V_{OH} (V)		+3.2	+6.0	+4.3	−0.5	30 Max	30 Max
V_{OL} (V)		+0.2	−6.0	+0.2	+0.2	0.8 1.25	0.4
I_O (on) (mA)						500	250
I_O (off) (μA)						100	100
I_{SC} (mA)		−90	+15 −15	300	−20		
P_D (mW)		175	250	120	40	120	30
t_{pd} (ns)		16	300	10	120	50	

NOTES FOR LINE DRIVERS/INTERFACE DRIVERS

1. The μA9616 is a triple EIA line driver. Each driver incorporates an internal response control circuit. The slew rate is a maximum of 30 V/μs and a minimum of 4 V/μs (3% of unit interval at 20 k band). The two values for I_{SC} are the typical V_{OH} and V_{OL} short circuit currents. The t_{pd} is measured from 1.5 V on the input to the output passing through the 0 V point. The delay is caused by the internally controlled slew rate of the output. The μA9616 meets the electrical interface requirements of EIA-RS-232-C and the CCITT recommendation V.24. By using an external capacitor from the output to ground for wave shaping, the μA9616 will also meet the low level digital interface for MIL STD 188C.
2. The μA9624 is designed to operate with a V_{DD} from 0 to −30 V.
3. The V_{OH} value is a maximum stand off voltage on the collector of the output device. I_O (on) is the maximum steady state current sinking capability of the output device. I_O (off) is the maximum leakage current into the output with the output device off.
4. V_{OL} is the typical V_{CE} (sat) of the output device at collector currents of 100 mA (V_{OL} = 0.8 V) and 500 mA (V_{OL} = 1.25 V).
5. V_{OL} is a typical V_{CE} (sat) of the output transistor at collector currents of 100 mA (V_{OL} = 0.25 V) and 300 mA (V_{OL} = 0.5 V).

SELECTION GUIDE FOR LINE RECEIVERS/INTERFACE RECEIVERS

Key Features		μA9615 (1)	μA9617 (1, 2)	μA9620 (1, 3)	μA9622 (1)	μA9625 (1, 4)
Supply Voltages		+5.0	+5.0	+5.0 +12	+5.0 −10	+5.0 −11 to −30
V_{OL} (V)	51	0.40		0.40	0.40	0.40
	59	0.45	0.40	0.45	0.45	0.50
V_{OH} (V)	51	2.4		3.0	3.0	2.6
	59	2.4	2.4	3.0	3.0	2.6
V_{TH} (V)		±0.5	+1.5	±0.5	±2.0	−3.0 −9.0
VCM (V)		±15	±25	±15	±10	
R_{IN} (kΩ)		7	4	2.4	5	22
P_{DISS} (mW)		175	100	110	140	60
t_{pd} (ns)		28	50	30	35	70
Diff. Inputs		X		X	X	
Output Enable		X			X	
Response Control		X	X	X		
Line Terminator		X	X		X	
Wired−OR Output		X	X	X	X	
Failsafe Control			X		X	

NOTES FOR LINE RECEIVERS/INTERFACE RECEIVERS

1. V_{OL} is the worst-case, guaranteed maximum output low voltage at 25°C. V_{OH} is the worst-case, guaranteed minimum output high voltage at 25°C. Upper listed voltages are for 51 grade (temperature range −55°C to +125°C) devices, while lower voltages are for 59 grade (0°C to 70°C) devices.
2. The μA9617 receiver has a V_{TH} of 1.0 when the hysteresis pin is left open. If the response control pin is shorted to the hysteresis pin, the μA9617 receiver will operate with a typical 1.3 volts of hysteresis (i.e. V_{IH} = 20 V, V_{IL} = 0.7 V). With or without hysteresis, the receiver in the μA9617 operates in a failsafe mode as described in section 2.5 of EIA RS-232-C. The inputs are protected to ±25 volts (reference to ground). The μA9617 also meets the CCITT recommendation V.24.
3. The μA9620 provides two sets of differential inputs to each receiver: a 5 to 1 attenuated input (normally used) and a direct input. The V_{TH} and V_{CM} shown refer to the attenuated inputs. Divide the values by a factor of five to find values for the direct inputs. The response control on the μA9620 may be achieved by using two capacitors for each receiver; one from each direct input to ground. The attenuator inputs are connected to the line.
4. The μA9625 is not a line receiver; it is a dual MOS to TTL logic level converter. The negative 3.0 V V_{TH} is the guaranteed worst case V_{IH} necessary to produce a V_{OH}. The supply voltage range of −11 to −30 V is the min and max V_{DD} voltages allowable.

SELECTION GUIDE FOR COMMERCIAL GRADE OPERATIONAL AMPLIFIERS*

Key Features	μA702[x] Wide Band General Purpose	μA709 General Purpose	μA715 High Slew Rate Wide Band	μA725 High Accuracy Low Drift Excellent Stability	μA739 Low Noise Dual	μA740 High Z_{in} $10^{12}\Omega$ High Slew Rate	μA741 Internally Compensated General Purpose	μA747 Dual
Input Offset Voltage Max. (mV)	5.0	7.5	7.5	2.5	6.0	100	6.0	6.0
Input Offset Current Max. (nA)	2000	500	250	35	1000		200	200
Input Bias Current Max. (nA)	7500	1500	1500	125	2000	2.0	500	500
Minimum Voltage Gain (V/mV)	3.4	15	10	250	6.5	25	20	20
Operating Supply Voltage Range Min. (V)	+6, −3	±9.0	±6.0	±3.0	±4.0	±5.0	±5.0	±5.0
Max. (V)	+14,−7	±18	±18	±22	±18	±22	±18	±18
Unity Gain Bandwidth (MHz)	30	5.0	65	2.0	10	3.0	1.0	1.0
Slew Rate A_{CL} = 1 (V/μs)	3.5	0.3	18		1.0	6.0	0.5	0.5
A_{CL} = −1 (V/μs)	3.5	0.3	100		2.5	6.0	0.5	0.5
A_{CL} = 10 (V/μs)	5.0	3.0	38		8.0	6.0	0.5	0.5
Input Voltage Range (V)	+1.5, −6.0	±10	±15	±22	±15	±15	±15	±15
Differential Input Voltage (V)	±5.0	±5.0	±15	±22	±5.0	±30	±30	±30
Temp. Coefficient of Input Offset Voltage† (μV/°C)	10	10	6.0	0.5	4.0	20	7.0	7.0
Internal Compensation						x	x	x
Offset Adjust		x	x	x	x	x	x	x
Input Protection			x	x	x	x	x	x
Output Protection				x	x	x	x	x

SELECTION GUIDE FOR COMMERCIAL GRADE OPERATIONAL AMPLIFIERS*(Continued)

Key Features	μA748 Extended Bandwidth General Purpose	μA749 Dual Low Cost	μA776 Programmable I_{SET} = 1.5 μA	μA776 Programmable I_{SET} = 15 μA	μA777 Precision	LM201 Extended Bandwidth General Purpose	LM301A Precision
Input Offset Voltage Max. (mV)	6.0	6.0	6.0	6.0	7.5	7.5	7.5
Input Offset Current Max. (nA)	200	500	6.0	25	50	200	50
Input Bias Current Max. (nA)	500	1000	10	50	250	500	250
Minimum Voltage Gain (V/mV)	20	15	50	50	25	20	25
Operating Supply Voltage Range Min. (V)	±5.0	±4.0	±1.2	±1.2	±5.0	±5.0	±5.0
Max. (V)	±18	±18	±18	±18	±20	±20	±20
Unity Gain Bandwidth (MHz)	1.0	10	0.2	1.0	1.0	1.0	1.0
Slew Rate A_{CL} = 1 (V/μs)	0.5	1.5	0.1	0.7	0.5	0.5	0.5
A_{CL} = −1 (V/μs)	6.0	2.5	0.1	0.7	6.0	6.0	6.0
A_{CL} = 10 (V/μs)	2.0	8.0	0.1	0.7	2.0	2.0	2.0
Input Voltage Range (V)	±15	±15	±15	±15	±15	±15	±15
Differential Input Voltage (V)	±30	±5.0	±30	±30	±30	±30	±30
Temp. Coefficient of Input Offset Voltage† (μV/°C)	7.0	3.0	3.0	3.0	3.0	7.0	6.0
Internal Compensation			x	x			
Offset Adjust	x	x	x	x	x	x	x
Input Protection	x	x	x	x	x	x	x
Output Protection	x	x	x	x	x	x	x

* V_S = ±15 V, T_A = 25°C unless otherwise specified † Typical value, 0°C ≤ T_A ≤ 70°C x V_S = +12, −6 V

SELECTION GUIDE FOR MILITARY GRADE OPERATIONAL AMPLIFIERS*

Key Features	μA702× Wide Band General Purpose	μA709 (312) General Purpose	μA709A (311) General Purpose	μA715 High Slew Rate Wide Band	μA725 High Accuracy Low Drift Excellent Stability	μA740 High Z_{in} 10^{12} Ω High Slew Rate	μA741 Internally Compensated General Purpose	μA747 Dual
Input Offset Voltage Max. (mV)	2.0	5.0	2.0	5.0	1.0	20	5.0	5.0
Input Offset Current Max. (nA)	500	200	50	250	20		200	200
Input Bias Current Max. (nA)	5000	500	200	750	100	0.2	500	500
Minimum Voltage Gain (V/mV)	3.6	25	25	15	1000	50	50	50
Operating Supply Voltage Range Min. (V)	+6, −3	±9.0	±9.0	±6.0	±3.0	±5.0	±5.0	±5.0
Max. (V)	+14, −7	±18	±18	±18	±22	±22	±22	±22
Unity Gain Bandwidth (MHz)	30	5.0	5.0	65	2.0	3.0	1.0	1.0
Slew Rate A_{CL} = 1 (V/μs)	3.5	0.3	0.3	18		6.0	0.5	0.5
A_{CL} = −1 (V/μs)	3.5	0.3	0.3	100		6.0	0.5	0.5
A_{CL} = 10 (V/μs)	5.0	3.0	3.0	38		6.0	0.5	0.5
Input Voltage Range (V)	+1.5, −6.0	±10	±10	±15	±22	±15	±15	±15
Differential Input Voltage (V)	±5.0	±5.0	±5.0	±15	±22	±30	±30	±30
Temp. Coefficient of Input Offset Voltage† (μV/°C)	10	10	1.8	6.0	0.5	20	7.0	7.0
Internal Compensation						x	x	x
Offset Adjust		x	x	x	x	x	x	x
Input Protection				x	x	x	x	x
Output Protection					x	x	x	x

SELECTION GUIDE FOR MILITARY GRADE OPERATIONAL AMPLIFIERS*(Continued)

Key Features	μA748 Extended Bandwidth General Purpose	μA749 Dual Low Cost	μA776 Programmable		μA777 Precision	LM101 Extended Bandwidth General Purpose	LM101A Precision
			I_{SET} = 1.5 μA	I_{SET} = 15 μA			
Input Offset Voltage Max. (mV)	5.0	3.0	5.0	5.0	2.0	5.0	2.0
Input Offset Current Max. (nA)	200	400	3.0	15	10	200	10
Input Bias Current Max. (nA)	500	750	7.5	50	75	500	75
Minimum Voltage Gain (V/mV)	50	25	50	50	50	50	50
Operating Supply Voltage Range Min. (V)	±5.0	±4.0	±1.2	±1.2	±5.0	±5.0	±5.0
Max. (V)	±22	±18	±18	±18	±20	±20	±20
Unity Gain Bandwidth (MHz)	1.0	10	0.2	1.0	1.0	1.0	1.0
Slew Rate A_{CL} = 1 (V/μs)	0.5	1.5	0.1	0.7	0.5	0.5	0.5
A_{CL} = −1 (V/μs)	6.0	2.5	0.1	0.7	6.0	6.0	6.0
A_{CL} = 10 (V/μs)	2.0	8.0	0.1	0.7	2.0	2.0	2.0
Input Voltage Range (V)	±15	±15	±15	±15	±15	±15	±15
Differential Input Voltage (V)	±30	±5.0	±30	±30	±30	±30	±30
Temp. Coefficient of Input Offset Voltage† (μV/°C)	7.0	3.0	3.0	3.0	3.0	3.0	3.0
Internal Compensation			x	x			
Offset Adjust	x	x	x	x	x	x	x
Input Protection	x	x	x	x	x	x	x
Output Protection	x	x	x	x	x	x	x

*V_S = ±15 V, T_A = 25°C unless otherwise specified
† Typical value, −55°C ≤ T_A ≤ 125°C
× V_S = +12, −6 V

SELECTION GUIDE FOR COMMERCIAL GRADE VOLTAGE COMPARATORS [1]

PARAMETER	μA710	μA711	μA734	μA760
Input Offset Voltage, Max. (mV) (2)	5.0	5.0	7.5	6.0
Temperature Coefficient of Input Offset Voltage (μV/°C)	5.0	5.0	3.5	3.0
Input Bias Current, Max. (μA)	40	150	0.15	60
Input Offset Current, Max. (μA)	7.5	25	0.045	7.5
Supply Voltage (V)	+12, −6.0	+12, −6.0	±5.0 to ±15	±4.5 to ±6.5
Response Time (ns)	40	40	200	16
Input Voltage Range (V)	±5.0 (3)	±5.0 (3)	±5.0	±4.0
Output Voltage Swing (V)	−0.5 to −3.2	−0.5 to +3.2	0 to +8.0	0 to ±3.0
Voltage Gain, Min. (V/mV)	0.8	0.5	25	5.0 (4)
Power Consumption, Max. (mW)	150	230 (5)	145	325
TTL Fanout	1	1	2	2
Diff. Input Voltage Range (V)	±5.0	±5.0	±10	±5.0

(1) Typical values at 25° C unless otherwise specified.
(2) Minimum and maximum values are for $0°C \leq T_A \leq 70°C$.
(3) $V^- = -7.0$ V.
(4) Typical.
(5) $T_A = +25°C$.

SELECTION GUIDE FOR MILITARY GRADE VOLTAGE COMPARATORS [1]

PARAMETER	μA710	μA711	μA734	μA760
Input Offset Voltage, Max. (mV) (2)	3.0	4.5	4.0	6.0
Temperature Coefficient of Input Offset Voltage (μV/°C)	3.5	5.0	2.5	3.0
Input Bias Current, Max, (μA)	45	150	0.15	60
Input Offset Current, Max. (μA)	7.0	20	0.02	7.5
Supply Voltage (V)	+12, −6.0	+12, −6.0	±5.0 to ±15	±4.5 to ±6.5
Response Time (ns)	40	40	200	16
Input Voltage Range (V)	±5.0 (3)	±5.0 (3)	±10	±4.0
Output Voltage Swing (V)	−0.5 to +3.2	−0.5 to +3.2	0 to +8.0	0 to +3.0
Voltage Gain, Min. (V/mV)	1.0	0.5	25	5.0 (4)
Power Consumption, Max (mW)	150	200 (5)	145	312
TTL Fanout	1	1	2	2
Diff. Input Voltage Range (V)	±5.0	±5.0	±10	±5.0

(1) Typical values at 20° C unless otherwise specified.
(2) Maximum and minimum values are for $-55°C \leq T_A \leq +125°C$.
(3) $V^- = -7.0$ V.
(4) Typical.
(5) $T_A = +25°C$.

Competitive Cross-Reference

MOTOROLA	FAIRCHILD FUNCTIONAL EQUIVALENT
MC1303L	U6A7739393
MC1304P	
MC1304PQ	
MC1305P	
MC1305PQ	
MC1307P	
MC1307PQ	
MC1326PQ	U7F7746394
MC1326P	U6A7746394
MC1328G	
MC1328P	
MC1328PQ	
MC1345P	TBA550
MC1350P	U6A7757394
MC1351P	U6A7754394
MC1352P	U6A7757394
MC1353P	U6A7757394
MC1353PQ	U7F7757394
MC1355P	U6A7754394
MC1355PQ	U7F7754394
MC1357P	U6A7754394
MC1357PQ	U7F7754394
MC1414L	U6A7711393
MC1414P	U6A7711393
MC1429G	U5B7730393
MC1430F	U3F7702312
MC1430G	U5B7702393
MC1430L	U6A7702393
MC1430P	U6A7702393
MC1431F	U3F7702312
MC1431G	U5B7702393
MC1431L	U6A7702393
MC1431P	U6A7702393
MC1433F	U3F7101311
MC1433G	U5B7101392
MC1433L	U6A7101392
MC1436G	U5B7101392
MC1437L	U6A7749393
MC1437P	U6A7749393
MC1438P	U6A7749393
MC1439G	U5B7101392
MC1439L	U6A7101392
MC1440F	SN7525
MC1440G	SN7525
MC1440L	SN7525
MC1440P	SN7525
MC1441F	SN7524
MC1441L	SN7524
MC1441P	SN7524

MOTOROLA	FAIRCHILD FUNCTIONAL EQUIVALENT
MC1445F	U3F7733312
MC1445G	U5F7733393
MC1445L	U6A7733393
MC1446L	U6A7733393
MC1456G	U5T7725393
MC1458G	U5F7747393
MC1458P	U6A7747393
MC1460G	U5R7723393
MC1460R	U5R7723312
MC1461G	U5R7723393
MC1461R	U5R7723393
MC1463R	U5R7723393
MC1466L	U6A7723393
MC1469R	U5R7723393
MC1488L	U6A9616393
MC1489L	U6A9617393
MC1489AL	U6A9617393
MC1495L	
MC1496G	
MC1510F	U3F7733312
MC1510G	U5F7733312
MC1514L	U6A7711312
MC1519G	U5F7733312
MC1520F	U3F7101311
MC1520G	U5B7101311
MC1525G	U5B7730312
MC1526G	U5B7730312
MC1529G	U5B7730312
MC1530F	U3F7702312
MC1530G	U5B7702312
MC1531F	U3F7702312
MC1531G	U5B7702312
MC1533F	U3F7101311
MC1533G	U5B7101311
MC1533L	U6A7101311
MC1535F	U6A7749312
MC1535G	U6A7749312
MC1536G	U5B7741312
MC1537L	U6A7749312
MC1539G	U5B7101311
MC1539L	U6A7101311
MC1540F	SN7525
MC1540G	SN7525
MC1540L	SN7525
MC1541F	SN7524
MC1541L	SN7524
MC1543L	SN7524
MC1545F	U3F7733312
MC1545G	U5F7733312

MOTOROLA	FAIRCHILD DIRECT REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT
MC1545L		U6A7733312
MC1546L		U6A7733312
MC1550F		U6A7757312
MC1550G		U6A7757312
MC1552G		U5F7715312
MC1553G		U5F7715312
MC1556G		U5T7725312
MC1558G		U5F7747312
MC1558P		U6A7747312
MC1560G		U5R7723312
MC1560R		U5R7723312
MC1561G		U5R7723312
MC1561R		U5R7723312
MC1563R		U5R7723312
MC1566L		U6A7723312
MC1569R		U5R7723312
MC1580L		U6B961551X
MC1582L		U6B961451X
MC1583L		U6B961551X
MC1584L		U6B961551X
MC1590G		U6A7757394
MC1595L		
MC1596G		
MC1709CF		
MC1709CG		
MC1709CL		
MC1709F	U3F7709312	
MC1709G		
MC1709L		
MC1710CF		
MC1710CG		
MC1710CL		

MOTOROLA	FAIRCHILD DIRECT REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT
MC1710F	U3F7710312	
MC1710G		
MC1710L		
MC1711CF	U3F7711312	
MC1711CG		
MC1711CL		
MC1711F	U3F7711312	
MC1711G		
MC1711L		
MC1712CF		
MC1712CG		
MC1712CL		
MC1712F		
MC1712L		
MC1723CG		
MC1723G		
MC1723CL		
MC1723L		
MC1741CF		
MC1741CG		
MC1741CL		
MC1741CP		
MC1741F		
MC1741G		
MC1741G		
MC1741L		
MFC4060		U5R7723393
MFC6010		U5Z7703394
MFC8000		U6A7739393
MFC8001		U6A7739393
MFC8002		U6A7739393
MFC8040		UGH7791393

NATIONAL	FAIRCHILD DIRECT REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT
LH101		U5B7741312
LH101D		U6A7741312
LH101F		U3F7741312
LH201		U5B7741393
LH740A		U5B7740312
LH740AC		U5B7740393
LM100		U5R7723312
LM101		
LM101A		
LM101AD		
LM101D		
LM101F		
LM104		U5R7723312
LM105		U5R7723312
LM106		U5B7710312
LM106F		U3F7710312
LM107		U5B7741312
LM107D		U6A7741312
LM107F		U3F7741312
LM109K		
LM110		U5B7741312
LM111		U5B7734312

NATIONAL	FAIRCHILD DIRECT REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT
LM112		U5B7776312
LM201		
LM201A		
LM201AF		
LM201AD		
LM207		U5B7741312
LM207D		U6A7741312
LM207F		U3F7741312
LM209K		
LM210		U5B7741312
LM211		U5B7734312
LM212		U5B7776312
LM300		U5R7723393
LM301A		
LM301AD		
LM301AF		
LM304		U5R7723393
LM305		U5R7723393
LM306		U5B7710393
LM307		U5B7741393
LM307D		U6A7741393

NATIONAL	FAIRCHILD DIRECT REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT
LM307F		U3F7741393
LM309K	LM309K	
LM310		U5B7741393
LM311		U5B7734393
LM312		U5B7776393
LM376		U6A7723393
LM701C	U5B7710393	
LM703L	U5B7703393	
LM709	U5B7709312	
LM709A	U5B7709311	
LM709C	U5B7709393	
LM709CN	U6A7709393	
LM710	U5B7710312	
LM710A	U5B7710312	
LM710CN	U6A7710393	
LM711	U5F7711312	
LM711C	U5F7711393	
LM711CN	U6A7711393	
LM723	U6R7723312	
LM723C	U5R7723393	
LM741	U5B7741312	
LM741C	U5B7741393	
LM748	U5B7748312	
LM748C	U5B7748393	
LM1303	U6A7739393	
LM1304	U6A7732394	
LM1305	U6A7732394	
LM1458		U5F7747312
LM1558		U5F7747393
LM3065	CA3065	
LM7524	SN7524	
LM7525	SN7525	

RCA	FAIRCHILD DIRECT REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT
CA3000		U5B7702312
CA3001		U5F7733312
CA3002		U5Z7703394
CA3004		U5Z7703394
CA3005		U5Z7703394
CA3006		U5Z7703394
CA3007		U5B7716393
CA3008		U3F7702312
CA3010		U5B7702312
CA3011		U5E7754394
CA3012		U5E7754394
CA3013		U5E7754394
CA3014		U5Z7754394
CA3015		U5B7702312
CA3016		U3F7702312
CA3018	CA3018	
CA3019	CA3019	
CA3021		U6A7757394
CA3022		U6A7757394
CA3023		U6A7757394
CA3026	CA3026	
CA3028		U5Z7703394
CA3028A		U5Z7703394
CA3029		U6A7702393
CA3030		U6A7702393
CA3031	U5B7702312	
CA3032	U5B7702393	
CA3033		U6A7709312
CA3035		U6A7739393
CA3036	CA3036	
CA3037		U6A7709312
CA3038		U6A7709312
CA3039	CA3039	
CA3040		U5F7733312
CA3041		CA3065
CA3042		CA3065
CA3043		CA3065
CA3044		
CA3045	CA3045	
CA3046	CA3046	
CA3047		U6A7709393
CA3048		U6A7749393
CA3052		U6A7739393
CA3053		U5Z7703394
CA3054	CA3054	
CA3055		U5R7723312
CA3056A		U5B7702312
CA3059		U6A7742393
CA3060		U6A7739393
CA3064	CA3064	
CA3065	CA3065	
CA3066	CA3066	
CA3067	CA3067	
CA3068	CA3068	
CA3075	CA3075	
CA3076	CA3076	

SIGNETICS	FAIRCHILD FUNCTIONAL EQUIVALENT
SE501K	U5B7733312
NE501K	U5B7733393
NE501A	U6A7733393
NE510A	U6A7754394
NE511A	CA3045
SE515K	U5B7730312
NE515K	U5B7730393
SE518K	U5F7711312
NE518K	U5F7711393
NE518A	U6A7711393
SE526K	U5B7710312
NE526K	U5B7710393
NE526A	U6A7710393
NE528B	U7B7525393
SE528E	U7B7525312
SE528R	U7B7525312
SE531T	U5F7715312
NE531T	U5F7715393
SE533T	U5B7776312
NE533T	U5B7776393
SE536T	
NE536T	
SE550L	U5R7723312
NE550L	U5R7723393
NE550A	U6A7723393
S5101T	
S51A1T	U5B7101312
S51A8T	U5B7108312
N5201T	
N5201A	U6A7101333
N53A1T	U5B7101392
N53A1V	U9T7101393
N53A8T	U6B7108392
N5595A	U6A7795393

SIGNETICS	FAIRCHILD FUNCTIONAL EQUIVALENT
S5595F	
S5596K	
N5596K	
N5596A	U6A7796393
S5709T	
N5709T	
N5709A	U6A7709393
S5710T	
N5710T	
N5710A	U6A7710393
S5711K	
S5711T	U5F7711312
N5711K	
N5711A	U6A7711393
S5723L	
N5723L	
N5723A	U6A7723393
S5733K	
N5733K	
N5733A	U6A7733393
S5733F	
S5740T	
N5740T	
S5741T	
N5741T	
N5741A	U6A7741393
N5741V	
S5748T	
N5748T	
N5748A	U6A7748393
N5748V	
N7524B	
N7525B	

SPRAGUE	FAIRCHILD FUNCTIONAL EQUIVALENT
ULN2111A	U6A7754394
ULN2111N	U7F7754394
ULN2113A	U6A7754394
ULN2113N	U7F7754394
ULN2114A	
ULN2114K	
ULN2114N	
ULN2114W	
ULN2120A	
ULN2120N	
ULN2121A	U6A7767394
ULN2121N	U7F7767394
ULN2122A	
ULN2122N	

SPRAGUE	FAIRCHILD FUNCTIONAL EQUIVALENT
ULN2124A	
ULN2124N	
ULN2126A	U6A7739393
ULN2126N	U7F7739393
ULN2127A	
ULN2127N	
ULN2128A	
ULN2128N	
ULN2129A	
ULN2129N	
ULN2131A	U6A7754394
ULN2131N	U7F7754394
ULN2165A	
ULN2165N	

TI	FAIRCHILD FUNCTIONAL EQUIVALENT
SN5512L	U5F7733312
SN7512L	U5F7733393
SN5514L	U5F7733312
SN7514L	U5F7733393
SN55107AJ	
SN75107AJ	
SN75107AN	
SN55108AJ	
SN75108AJ	
SN75108AN	
SN55109J	
SN75109J	
SN75109N	
SN55110J	
SN75110J	
SN75110N	
SN75150J	U6A9616393
SN75150N	U6A9616393
SN75150P	U6A9616393
SN75100L	U7B961559X
SN75154J	U6A9617393
SN75154N	U6A9617393
SN52702AL	U5B7702312
SN52702AS	U3F7702312
SN52702L	U5B7702312
SN52702S	U3F7702312
SN72702N	U6A7702393
SN52702N	U6A7702312
SN72702L	U5B7702312
SN72702S	U3F7702312
SN52101J	
SN52101AL	
SN52101AZ	
SN72301AJ	
SN72301AN	
SN72301AL	
SN72301AZ	
SN52107J	U6A7777312
SN52107L	U5B7777312
SN52107S	U3F7777312
SN72107J	U6A7777393
SN72307N	U6A7777393
SN72307P	U9T7777393
SN72307L	U5B7777393
SN72307Z	U3F7777312
SN52709AL	U5B7709311
SN52709AS	U3F7709311
SN52709AN	U6A7709311
SN52709AJ	
SN52709N	U6A7709312
SN52709J	U6A7709312
SN52709L	U5B7709393
SN52709S	U3F7709312
SN72709N	U6A7709393
SN72709J	U6A7709393
SN72709L	U5B7709393
SN72709S	U3F7709312
SN52701J	U6A7710312
SN52710N	U6A7710312
SN52710L	U5B7710312
SN52710S	U3F7710312
SN72710J	U6A7710393

TI	FAIRCHILD FUNCTIONAL EQUIVALENT
SN73710N	
SN72710L	
SN72710S	
SN52810J	U6A7710312
SN52810N	U6A7710312
SN52810L	U5B7710312
SN52810Z	U3F7710312
SN72810J	U6A7710393
SN72810J	U6A7710393
SN72810P	U6A7710393
SN72810L	U5B7710393
SN72810Z	U3F7710312
SN52510J	U6A7710312
SN52510N	U6A7710312
SN52510L	U5B7710312
SN52510Z	U3F7710312
SN72510J	U6A7710393
SN72510N	U6A7710393
SN72510P	U6A7710393
SN72510L	U5B7710393
SN72510Z	U3F7710312
SN52711J	
SN52711N	
SN52711L	
SN52711S	
SN72711J	
SN72711N	
SN72711L	
SN72711S	
SN52811J	U6A7711312
SN52811N	U6A7711312
SN52811L	U5F7711312
SN72811J	U6A7711393
SN72811P	U6A7711393
SN72811L	U5F7711393
SN2720N	U6A7711393
SN52820J	U6A7734312
SN52820N	U6A7734312
SN72820J	U6A7734393
SN52733N	
SN52733L	
SN72733N	
SN72733L	
SN5510L	U5F7733312
SN5510F	U3F7733312
SN52741J	
SN52741N	
SN52741L	
SN52741Z	
SN72741N	
SN72741J	
SN72741P	
SN72741L	
SN72741Z	
SN52558L	U5F7747312
SN72558P	U7A7747393
SN72558L	U5F7747312
SN52747J	U7A7747312
SN52747N	U7A7747314
SN52747L	U5F7747312
SN72747J	U7A7747393
SN72747N	U7A7747393

TI	FAIRCHILD DIRECT REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT
SN72747L		
SN52748J		
SN52748N		
SN52748L		
SN52748Z		
SN72748J		
SN72748N		
SN72748P		
SN72748L		
SN72748Z		
SN52770L		U5B7740312
SN72770L		U5B7740393
SN52771L		U5B7740312
SN72771L		U5B7740393
SN7524J		
SN7524N		
SN7525J		
SN7525N		
SN75235J		
SN75235N		
SN75450AN		

TI	FAIRCHILD DIRECT REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT
SN75451AP		
SN72400N		U6A7723393
SN72400L		U5R7723393
SN56514J		U6A7796393
SN56514N		U6A7706393
SN56514L		U5F7796393
SN76110N		
SN76104		
SN76105		
SN76131		
SN76242		
SN76243		
SN76246		
SN76630		
SN76533		
SN76564		
SN76619		U5Z7703394
SN76640		U6A7754394
SN76660		CA3065
SN76665		
SN76110		

Data Sheets

μA101

HIGH PERFORMANCE OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

- **SHORT-CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **LOW POWER CONSUMPTION**
- **NO LATCH UP**

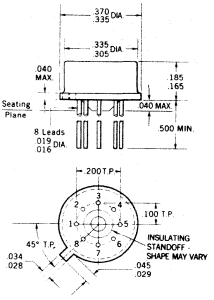
GENERAL DESCRIPTION — The μA101 is a high performance monolithic operational amplifier electrically and pin for pin equivalent to the LM101 constructed on a single silicon chip, using the Fairchild Planar* epitaxial process. It is intended for a wide range of analog applications where tailoring of frequency characteristics is desirable. The μA101 compensates easily with a single external component. High common mode voltage range and absence of "latch-up" make the μA101 ideal for use as a voltage follower. The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier, and general feedback applications. The μA101 is short-circuit protected and has the same pin configuration as the popular μA741, μA748 and μA709. (For Other Fairchild Operational Amplifiers, See Listing Below)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22 V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 60 seconds)	300°C
Output Short-Circuit Duration (Note 3)	Indefinite

PHYSICAL DIMENSIONS

In accordance with JEDEC (TO-99) outline

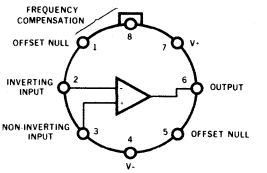


NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.22 grams

ORDER PART NO. U5B7101312

CONNECTION DIAGRAM

(TOP VIEW)



NOTE: Pin 4 connected to case

*Planar is a patented Fairchild process.

NOTES:

(1) Rating applies for case temperatures to 125°C; derate linearly at 6.5 mW/°C for ambient temperatures above +75°C.
(2) For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
(3) Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

NOTE:

FOR OTHER FAIRCHILD OPERATIONAL AMPLIFIERS, SEE THE FOLLOWING DATA SHEETS:

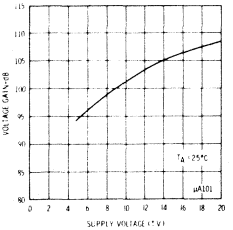
HIGH SPEED — μA715, μA715C
INSTRUMENTATION — μA725, μA725B, μA725C
TEMPERATURE STABLE PREAMPS — μA727, μA727B
MICROPOWER — μA735, μA735B, μA735C
FET INPUT — μA740, μA740C
FREQUENCY COMPENSATED — μA741, μA741C
DUALS — μA739C, μA749, μA749C, μA747, μA747C
HIGH PERFORMANCE — μA201, μA748, μA748C
PRECISION — μA777, μA777B, μA777C

FAIRCHILD
SEMICONDUCTOR

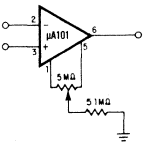
ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $C_C = 30$ pF, $T_A = 25°C$ unless otherwise specified)

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	5.0	mV
Input Offset Current			20	200	nA
Input Bias Current			80	500	nA
Input Resistance		0.3	2.0		MΩ
Input Capacitance			1.4		pF
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	50,000	200,000		
Output Resistance			75		Ω
Output Short-Circuit Current			25		mA
Power Consumption			50	85	mW
Transient Response (unity gain)	$V_{in} = 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF				
Risetime			0.3		μs
Overshoot			5.0		%
Slew Rate	$R_L \geq 2$ kΩ		0.5		V/μs
The following specifications apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	6.0	mV
Input Offset Current	$T_A = +125°C$		7.0	200	nA
	$T_A = -55°C$		85	500	nA
Input Bias Current	$T_A = +125°C$		0.03	0.5	μA
	$T_A = -55°C$		0.3	1.5	μA
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150	μV/V
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	25,000			
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		V
Power Consumption	$T_A = +125°C$		45	75	mW
	$T_A = -55°C$		60	100	mW

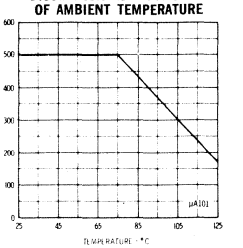
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



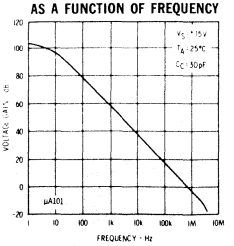
VOLTAGE OFFSET NULL CIRCUIT



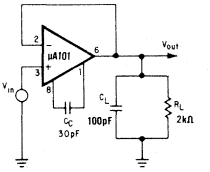
ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



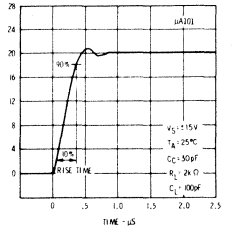
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



TRANSIENT RESPONSE TEST CIRCUIT



TRANSIENT RESPONSE



μA101A . μA201A . μA301A
GENERAL PURPOSE OPERATIONAL AMPLIFIERS
FAIRCHILD LINEAR INTEGRATED CIRCUITS

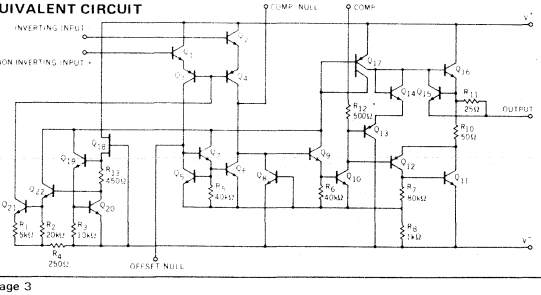
- **LOW OFFSET CURRENT AND VOLTAGE**
- **LOW OFFSET CURRENT DRIFT**
- **LOW BIAS CURRENT**
- **SHORT CIRCUIT PROTECTED**
- **LOW POWER CONSUMPTION**

GENERAL DESCRIPTION – The μA101A, μA201A and μA301A are general purpose monolithic operational amplifiers constructed on a single silicon chip, using the Fairchild Planar* epitaxial process. These integrated circuits are intended for applications requiring low input offset voltage or low input offset current. The accuracy of long interval integrators, timers and sample and hold circuits is improved due to the low drift and low bias currents of the μA101A, μA201A, or μA301A. Frequency response may be matched to the individual circuit need with one external capacitor. The absence of "Latch-Up" coupled with internal short circuit protection make the μA101A, μA201A and μA301A virtually foolproof. The μA101A, μA201A, and μA301A are pin compatible with the popular μA709, μA741, μA748 and μA777 . (For other Fairchild operational amplifiers, see last page.)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
Military and Instrument (311 and 333 grades)	±22 V
Commercial (392 grade)	±18 V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	
Metal Can, Ceramic DIP, and Flatpak	-65°C to + 150°C
Mini DIP and Silicon DIP	-55°C to + 125°C
Operating Temperature Range	
Military (311 grade)	-55°C to + 125°C
Instrument (333 grade)	−25°C to + 85°C
Commercial (392 grade)	0°C to + 70°C
Lead Temperature (Soldering,	
Metal Can, Ceramic DIP and Flatpak (60 seconds)	300°C
Mini DIP and Silicone DIP (10 seconds)	260°C
Output Short Circuit Duration (Note 3)	Indefinite

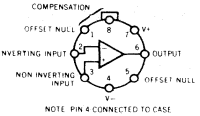
EQUIVALENT CIRCUIT



Notes on page 3

CONNECTION DIAGRAMS
(TOP VIEW)

8 LEAD METAL CAN

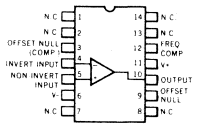


NOTE: PIN 4 CONNECTED TO CASE

ORDER PART NOS.

DEVICE TYPE	PRODUCT CODE
μA101AH	U5B7101311
μA201AH	U5B7101333
μA301AH	U5B7101392

14 LEAD DIP



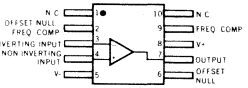
FOR CERAMIC DIP ORDER PART NOS.:

DEVICE TYPE	PRODUCT CODE
μA101AD	U6A7101311
μA201AD	U6A7101333
μA301AD	U6A7101392

FOR SILICONE DIP ORDER PART NO.:

μA301AP	U9A7101392

FLATPACK

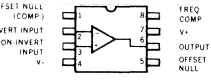


ORDER PART NOS.

DEVICE TYPE	PRODUCT CODE
μA101AF	U3F7101311*
μA201AF	U3F7101333*

*Available on special request

MINIDIP



ORDER PART NO.

DEVICE TYPE	PRODUCT CODE
μA301AN	U9T7101392

*Planar is a patented Fairchild process.

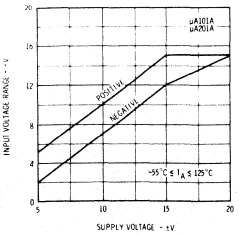
FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS FOR μA101A and μA201A ($\pm 5.0V \leq V_S \leq \pm 20V$, $T_A = 25°C$, $C_1 = 30$ pF unless otherwise specified)

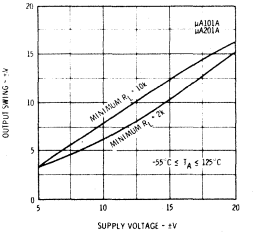
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 50\ k\Omega$		0.7	2.0	mV
Input Offset Current			1.5	10	nA
Input Bias Current			30	75	nA
Input Resistance		1.5	4.0		MΩ
Supply Current	$V_S = \pm 20V$		1.8	3.0	mA
Large Signal Voltage Gain	$V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2\ k\Omega$	50	160		V/mV
The following specifications apply for $-55°C \leq T_A \leq +125°C$: (Note 4)					
Input Offset Voltage	$R_S \leq 50\ k\Omega$			3.0	mV
Average Temperature Coefficient of Input Offset Voltage			3.0	15	μV/°C
Input Offset Current				20	nA
Average Temperature Coefficient of Input Offset Current	$+25°C \leq T_A \leq +125°C$ $-55°C \leq T_A \leq +25°C$		0.01 0.02	0.1 0.2	nA/°C nA/°C
Input Bias Current				100	nA
Supply Current	$T_A = +125°C$, $V_S = \pm 20V$		1.2	2.5	mA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2\ k\Omega$	25			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$ $R_L = 2\ k\Omega$	±12 ±10	±14 ±13		V V
Input Voltage Range	$V_S = \pm 20V$	±15			V
Common Mode Rejection Ratio	$R_S \leq 50\ k\Omega$	80	96		dB
Supply Voltage Rejection Ratio	$R_S \leq 50\ k\Omega$	80	96		dB

GUARANTEED PERFORMANCE CURVES (μA101A AND μA201A)

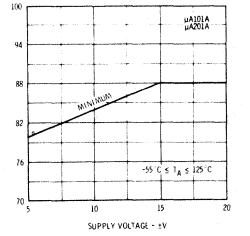
INPUT VOLTAGE RANGE VS. SUPPLY



OUTPUT SWING VS. SUPPLY



VOLTAGE GAIN VS. SUPPLY



ELECTRICAL CHARACTERISTICS FOR μA301A ($\pm 5.0\,V \leq V_S \leq \pm 15V$, $T_A = 25°C$, $C_1 = 30\,pF$ unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 50\,k\Omega$		2.0	7.5	mV
Input Offset Current			3	50	nA
Input Bias Current			70	250	nA
Input Resistance		0.5	2		MΩ
Supply Current	$V_S = \pm 15V$		1.8	3.0	mA
Large Signal Voltage Gain	$V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2\,k\Omega$	25	160		V/mV
The following specifications apply for $0°C \leq T_A \leq 70°C$:					
Input Offset Voltage	$R_S \leq 50\,k\Omega$			10	mV
Average Temperature Coefficient of Input Offset Voltage			6.0	30	μV/°C
Input Offset Current				70	nA
Average Temperature Coefficient of Input	$25°C \leq T_A \leq 70°C$ $0°C \leq T_A \leq 25°C$		0.01 0.02	0.3 0.6	nA/°C nA/°C
Input Bias Current				300	nA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2\,k\Omega$	15			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\,k\Omega$ $R_L = 2\,k\Omega$	±12 ±10	±14 ±13		V V
Input Voltage Range	$V_S = \pm 15V$	±12			V
Common Mode Rejection Ratio	$R_S \leq 50\,k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 50\,k\Omega$	70	96		dB

NOTES:

(1) Absolute maximum rating holds for all packages. The maximum junction temperature of the μA 101A is 150°C, while that of the μA 201A and μA 301A is 100°C. For operation at elevated temperature devices in the TO-99 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. Thermal resistance of the DIP package is 100°C/W, junction to ambient. Flat pack derating is based on a thermal resistance of 185°C/W. All μA 301A ratings apply for ambient temperatures to +70°C.

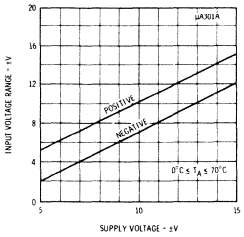
(2) For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

(3) Short circuit may be to ground or either supply. μA 101A and μA 201A ratings apply to +125°C case temperature or +75°C ambient temperature. μA 301A ratings apply for case temperatures to 70°C.

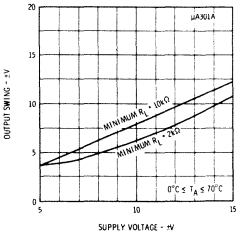
(4) All **μA201A** specifications apply for $-25°C \leq T_A \leq +85°C$ unless otherwise specified.

GUARANTEED PERFORMANCE CURVES (μA301A)

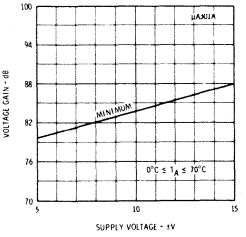
INPUT VOLTAGE RANGE VS. SUPPLY



OUTPUT SWING VS. SUPPLY

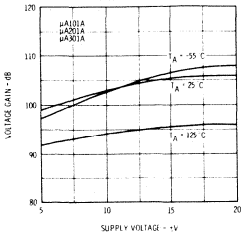


VOLTAGE GAIN VS. SUPPLY

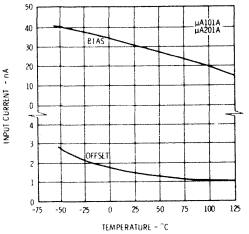


TYPICAL PERFORMANCE CURVES

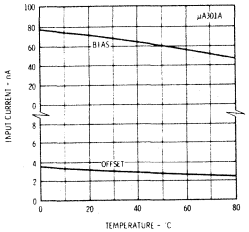
VOLTAGE GAIN



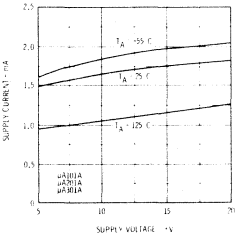
INPUT CURRENT (μA101A AND μA201A)



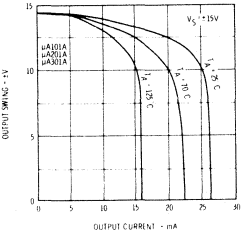
INPUT CURRENT (μA301A)



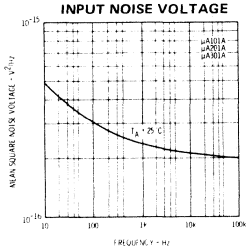
SUPPLY CURRENT



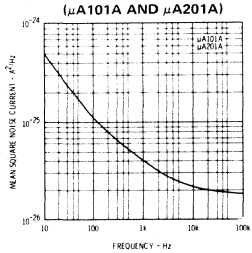
CURRENT LIMITING



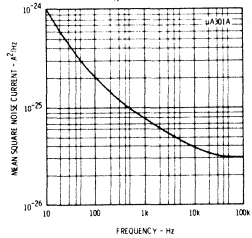
INPUT NOISE VOLTAGE



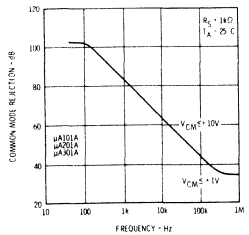
INPUT NOISE CURRENT (μA101A AND μA201A)



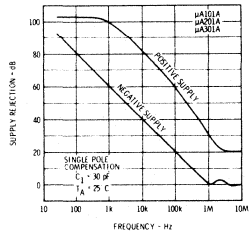
INPUT NOISE CURRENT (μA301A)



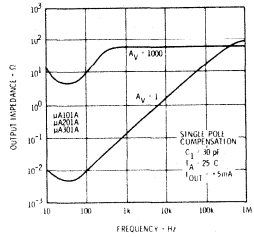
COMMON MODE REJECTION



POWER SUPPLY REJECTION

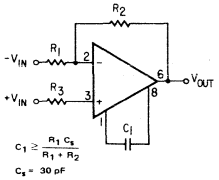


CLOSED LOOP OUTPUT IMPEDANCE

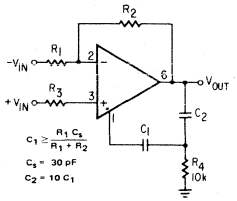


COMPENSATION CIRCUITS

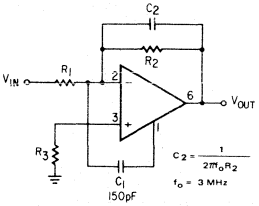
SINGLE POLE COMPENSATION



TWO POLE COMPENSATION

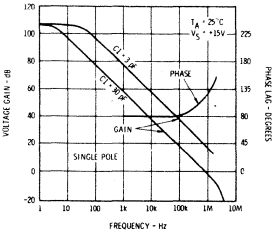


FEEDFORWARD COMPENSATION

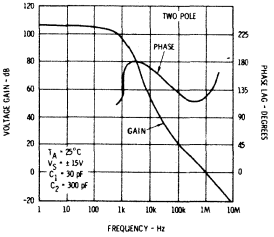


TYPICAL PERFORMANCE CURVES

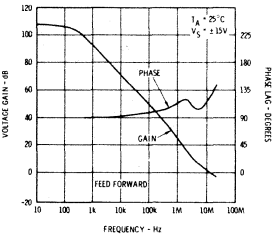
OPEN LOOP FREQUENCY RESPONSE



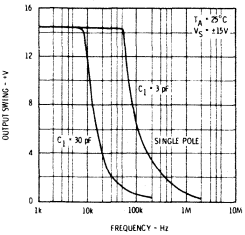
OPEN LOOP FREQUENCY RESPONSE



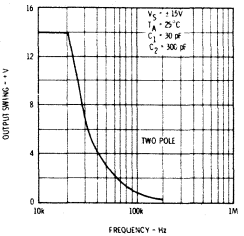
OPEN LOOP FREQUENCY RESPONSE



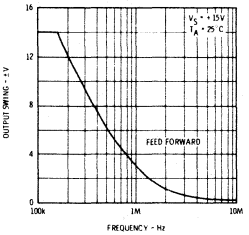
LARGE SIGNAL FREQUENCY RESPONSE



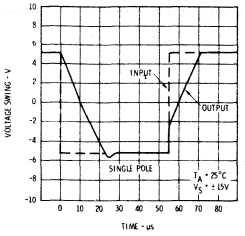
LARGE SIGNAL FREQUENCY RESPONSE



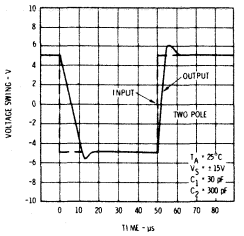
LARGE SIGNAL FREQUENCY RESPONSE



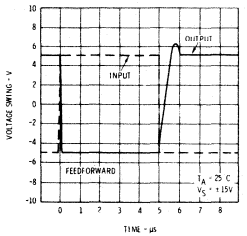
VOLTAGE FOLLOWER PULSE RESPONSE



VOLTAGE FOLLOWER PULSE RESPONSE



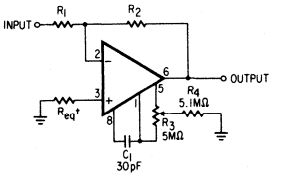
INVERTER PULSE RESPONSE



TYPICAL APPLICATIONS

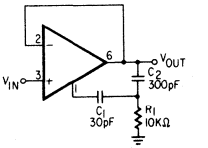
(All pin numbers shown refer to 8 pin TO-5 package)

INVERTING AMPLIFIER –WITH BALANCING CIRCUIT



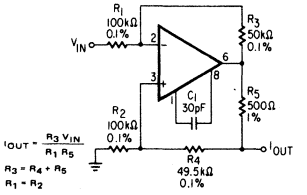
† May be zero or equal to parallel combination of R1 and R2 for minimum offset.

FAST VOLTAGE FOLLOWER



Power Bandwidth: 15 kHz
Slew Rate: 1V/μs

BILATERAL CURRENT SOURCE

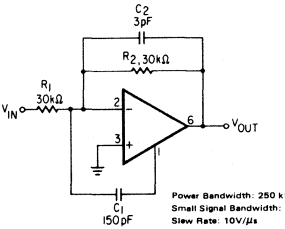


$I_{OUT} = \frac{R_3 V_{IN}}{R_1 R_5}$

$R_3 = R_4 + R_5$

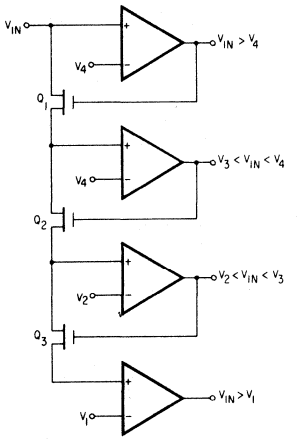
$R_1 = R_2$

FAST SUMMING AMPLIFIER

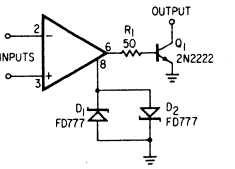


Power Bandwidth: 250 kHz
Small Signal Bandwidth: 3.5 MHz
Slew Rate: 10V/μs

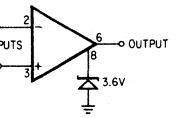
MULTIPLE APERTURE WINDOW DISCRIMINATOR



VOLTAGE COMPARATOR FOR DRIVING RTL LOGIC OR HIGH CURRENT DRIVER



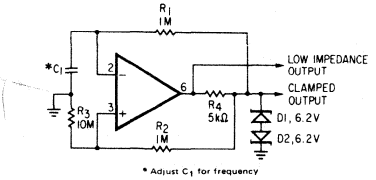
VOLTAGE COMPARATOR FOR DRIVING DTμL OR TTμL INTEGRATED CIRCUITS



TYPICAL APPLICATIONS (CON'D)

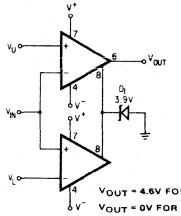
(All pin numbers shown refer to 8 pin TO-5 package)

LOW FREQUENCY SQUARE WAVE GENERATOR



* Adjust C_1 for frequency

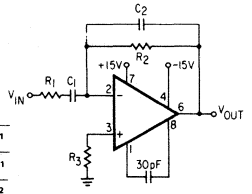
DOUBLE ENDED LIMIT DETECTOR



V_{OUT} = 4.6V FOR $V_L \leq V_{IN} \leq V_U$

V_{OUT} = 0V FOR $V_{IN} < V_L$ OR $V_{IN} < V_U$

PRACTICAL DIFFERENTIATOR

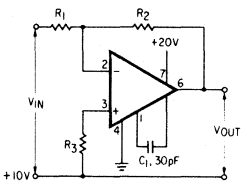


$f_c = \frac{1}{2\pi R_2 C_1}$

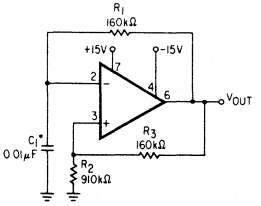
$f_h = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi R_2 C_2}$

$f_c < f_h <$ funity gain

CIRCUIT FOR OPERATING THE μA101A WITHOUT A NEGATIVE SUPPLY

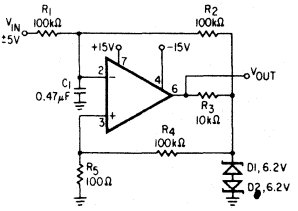


FREE-RUNNING MULTIVIBRATOR

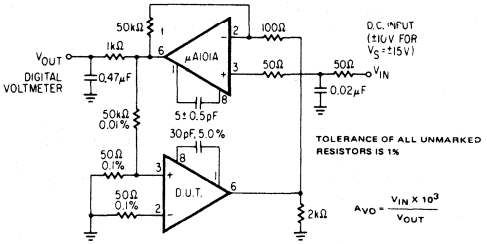


* Chosen for oscillation at 100 Hz

PULSE WIDTH MODULATOR

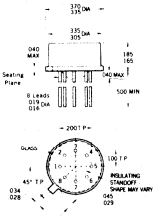


GAIN TEST CIRCUIT



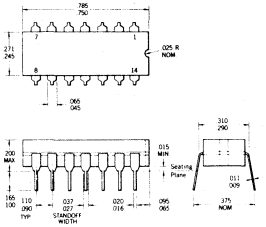
PHYSICAL DIMENSIONS

METAL CAN 5B PACKAGE

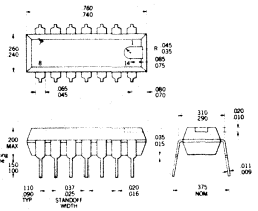


NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.22 grams

CERAMIC DIP 6A PACKAGE



SILICONE DIP 9A PACKAGE



NOTES FOR DIP'S

All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for .020 inch diameter lead.

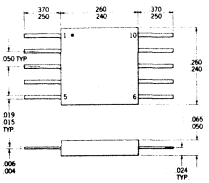
6A
Leads are tin-plated kovar
Package weight is 2.0 grams

9A
Leads are gold-plated kovar
Package weight is 0.9 gram

9T
Leads are tin-plated kovar
Package weight is 0.6 gram
Package material is silicone

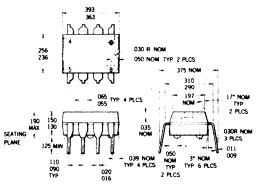
FLATPACK 3F PACKAGE

In accordance with JEDEC (TO-91) outline



NOTES:
All dimensions in inches
Package weight is 0.26 gram
Leads are gold-plated kovar
Available on special request

MINIDIP 9T PACKAGE



DEFINITION OF TERMS

INPUT OFFSET VOLTAGE – That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT – The difference in the currents into the two input terminals with the output at zero volts.

INPUT BIAS CURRENT – The average of the two input currents.

INPUT RESISTANCE – The resistance looking into either input terminal with the other grounded.

INPUT CAPACITANCE – The capacitance looking into either input terminal with the other grounded.

LARGE-SIGNAL VOLTAGE GAIN – The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT RESISTANCE – The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

OUTPUT SHORT-CIRCUIT CURRENT – The maximum output current available from the amplifier with the output shorted to ground or to either supply.

SUPPLY CURRENT – The DC current from the supplies required to operate the amplifier with the output at zero and with no load current.

POWER CONSUMPTION – The DC power required to operate the amplifier with the output at zero and with no load current.

TRANSIENT RESPONSE – The closed-loop step-function response of the amplifier under small-signal conditions.

INPUT VOLTAGE RANGE – The range of voltages on the input terminals for which the offset specifications apply.

INPUT COMMON MODE REJECTION RATIO – The ratio of the input voltage range to the maximum change in input offset voltage over this range.

SUPPLY VOLTAGE REJECTION RATIO – The ratio of the change in input offset voltage to the change in supply voltage producing it.

OUTPUT VOLTAGE SWING – The peak output swing, referred to zero, that can be obtained without clipping.

NOTES:

FOR OTHER FAIRCHILD OPERATIONAL AMPLIFIERS, SEE THE FOLLOWING DATA SHEETS:

HIGH SPEED – μA715, μA715C
INSTRUMENTATION – μA725, μA725B, μA725B
TEMPERATURE STABLE PREAMPS – μA727, μA727B
MICROPOWER – μA735, μA735B, μA735C
FET INPUT – μA740, μA740C
FREQUENCY COMPENSATED – μA741, μA741C
DUALS – μA749, μA749C, μA747, μA747C
HIGH PERFORMANCE – μA748, μA748C
PROGRAMMABLE – μA776, μA776C
PRECISION – μA777, μA777C

μA109 . μA209 . μA309
5 VOLT REGULATOR
FAIRCHILD LINEAR INTEGRATED CIRCUITS

- **OUTPUT CURRENT IN EXCESS OF 1 AMP**
- **SPECIFIED TO MATCH WORST CASE TTμL AND DTμL REQUIREMENTS**
- **NO EXTERNAL COMPONENTS**
- **INTERNAL THERMAL OVERLOAD PROTECTION**
- **OUTPUT TRANSISTOR SAFE-AREA COMPENSATION**

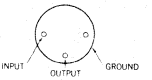
GENERAL DESCRIPTION – The μA109, μA209 and μA309 are complete 5 volt regulators constructed on a single silicon chip using the Fairchild Planar* epitaxial process. These regulators employ internal current limiting, thermal shutdown and safe-area compensation making them essentially blow-out proof. They are intended for use as local regulators, eliminating noise and distribution problems associated with single point regulation. If adequate heat sinking is provided, they can provide over 200 mA output current in the TO-5 package and over 1 A in the TO-3 package. The μA109, μA209 and μA309 are intended primarily for use with TTμL and DTμL logic and are completely specified under worst case conditions to match the power supply requirements of these logic families. In addition to use as a fixed 5 volt regulator, these devices can be used with external components to obtain adjustable output voltages and currents and as the power pass element in precision regulators.

For information on other Fairchild voltage regulators and power control circuits, see listing on last page.

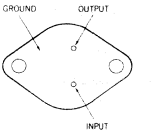
ABSOLUTE MAXIMUM RATINGS

Input Voltage		35 V
Internal Power Dissipation		Internally Limited
Storage Temperature Range		-65°C to + 150°C
Operating Junction Temperature Range	μA109	-55°C to + 150°C
	μA209	-25°C to + 150°C
	μA309	0°C to + 125°C
Lead Temperature (Soldering, 60 second time limit)		300°C

CONNECTION DIAGRAM
TO-5 PACKAGE
(TOP VIEW)



TO-3 PACKAGE
(TOP VIEW)



Case is connected to ground.

ORDER PART NO:

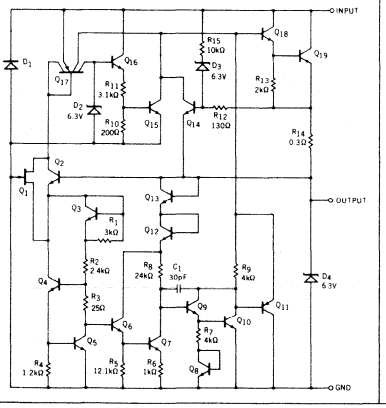
FOR TO-3 ORDER PART NOS.

DEVICE TYPE	PRODUCT CODE
μA109K	UGJ7109312
μA209K	UGJ7109333
μA309K	UGJ7109393

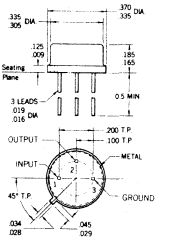
FOR TO-5 ORDER PART NOS.

DEVICE TYPE	PRODUCT CODE
μA109H	UBN7109312
μA209H	UBN7109333
μA309H	UBN7109393

EQUIVALENT CIRCUIT

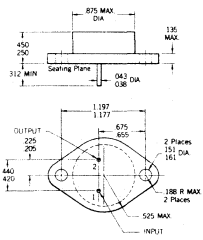


PHYSCIAL DIMENSIONS
TO-5 PACKAGE



NOTES:
All dimensions in inches.
Leads are gold-plated kovar.
Lead No. 3 connected to case.
Package weight is 0.9 gram.

PHYSCIAL DIMENSIONS
TO-3 PACKAGE



NOTES:
All dimensions in inches.
Leads 1 and 2 electrically isolated from case.
Case is third electrical connection.
Leads are gold-plated copper cored kovar.
Package weight is 7.4 grams.

*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS FOR μA109 AND μA209 (Note 1)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Voltage	$T_j = 25°C$	4.7	5.05	5.3	V
Line Regulation	$T_j = 25°C$				
	$7\ V \leqslant V_{IN} \leqslant 25\ V$		4	50	mV
Load Regulation	$T_j = 25°C$				
TO-5 Package	$5\ mA \leqslant I_{OUT} \leqslant 0.5A$		20	50	mV
TO-3 Package	$5\ mA \leqslant I_{OUT} \leqslant 1.5\ A$		50	100	mV
Output Voltage	$7\ V \leqslant V_{IN} \leqslant 25\ V$				
	$5\ mA \leqslant I_{OUT} \leqslant I_{MAX}$				
	$P \leqslant P_{MAX}$	4.6		5.4	V
Quiescent Current	$7\ V \leqslant V_{IN} \leqslant 25\ V$		5.2	10	mA
Quiescent Current Change	$7\ V \leqslant V_{IN} \leqslant 25\ V$			0.5	mA
	$5\ mA \leqslant I_{OUT} \leqslant I_{MAX}$			0.8	mA
Output Noise Voltage	$T_A = 25°C$				
	$10\ Hz \leqslant f \leqslant 100\ kHz$		40		μV
Long Term Stability				10	mV
Thermal Resistance					
Junction to Case (Note 2)					
TO-5 package			15		°C/W
TO-3 package			3		°C/W

ELECTRICAL CHARACTERISTICS FOR μA309 (Note 3)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Voltage	$T_j = 25°C$	4.8	5.05	5.2	V
Line Regulation	$T_j = 25°C$				
	$7\ V \leqslant V_{IN} \leqslant 25\ V$		4.0	50	mV
Load Regulation	$T_j = 25°C$				
TO-5 Package	$5\ mA \leqslant I_{OUT} \leqslant 0.5A$		20	50	mV
TO-3 Package	$5\ mA \leqslant I_{OUT} \leqslant 1.5\ A$		50	100	mV
Output Voltage	$7\ V \leqslant V_{IN} \leqslant 25\ V$				
	$5\ mA \leqslant I_{OUT} \leqslant I_{MAX}$	4.75		5.25	V
	$P \leqslant P_{MAX}$				
Quiescent Current	$7\ V \leqslant V_{IN} \leqslant 25\ V$		5.2	10	mA
Quiescent Current Change	$7\ V \leqslant V_{IN} \leqslant 25\ V$			0.5	mA
	$5\ mA \leqslant I_{OUT} \leqslant I_{MAX}$			0.8	mA
Output Noise Voltage	$T_A = 25°C$				
	$10\ Hz \leqslant f \leqslant 100\ kHz$		40		μV
Long Term Stability				20	mV
Thermal Resistance					
Junction to Case (Note 2)					
TO-5 package			15		°C/W
TO-3 package			3.0		°C/W

NOTES:

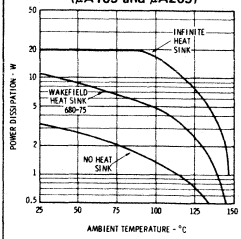
(1) Unless otherwise specified, these specifications apply for $-55°C \leqslant T_j \leqslant 150°C$ ($-25°C \leqslant T_j \leqslant 150°C$ for the μA209), $V_{IN} = 10\ V$ and $I_{OUT} = 0.1A$ for the TO-5 package or $I_{OUT} = 0.5A$ for the TO-3 package. For the TO-5 package, $I_{MAX} = 0.2A$ and $P_{MAX} = 2.0W$. For the TO-3 package, $I_{MAX} = 1.0A$ and $P_{MAX} = 20W$.

(2) Without a heat sink, the thermal resistance of the TO-5 package is about 150°C/W, while that of the TO-3 package is approximately 35°C/W. With a heat sink, the effective thermal resistance can only approach the values specified, depending on the efficiency of the sink.

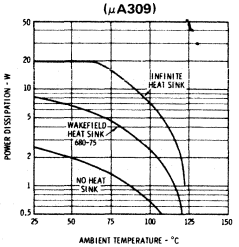
(3) Unless otherwise specified, these specifications apply for $0°C \leqslant T_j \leqslant 125°C$, $V_{IN} = 10\ V$ and $I_{OUT} = 0.1A$ for the TO-5 package or $I_{OUT} = 0.5A$ for the TO-3 package. For the TO-5 package, $I_{MAX} = 0.2A$ and $P_{MAX} = 2.0W$. For the TO-3 package, $I_{MAX} = 1.0A$ and $P_{MAX} = 20W$.

TYPICAL PERFORMANCE CURVES

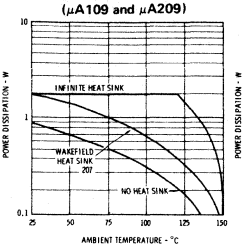
TO–3 MAXIMUM AVERAGE POWER DISSIPATION (μA109 and μA209)



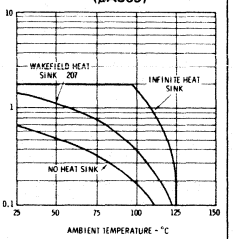
TO–3 MAXIMUM AVERAGE POWER DISSIPATION (μA309)



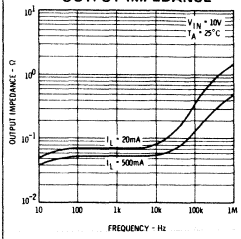
TO–5 MAXIMUM AVERAGE POWER DISSIPATION (μA109 and μA209)



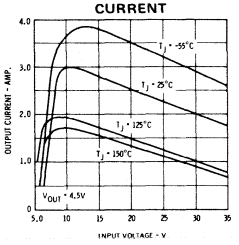
TO–5 MAXIMUM AVERAGE POWER DISSIPATION (μA309)



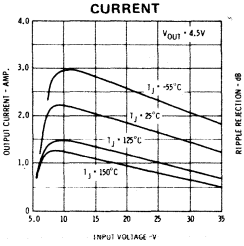
OUTPUT IMPEDANCE



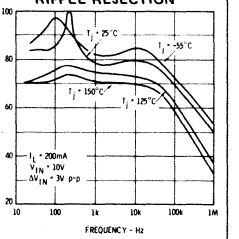
TO–3 PEAK OUTPUT CURRENT



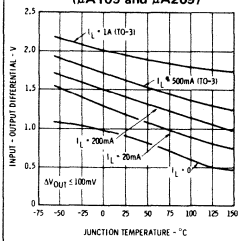
TO–5 PEAK OUTPUT CURRENT



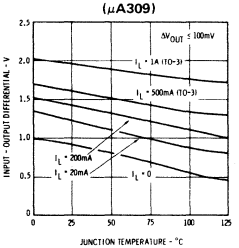
RIPPLE REJECTION



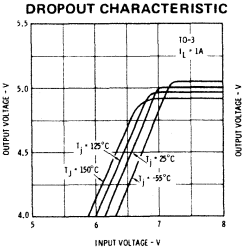
DROPOUT VOLTAGE (μA109 and μA209)



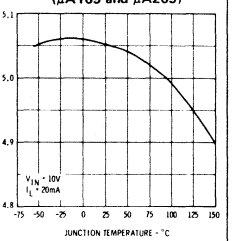
DROPOUT VOLTAGE (μA309)



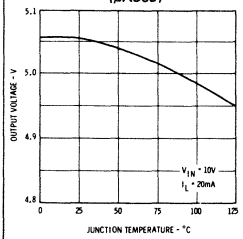
DROPOUT CHARACTERISTIC



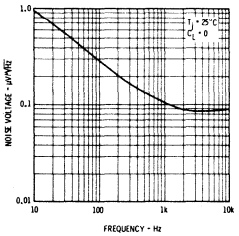
OUTPUT VOLTAGE (μA109 and μA209)



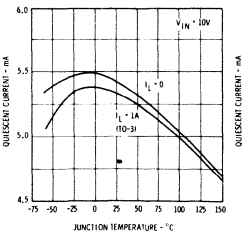
OUTPUT VOLTAGE (μA309)



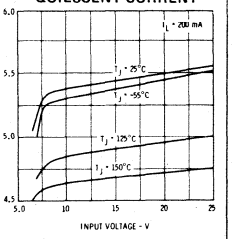
OUTPUT NOISE VOLTAGE



QUIESCENT CURRENT



QUIESCENT CURRENT



DEFINITION OF TERMS

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.

Dropout Voltage: The input-output voltage differential at which the circuit ceases to regulate against further reductions in input voltage.

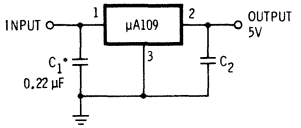
Maximum Power Dissipation: The maximum total device dissipation for which the regulator will operate within specifications.

Quiescent Current: That part of input current to the regulator that is not delivered to the load.

Output Noise Voltage: The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

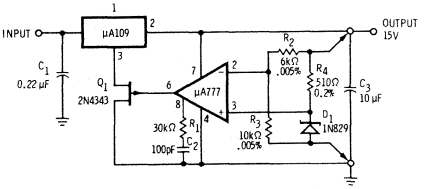
Long Term Stability: Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and power dissipation.

FIXED 5 V REGULATOR



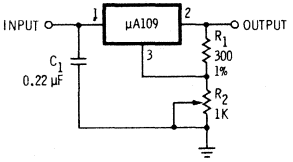
NOTES:
* Required if regulator is located an appreciable distance from power supply filter.
† Although no output capacitor is needed for stability, it does improve transient response.

PRECISION VOLTAGE REGULATOR

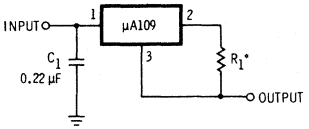


NOTES:
* Regulation better than 0.01% load, line and temperature, can be obtained.
† Determines zener current. May be adjusted to minimize thermal drift.
‡ Solid tantalum.

ADJUSTABLE OUTPUT REGULATOR



CURRENT REGULATOR



NOTES:
* Determines output current.

For information on other Fairchild Voltage Regulators and Power Control Circuits, see the following data sheets:

- ADJUSTABLE VOLTAGE REGULATORS:
  PRECISION POSITIVE OR NEGATIVE – μA723, μA723C
  POSITIVE – μA100, μA200, μA300, μA105, μA205, μA305 *
  NEGATIVE – μA104, μA204, μA304 *
- FIXED VOLTAGE REGULATORS: (other output values available on special request)
  5 VOLT – μA7805, μA7805C
  6 VOLT – μA7806, μA7806C
  12 VOLT – μA7812, μA7812C
  15 VOLT – μA7815, μA7815C
  24 VOLT – μA7824, μA7824C
- INSTRUMENTATION VOLTAGE/CURRENT REFERENCE: μA728, μA728B, μA728C (to be announced)
- AC POWER CONTROL
  ZERO CROSSING – μA742, μA742C
  PHASE CONTROL – μA743, μA743C *
- COMPARATOR/BUFFER: μA106, μA206, μA306 *
- DUAL POWER COMPARATOR: μA750, μA750C *

* TO BE ANNOUNCED

μA201
HIGH PERFORMANCE OPERATIONAL AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

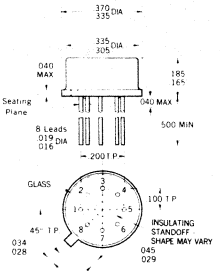
- **SHORT-CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **LOW POWER CONSUMPTION**
- **NO LATCH UP**

GENERAL DESCRIPTION — The μA201 is a high performance monolithic operational amplifier electrically and pin for pin equivalent to the LM201 constructed on a single silicon chip, using the Fairchild Planar° epitaxial process. It is intended for a wide range of analog applications where tailoring of frequency characteristics is desireable. The μA201 compensates easily with a single external component. High common mode voltage range and absence of "latch-up" make the μA201 ideal for use as a voltage follower. The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier, and general feedback applications. The μA201 is short-circuit protected and has the same pin configuration as the popular μA741C, μA748C and μA709C. (For other Fairchild Operational Amplifiers, see listing on back page.)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage		±22 V
Internal Power Dissipation (Note 1)		500 mW
Differential Input Voltage		±30 V
Input Voltage (Note 2)		±15 V
Storage Temperature Range	Plastic DIP	−55°C to +125°C
	Metal Can	−65°C to +150°C
Operating Temperature Range		0°C to +70°C
Lead Temperature (Soldering, 60 seconds)	Plastic DIP	260°C
	Metal Can	300°C
Output Short-Circuit Duration (Note 3)		Indefinite

PHYSICAL DIMENSIONS
In accordance with JEDEC (TO-99) outline

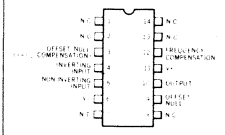


NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.22 gram

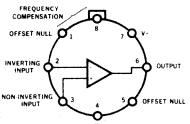
ORDER PART NO. U5B7201393

CONNECTION DIAGRAMS

14 LEAD PLASTIC DIP

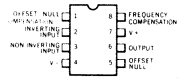


8 LEAD METAL CAN
(TOP VIEW)



NOTE: Pin 4 is connected to case

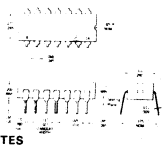
8 LEAD PLASTIC DIP



PHYSICAL DIMENSIONS

In accordance with JEDEC (TO-116) outline

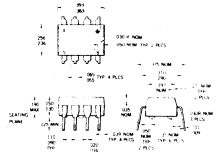
CERAMIC DIP
6A PACKAGE



NOTES
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers.
They are purposely shipped with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for .020 inch diameter lead.
Leads are tin-plated kovar
Package weight is 2.0 grams

ORDER PART NO. U6A7201393

8 LEAD PLASTIC DIP



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for .020 inch diameter lead.
Leads are gold-plated kovar
Package weight is 0.6 gram

ORDER PART NO. U9T7201393

NOTES:
(1) Rating applies for case temperatures to +70°C.
(2) For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
(3) Short circuit may be to ground or either supply. Rating applies to +70°C ambient temperature.

*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR

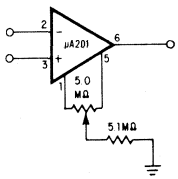
ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $C_C = 30$ pF, $T_A = 25°C$ unless otherwise specified)

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	7.5	mV
Input Offset Current			20	500	nA
Input Bias Current			080	1.5	μA
Input Resistance		0.1	2.0		MΩ
Input Capacitance			1.4		pF
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	20,000	200,000		
Output Resistance			75		Ω
Output Short-Circuit Current			25		mA
Power Consumption			50	85	mW
Transient Response (unity gain)	$V_{in} = 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF				
Risetime			0.3		μs
Overshoot			5.0		%
Slew Rate	$R_L \geq 2$ kΩ		0.5		V/μs
The following specifications apply for $0°C \leq T_A \leq +70°C$:					
Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	10	mV
Input Offset Current	$T_A = 70°C$		50	400	nA
	$T_A = 0°C$		150	750	nA
Input Bias Current			0.03	2.0	μA
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	65	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	300	μV/V
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	15,000			
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		V
Power Consumption			60	100	mW

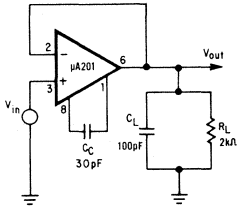
NOTE:
FOR OTHER FAIRCHILD OPERATIONAL AMPLIFIERS, SEE THE FOLLOWING DATA SHEETS:

HIGH SPEED — μA715, μA715C
INSTRUMENTATION — μA725, μA725B, μA725C
TEMPERATURE STABLE PREAMPS — μA727, μA727B
MICROPOWER — μA735, μA735B, μA735C
FET INPUT — μA740, μA740C
FREQUENCY COMPENSATED — μA741, μA741C
DUALS — μA739C, μA749, μA749C, μA747, μA747C
HIGH PERFORMANCE — μA101, μA748, μA748C
PRECISION — μA777, μA777B, μA777C

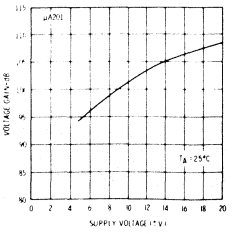
VOLTAGE OFFSET NULL CIRCUIT



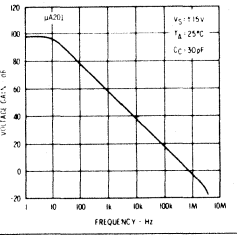
TRANSIENT RESPONSE TEST CIRCUIT



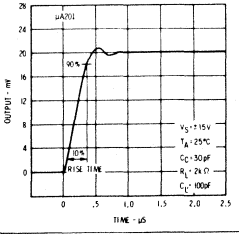
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



TRANSIENT RESPONSE



μA702A
HIGH GAIN, WIDEBAND DC AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

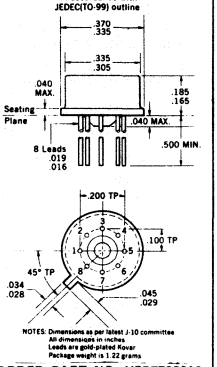
- **IMPROVED SPECIFICATIONS**
- **2 mV MAXIMUM OFFSET VOLTAGE**
- **2500 MINIMUM VOLTAGE GAIN**
- **10 μV/°C MAXIMUM OFFSET VOLTAGE DRIFT**

GENERAL DESCRIPTION — The μA702A is a complete DC amplifier constructed on a single silicon chip, using the Fairchild Planar* epitaxial process. It is intended for use as an operational amplifier in high speed analog computers, as a precision instrumentation amplifier, or in other applications requiring a feedback amplifier useful from DC to 30 MHz.

ABSOLUTE MAXIMUM RATINGS

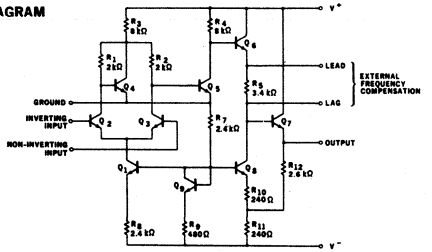
Voltage Between V^+ and V^- Terminals	21 V
Peak Output Current	50 mA
Differential Input Voltage	±5.0 V
Input Voltage	+1.5 Volts to −6.0 V
Internal Power Dissipation	
TO-99 [Note 1]	300 mW
Flat Package [Note 2]	200 mW
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	300°C

PHYSICAL DIMENSIONS
in accordance with JEDEC(TO-99) outline

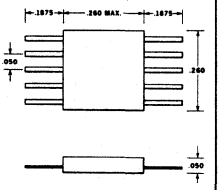


ORDER PART NO. U5B7702312

SCHEMATIC DIAGRAM



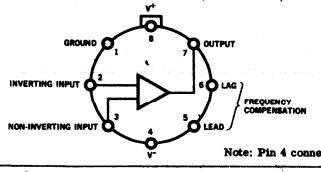
PHYSICAL DIMENSIONS
(TYPICAL FLAT PACKAGE)
(TOP VIEW)



ORDER PART NO. U3F7702312

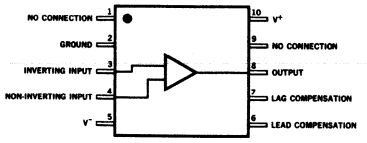
ALSO AVAILABLE IN DIL ORDER PART NO. U6A7702312

TO-99 CONNECTION DIAGRAM (TOP VIEW)



Note: Pin 4 connected to case.

FLAT PACKAGE CONNECTION DIAGRAM (TOP VIEW)



Notes on page 2

* Planar is a patented Fairchild process.

FAIRCHILD SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

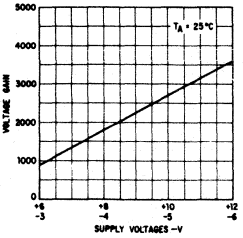
PARAMETER (see definitions)	CONDITIONS	V^+ = 12.0 V, V^- = −6.0 V MIN.	TYP.	MAX.	V^+ = 6.0 V, V^- = −3.0 V MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 2$ kΩ		0.5	2.0		0.7	3.0	mV
Input Offset Current			180	500		120	500	nA
Input Bias Current			2.0	5.0		1.2	3.5	μA
Input Resistance		16	40		22	67		kΩ
Input Voltage Range		−4.0		+0.5	−1.5		+0.5	V
Common Mode Rejection Ratio	$R_S \leq 2$ kΩ, f ≤ 1 kHz	80	100		80	100		dB
Large-Signal Voltage Gain	$R_L \geq 100$ kΩ, $V_{out} = \pm 5.0$ V	2500	3600	6000				
	$R_L \geq 100$ kΩ, $V_{out} = \pm 2.5$ V				600	900	1500	
Output Resistance			200	500		300	700	Ω
Supply Current	$V_{out} = 0$		5.0	6.7		2.1	3.3	mA
Power Consumption	$V_{out} = 0$		90	120		19	30	mW
Transient Response (unity-gain)	$C_L = 0.01$ μF, $R_i = 20$ Ω, $R_L \geq 100$ kΩ, $V_{in} = 10$ mV							
Risetime			25	120				ns
Overshoot	$C_L \leq 100$ pF		10	50				%
Transient Response (×100 gain)	$C_S = 50$ pF, $R_L \geq 100$ kΩ, $V_{in} = 1$ mV							
Risetime			10	30				ns
Overshoot			20	40				%
The following specifications apply for −55°C ≤ T_A ≤ +125°C:								
Input Offset Voltage	$R_S \leq 2$ kΩ			3.0			4.0	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50$ Ω, $T_A = 25$°C to $T_A = +125$°C		2.5	10		3.5	15	μV/°C
	$R_S = 50$ Ω, $T_A = 25$°C to $T_A = -55$°C		2.0	10		3.0	15	μV/°C
Input Offset Current	$T_A = +125$°C		80	500		50	500	nA
	$T_A = -55$°C		400	1500		280	1500	nA
Average Temperature Coefficient of Input Offset Current	$T_A = 25$°C to $T_A = +125$°C		1.0	5.0		0.7	4.0	nA/°C
	$T_A = 25$°C to $T_A = -55$°C		3.0	16		2.0	13	nA/°C
Input Bias Current	$T_A = -55$°C		4.3	10		2.6	7.5	μA
Input Resistance		6.0			8.0			kΩ
Common Mode Rejection Ratio	$R_S \leq 2$ kΩ, f ≤ 1 kHz	70	95		70	95		dB
Supply Voltage Rejection Ratio	$V^+ = 12$ V, $V^- = -6$ V to $V^+ = 6$ V, $V^- = -3$ V, $R_S \leq 2$ kΩ		75	200		75	200	μV/V
Large-Signal Voltage Gain	$R_L \geq 100$ kΩ, $V_{out} = \pm 5.0$ V	2000		7000				
	$R_L \geq 100$ kΩ, $V_{out} = \pm 2.5$ V				500		1750	
Output Voltage Swing	$R_L \geq 100$ kΩ	±5.0	±5.3		±2.5	±2.7		V
	$R_L \geq 10$ kΩ	±3.5	±4.0		±1.5	±2.0		V
Supply Current	$T_A = +125$°C, $V_{out} = 0$		4.4	6.7		1.7	3.3	mA
	$T_A = -55$°C, $V_{out} = 0$		5.0	7.5		2.1	3.9	mA
Power Consumption	$T_A = +125$°C, $V_{out} = 0$		80	120		15	30	mW
	$T_A = -55$°C, $V_{out} = 0$		90	135		19	35	mW

NOTES:

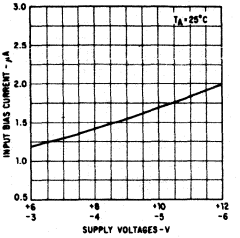
(1) Rating applies for case temperatures to +125°C; derate linearly at 5.6 mW/°C for ambient temperatures above +105°C.
(2) Derate linearly at 4.4 mW/°C for case temperatures above +115°C; derate linearly at 3.3 mW/°C for ambient temperatures above +100°C.

TYPICAL PERFORMANCE CURVES

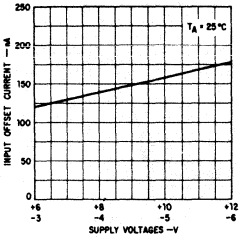
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



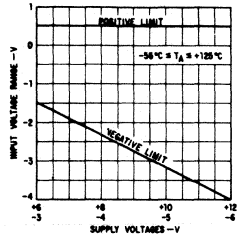
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



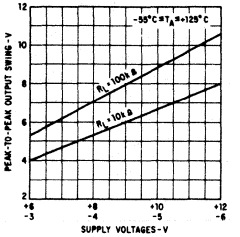
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



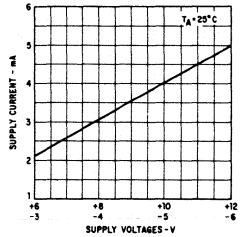
INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGES



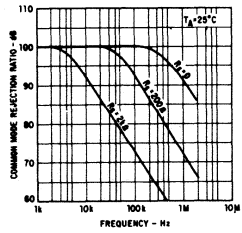
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGES



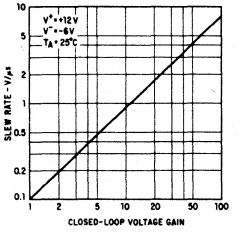
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



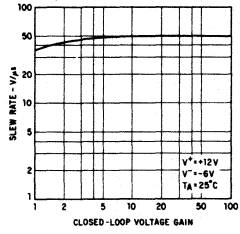
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



SLEW RATE AS A FUNCTION OF CLOSED-LOOP VOLTAGE GAIN (LAG COMPENSATION)

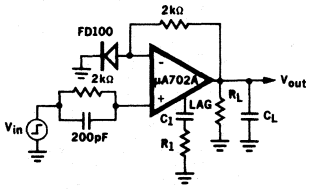


SLEW RATE AS A FUNCTION OF CLOSED-LOOP VOLTAGE GAIN (LEAD-LAG COMPENSATION)

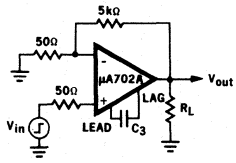


TRANSIENT RESPONSE TEST CIRCUITS

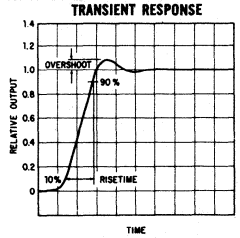
UNITY-GAIN AMPLIFIER (LAG COMPENSATION)



X100 AMPLIFIER (LEAD COMPENSATION)

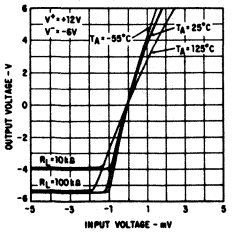


TRANSIENT RESPONSE

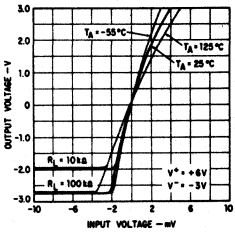


TYPICAL PERFORMANCE CURVES

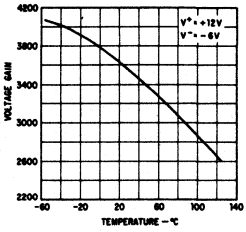
VOLTAGE TRANSFER CHARACTERISTIC



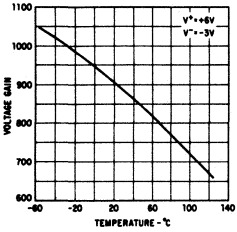
VOLTAGE TRANSFER CHARACTERISTIC



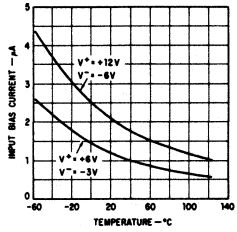
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



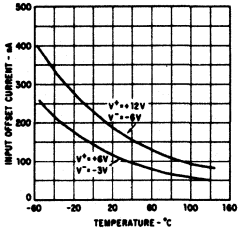
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



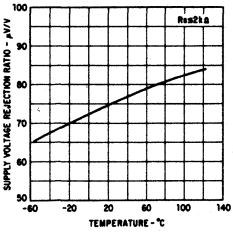
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



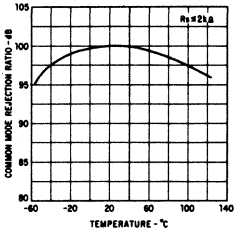
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



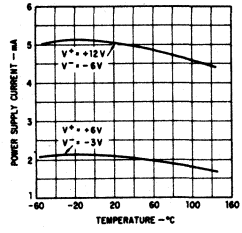
SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



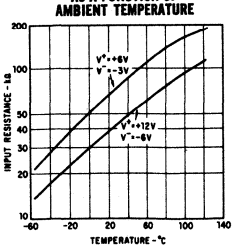
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



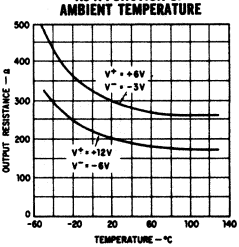
POWER SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



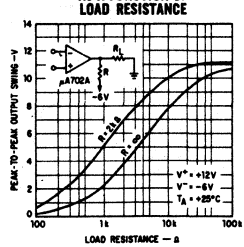
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



OUTPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



DEFINITION OF TERMS

INPUT OFFSET VOLTAGE — That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the output at zero volts.

INPUT RESISTANCE — The resistance looking into either input terminal with the other grounded.

INPUT BIAS CURRENT — The average of the two input currents.

INPUT VOLTAGE RANGE — The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

INPUT COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.

SUPPLY VOLTAGE REJECTION RATIO — The ratio of the change in input offset voltage to the change in supply voltage producing it.

LARGE-SIGNAL VOLTAGE GAIN — The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT VOLTAGE SWING — The peak output swing, referred to zero, that can be obtained without clipping.

OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

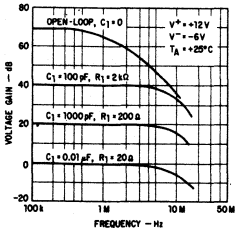
POWER CONSUMPTION — The DC power required to operate the amplifier with the output at zero and with no load current.

TRANSIENT RESPONSE — The closed-loop step-function response of the amplifier under small-signal conditions.

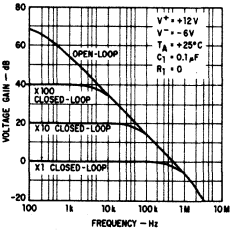
PEAK OUTPUT CURRENT — The maximum current that may flow in the output load without causing damage to the unit.

TYPICAL PERFORMANCE CURVES

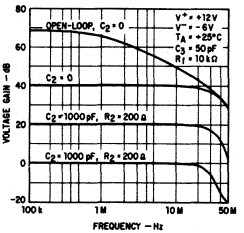
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LAG COMPENSATION)



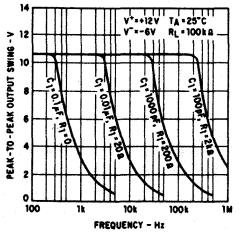
FREQUENCY RESPONSE WITH CONSERVATIVE COMPENSATION NETWORK



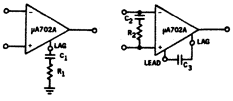
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LEAD-LAG COMPENSATION)



OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS LAG COMPENSATION NETWORKS



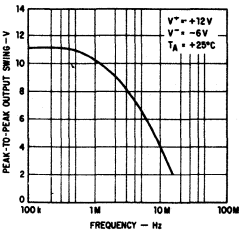
FREQUENCY COMPENSATION CIRCUITS
(Refer to Fairchild APP-117 for further details.)



LAG COMPENSATION

LEAD-LAG COMPENSATION

OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY WITH LEAD-LAG COMPENSATION



μA702B
HIGH GAIN, WIDEBAND DC AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

- **5 mV MAXIMUM OFFSET VOLTAGE**
- **2000 MINIMUM VOLTAGE GAIN**
- **20 μV/°C MAXIMUM OFFSET VOLTAGE DRIFT**

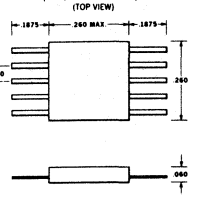
GENERAL DESCRIPTION — The μA702B is a complete DC amplifier constructed on a single silicon chip, using the Fairchild Planar* epitaxial process. It is intended for use as an operational amplifier in miniaturized analog computers, as a precision instrumentation amplifier, or in other applications requiring a feedback amplifier useful from DC to 30 MHz.

For improved specifications, see μA702A data sheet.

ABSOLUTE MAXIMUM RATINGS

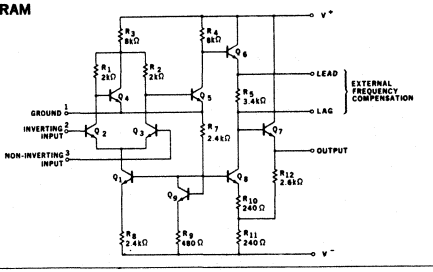
Voltage Between V^+ and V^- Terminals	21 V
Peak Output Current	50 mA
Differential Input Voltage	±5.0 V
Input Voltage	+1.5 V to −6.0 V
Internal Power Dissipation (Note 1)	200 mW
Operating Temperature Range	−55° C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

PHYSICAL DIMENSIONS
(TYPICAL FLAT PACKAGE)
(TOP VIEW)

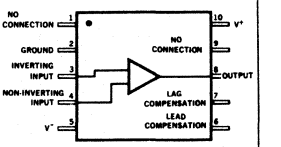


ORDER PART NO.
U3F7702313

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



(TOP VIEW)

NOTE 1: Derate linearly at 4.4 mW/°C for case temperatures above +115°C; derate linearly at 3.3 mW/°C for ambient temperatures above +100°C.

*Planar is a patented Fairchild process.

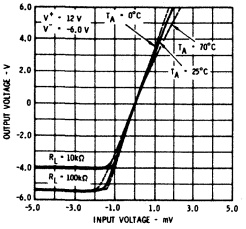
FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

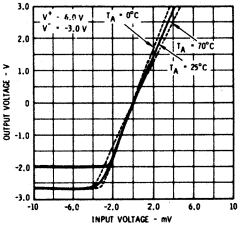
PARAMETER (see definitions)	CONDITIONS	V^+ = 12.0 V, V^- = −6.0 V MIN.	TYP.	MAX.	V^+ = 6.0 V, V^- = −3.0 V MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 2\ k\Omega$		1.5	5.0		1.7	6.0	mV
Input Offset Current			0.5	2.0		0.3	2.0	μA
Input Bias Current			2.5	7.5		1.5	5.0	μA
Input Resistance		10	32		16	55		kΩ
Input Voltage Range		−4.0		+0.5	−1.5		+0.5	V
Common Mode Rejection Ratio	$R_S \leq 2\ k\Omega$, $f \leq 1$ kHz	70	92		70	92		dB
Large-Signal Voltage Gain	$R_L \geq 100\ k\Omega$, $V_{out} = \pm 5.0$ V	2000	3400	6000				
	$R_L \geq 100\ k\Omega$, $V_{out} = \pm 2.5$ V				500	800	1500	
Output Resistance			200	600		300	800	Ω
Supply Current	$V_{out} = 0$		5.0	6.7		2.1	3.3	mA
Power Consumption	$V_{out} = 0$		90	120		19	30	mW
Transient Response (unity gain)	$C_1 = 0.01\ \mu F$, $R_L = 20\Omega$ $R_L \leq 100\ k\Omega$, $V_{in} = 10$ mV							
Risetime			25	120				ns
Overshoot	$C_L \leq 100$ pF		10	50				%
Transient Response (×100 gain)	$C_1 = 50$ pF, $R_L \geq 100\ k\Omega$, $V_{in} = 1$ mV							
Risetime			10	30				ns
Overshoot			20	40				%
The following specifications apply for 0°C ≤ T_A ≤ +70°C:								
Input Offset Voltage	$R_S \leq 2\ k\Omega$			6.5			7.5	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\ \Omega$, $T_A = +70°C$ to $T_A = 0°C$		5.0	20		7.5	25	μV/°C
Input Offset Current				2.5			2.5	μA
Average Temperature Coefficient of Input Offset Current	$T_A = 25°C$ to $T_A = +70°C$		4.0	10		3.0	8.0	nA/°C
	$T_A = 25°C$ to $T_A = 0°C$		6.0	20		5.5	18	nA/°C
Input Bias Current	$T_A = 0°C$		4.0	12		2.7	8	μA
Input Resistance		6.0	18		9.0	27		kΩ
Common Mode Rejection Ratio	$R_S \leq 2\ k\Omega$, $f \leq 1$ kHz	65	86		65	86		dB
Supply Voltage Rejection Ratio	$V^+ = 12$ V, $V^- = 6$ V to $V^+ = 6$ V, $V^- = 3$ V $R_S \leq 2\ k\Omega$		90	300		90	300	μV/V
Large-Signal Voltage Gain	$R_L \geq 100\ k\Omega$, $V_{out} = \pm 5.0$ V	1500		7000				
	$R_L \geq 100\ k\Omega$, $V_{out} = \pm 2.5$ V				400		1750	
The following specifications apply for −55°C ≤ T_A ≤ +125°C:								
Input Offset Voltage	$R_S \leq 2\ k\Omega$			7.5			8.0	mV
Input Offset Current	$T_A = +125°C$		0.2	2.0		0.14	2.0	μA
	$T_A = -55°C$		1.2	4.0		0.8	4.0	μA
Input Bias Current	$T_A = -55°C$		5.5	20		3.4	15	μA
Input Resistance		3.0			4.0			kΩ
Common Mode Rejection Ratio	$R_S \leq 2\ k\Omega$, $f \leq 1$ kHz	60	80		60	80		dB
Large Signal Voltage Gain	$R_L \geq 100\ k\Omega$, $V_{out} = \pm 5.0$ V	1200						
	$R_L \geq 100\ k\Omega$, $V_{out} = \pm 2.5$ V				300			
Output Voltage Swing	$R_L \geq 100\ k\Omega$	±5.0	±5.3		±2.5	±2.7		V
	$R_L \geq 10\ k\Omega$	±3.5	±4.0		±1.5	±2.0		V
Supply Current	$T_A = +125°C$, $V_{out} = 0$		4.4	6.7		1.7	3.3	mA
	$T_A = -55°C$, $V_{out} = 0$		5.0	7.5		2.1	3.9	mA
Power Consumption	$T_A = +125°C$, $V_{out} = 0$		80	120		15	30	mW
	$T_A = -55°C$, $V_{out} = 0$		90	135		19	35	mW

TYPICAL PERFORMANCE CURVES

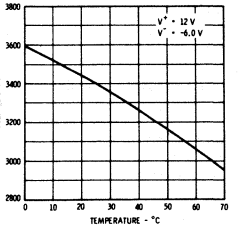
VOLTAGE TRANSFER CHARACTERISTIC



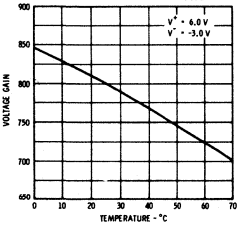
VOLTAGE TRANSFER CHARACTERISTIC



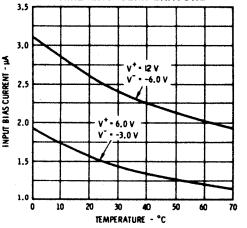
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



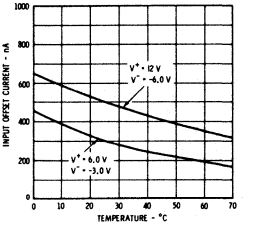
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



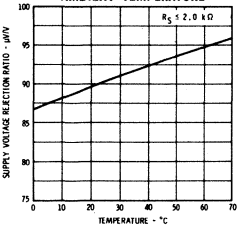
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



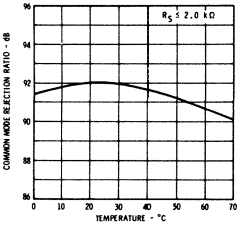
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



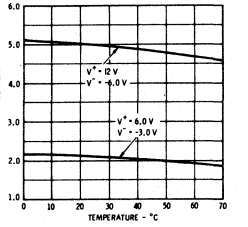
SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



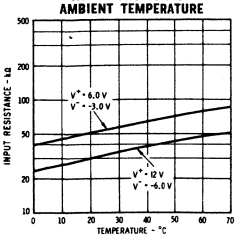
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



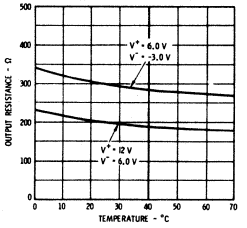
POWER SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



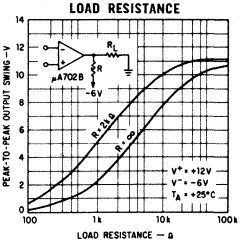
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



OUTPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

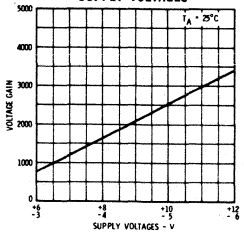


OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

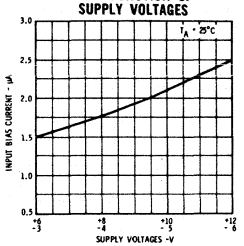


TYPICAL PERFORMANCE CURVES

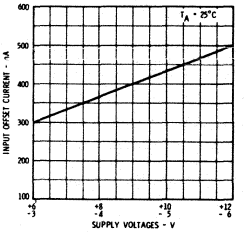
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



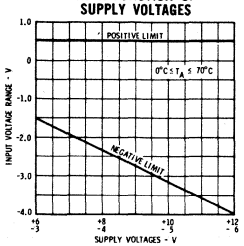
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



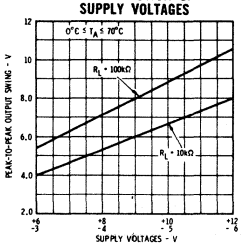
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



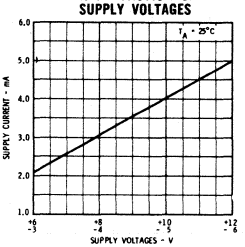
INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGES



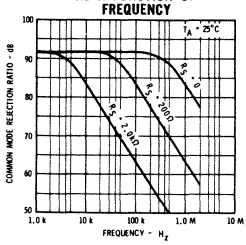
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGES



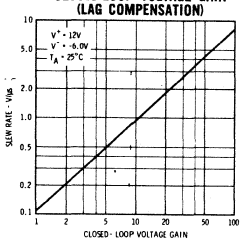
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



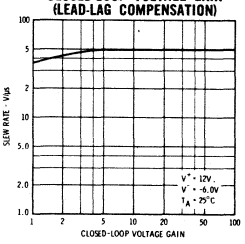
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



SLEW RATE AS A FUNCTION OF CLOSED-LOOP VOLTAGE GAIN (LAG COMPENSATION)

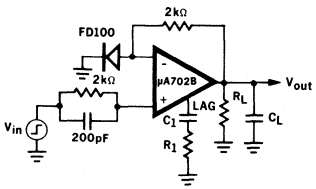


SLEW RATE AS A FUNCTION OF CLOSED-LOOP VOLTAGE GAIN (LEAD-LAG COMPENSATION)

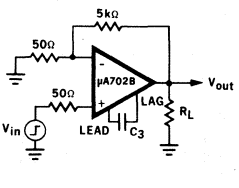


TRANSIENT RESPONSE TEST CIRCUITS

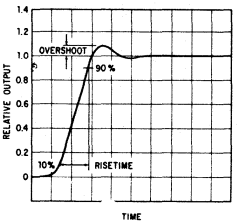
UNITY-GAIN AMPLIFIER (LAG COMPENSATION)



X100 AMPLIFIER (LEAD COMPENSATION)



TRANSIENT RESPONSE



DEFINITION OF TERMS

INPUT OFFSET VOLTAGE — That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the output at zero volts.

INPUT RESISTANCE — The resistance looking into either input terminal with the other grounded.

INPUT BIAS CURRENT — The average of the two input currents.

INPUT VOLTAGE RANGE — The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

INPUT COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.

SUPPLY VOLTAGE REJECTION RATIO — The ratio of the change in input offset voltage to the change in supply voltage producing it.

LARGE-SIGNAL VOLTAGE GAIN — The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT VOLTAGE SWING — The peak output swing, referred to zero, that can be obtained without clipping.

OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

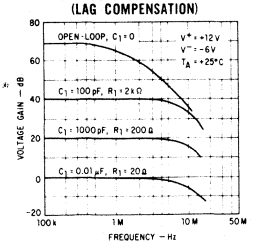
POWER CONSUMPTION — The DC power required to operate the amplifier with the output at zero and with no load current.

TRANSIENT RESPONSE — The closed-loop step-function response of the amplifier under small-signal conditions.

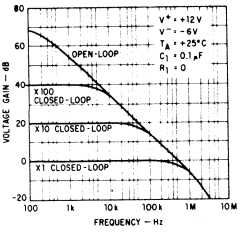
PEAK OUTPUT CURRENT — The maximum current that may flow in the output load without causing damage to the unit.

TYPICAL PERFORMANCE CURVES

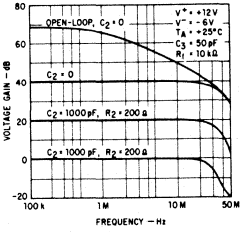
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LAG COMPENSATION)



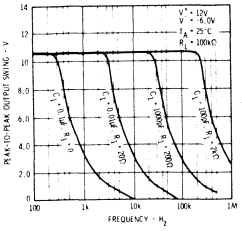
FREQUENCY RESPONSE WITH CONSERVATIVE COMPENSATION NETWORK



FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LEAD-LAG COMPENSATION)

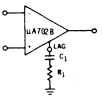


OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS LAG COMPENSATION NETWORKS

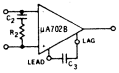


FREQUENCY COMPENSATION CIRCUITS

(Refer to Fairchild APP-117 for further details)

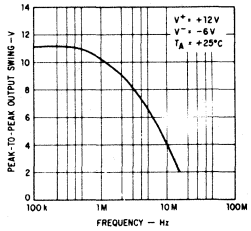


LAG COMPENSATION



LEAD-LAG COMPENSATION

OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY WITH LEAD-LAG COMPENSATION



μA702C
HIGH GAIN, WIDEBAND DC AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

- **IMPROVED SPECIFICATIONS**
- **5 mV MAXIMUM OFFSET VOLTAGE**
- **2000 MINIMUM VOLTAGE GAIN**
- **20 μV/°C MAXIMUM OFFSET VOLTAGE DRIFT**

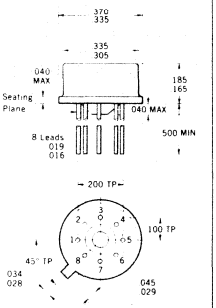
GENERAL DESCRIPTION — The μA702C is a complete DC amplifier constructed on a single silicon chip, using the Fairchild Planar* epitaxial process. It is intended for use as an operational amplifier in miniaturized analog computers, as a precision instrumentation amplifier, or in other applications requiring a feedback amplifier useful from DC to 30 MHz.

For full temperature range operation (−55°C to +125°C) see μA702A data sheet.

ABSOLUTE MAXIMUM RATINGS

Voltage Between V⁺ and V⁻ Terminals	21 V
Peak Output Current	50 mA
Differential Input Voltage	±5.0 V
Input Voltage	+1.5 V to −6.0 V
Internal Power Dissipation (Note 1)	
TO-99	300 mW
Flat Package	200 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

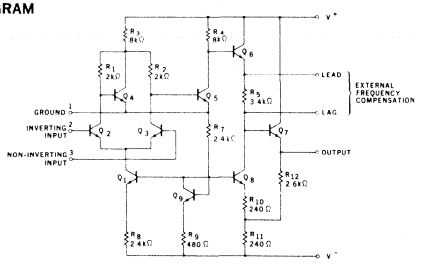
PHYSICAL DIMENSIONS
in accordance with
JEDEC(TO 99) outline



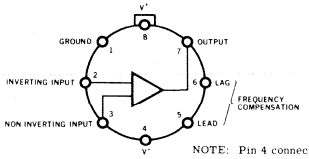
NOTES: Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold plated Kovar
Package weight is 1.22 grams

ORDER PART NO. U5B7702393

SCHEMATIC DIAGRAM



TO-99 CONNECTION DIAGRAM (TOP VIEW)



NOTE: Pin 4 connected to can.

ALSO AVAILABLE IN DIL ORDER PART NO. U6A7702393

NOTE 1: Rating applies for ambient temperatures to +70°C.

*Planar is a patented Fairchild process.

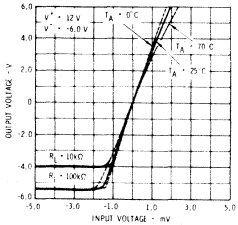
FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

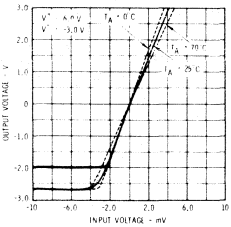
PARAMETER (see definitions)	CONDITIONS	V^+ = 12.0 V, V^- = −6.0 V MIN.	TYP.	MAX.	V^+ = 6.0 V, V^- = −3.0 V MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 2$ kΩ		1.5	5.0		1.7	6.0	mV
Input Offset Current			0.5	2.0		0.3	2.0	μA
Input Bias Current			2.5	7.5		1.5	5.0	μA
Input Resistance		10	32		16	55		kΩ
Input Voltage Range		−4.0		+0.5	−1.5		+0.5	V
Common Mode Rejection Ratio	$R_S \leq 2$ kΩ, $f \leq 1$ kHz	70	92		70	92		dB
Large-Signal Voltage Gain	$R_L \geq 100$ kΩ, $V_{out} = \pm 5.0$ V	2000	3400	6000				
	$R_L \geq 100$ kΩ, $V_{out} = \pm 2.5$ V				500	800	1500	
Output Resistance			200	600		300	800	Ω
Supply Current	$V_{out} = 0$		5.0	6.7		2.1	3.3	mA
Power Consumption	$V_{out} = 0$		90	120		19	30	mW
Transient Response (unity gain)	$C_1 = 0.01$ μF, $R_1 = 20$Ω $R_L \leq 100$ kΩ, $V_{in} = 10$ mV							
Risetime			25	120				ns
Overshoot	$C_L \leq 100$ pF		10	50				%
Transient Response (×100 gain)	$C_1 = 50$ pF, $R_L \geq 100$ kΩ, $V_{in} = 1$ mV							
Risetime			10	30				ns
Overshoot			20	40				%
The following specifications apply for 0°C ≤ T_A ≤ +70°C:								
Input Offset Voltage	$R_S \leq 2$ kΩ			6.5			7.5	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50$ Ω, $T_A = +70$°C to $T_A = 0$°C		5.0	20		7.5	25	μV/°C
Input Offset Current				2.5			2.5	μA
Average Temperature Coefficient of Input Offset Current	$T_A = 25$°C to $T_A = +70$°C		4.0	10		3.0	8.0	nA/°C
	$T_A = 25$°C to $T_A = 0$°C		6.0	20		5.5	18	nA/°C
Input Bias Current	$T_A = 0$°C		4.0	12		2.7	8	μA
Input Resistance		6.0	18		9.0	27		kΩ
Common Mode Rejection Ratio	$R_S \leq 2$ kΩ, $f \leq 1$ kHz	65	86		65	86		dB
Supply Voltage Rejection Ratio	$V^+ = 12$ V, $V^- = 6$ V to $V^+ = 6$ V, $V^- = 3$ V $R_S \leq 2$ kΩ		90	300		90	300	μV/V
Large-Signal Voltage Gain	$R_L \geq 100$ kΩ, $V_{out} = \pm 5.0$ V	1500		7000				
	$R_L \geq 100$ kΩ, $V_{out} = \pm 2.5$ V				400		1750	
Output Voltage Swing	$R_L \geq 100$ kΩ	±5.0	±5.3		±2.5	±2.7		V
	$R_L \geq 10$ kΩ	±3.5	±4.0		±1.5	±2.0		V
Supply Current	$V_{out} = 0$		5.0	7.0		2.1	3.9	mA
Power Consumption	$V_{out} = 0$		90	125		19	35	mW

TYPICAL PERFORMANCE CURVES

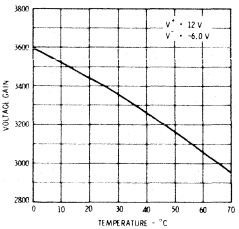
VOLTAGE TRANSFER CHARACTERISTIC



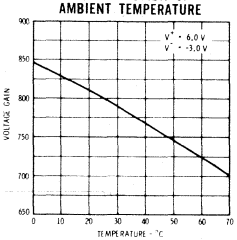
VOLTAGE TRANSFER CHARACTERISTIC



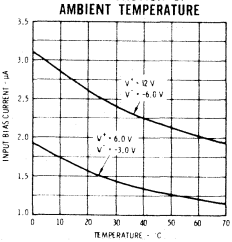
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



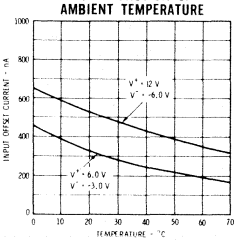
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



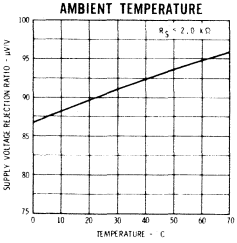
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



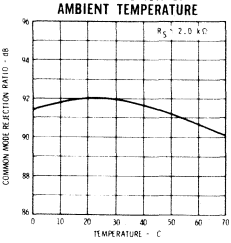
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



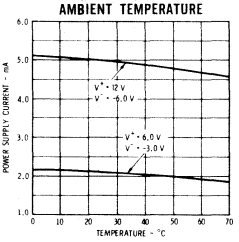
SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



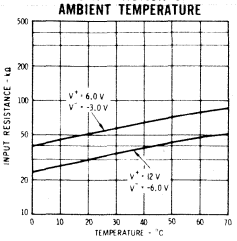
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



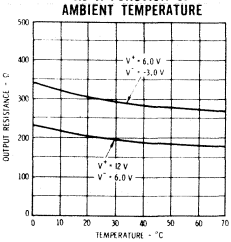
POWER SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



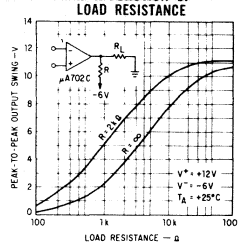
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



OUTPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

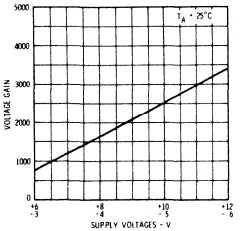


OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

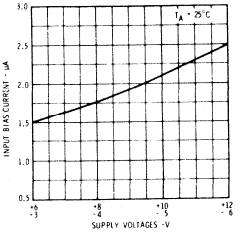


TYPICAL PERFORMANCE CURVES

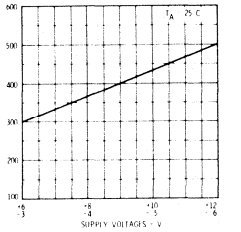
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



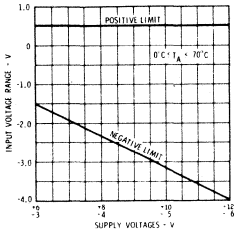
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



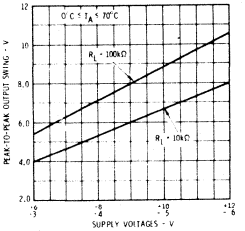
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



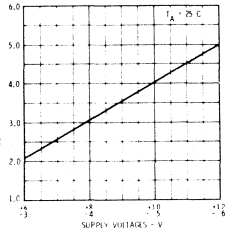
INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGES



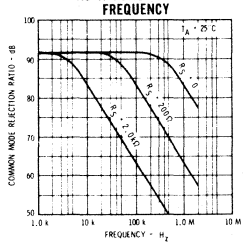
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGES



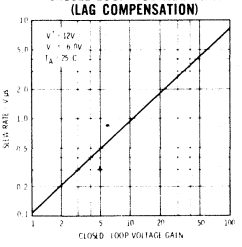
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



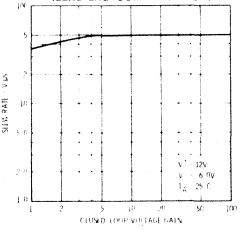
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



SLEW RATE AS A FUNCTION OF CLOSED-LOOP VOLTAGE GAIN (LAG COMPENSATION)

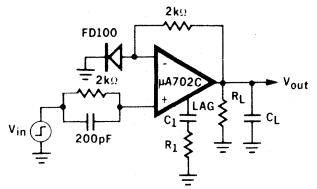


SLEW RATE AS A FUNCTION OF CLOSED-LOOP VOLTAGE GAIN (LEAD-LAG COMPENSATION)

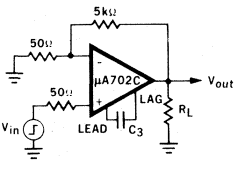


TRANSIENT RESPONSE TEST CIRCUITS

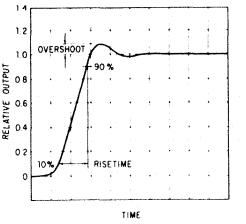
UNITY-GAIN AMPLIFIER (LAG COMPENSATION)



X100 AMPLIFIER (LEAD COMPENSATION)



TRANSIENT RESPONSE



DEFINITION OF TERMS

INPUT OFFSET VOLTAGE — That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the output at zero volts.

INPUT RESISTANCE — The resistance looking into either input terminal with the other grounded.

INPUT BIAS CURRENT — The average of the two input currents.

INPUT VOLTAGE RANGE — The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

INPUT COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.

SUPPLY VOLTAGE REJECTION RATIO — The ratio of the change in input offset voltage to the change in supply voltage producing it.

LARGE-SIGNAL VOLTAGE GAIN — The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT VOLTAGE SWING — The peak output swing, referred to zero, that can be obtained without clipping.

OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

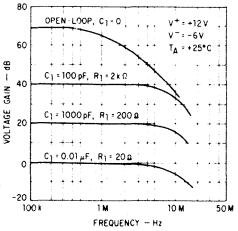
POWER CONSUMPTION — The DC power required to operate the amplifier with the output at zero and with no load current.

TRANSIENT RESPONSE — The closed-loop step-function response of the amplifier under small-signal conditions.

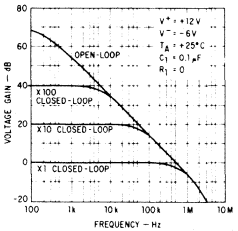
PEAK OUTPUT CURRENT — The maximum current that may flow in the output load without causing damage to the unit.

TYPICAL PERFORMANCE CURVES

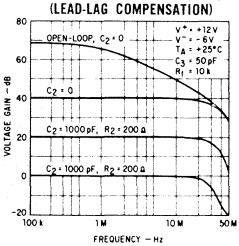
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LAG COMPENSATION)



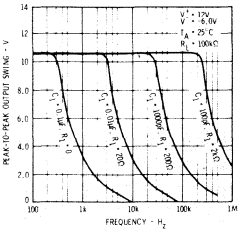
FREQUENCY RESPONSE WITH CONSERVATIVE COMPENSATION NETWORK



FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LEAD-LAG COMPENSATION)

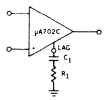


OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS LAG COMPENSATION NETWORKS

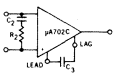


FREQUENCY COMPENSATION CIRCUITS

(Refer to Fairchild APP-117 for further details)

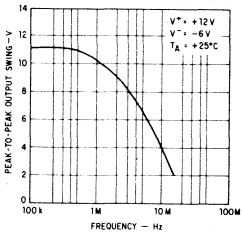


LAG COMPENSATION



LEAD-LAG COMPENSATION

OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY WITH LEAD-LAG COMPENSATION



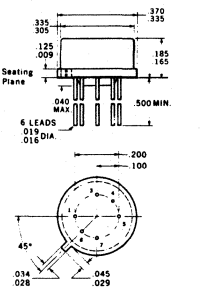
μA703
RF-IF AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION - The μA703 is an RF-IF amplifier constructed on a single silicon chip and is intended for use as a limiting or nonlimiting amplifier, harmonic mixer, or oscillator to 150 MHz. The low internal feedback of the device insures a higher stability-limited gain than that available from conventional circuitry. Including the biasing network in the same package reduces the number of external components required, thereby increasing the reliability and versatility of the device.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	20 V
Output Collector Voltage	24 V
Voltage Between Input Terminals	± 5.0 V
Internal Power Dissipation (Note 1)	200 mW
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering - 60 seconds)	300°C

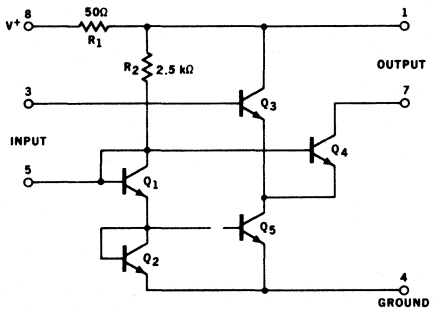
PHYSICAL DIMENSIONS
(in accordance with JEDEC TO-99 outline)



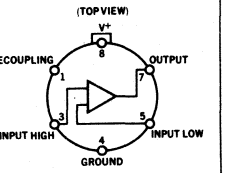
NOTES: All dimensions in inches.
Leads are gold-plated kovar.
Package weight ≈ 1.27 grams

ORDER PART NO. U5D7703312

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



NOTE: Pin 4 connected to case.

NOTE 1: Rating applies for ambient temperatures to 125°C.

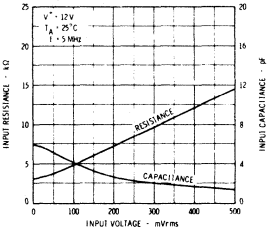
FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V^+ = 12 V unless otherwise specified)

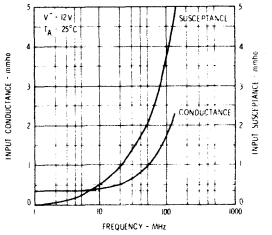
Parameter	Conditions	Min.	Typ.	Max.	Units
Power Consumption	e_{in} = 0		110	170	mW
Quiescent Output Current	e_{in} = 0	2.1	2.5	3.1	mA
Peak-to-Peak Output Current	e_{in} = 400 mV rms, f = 1 kHz	4.0			mA
Output Saturation Voltage				1.7	V
Forward Transadmittance	e_{in} = 10 mV rms, f $\leq$ 5 MHz	29	35		mmho
Input Conductance	e_{in} < 10 mV rms, f $\leq$ 5 MHz		0.30	0.43	mmho
Input Capacitance	e_{in} < 10 mV rms, f $\leq$ 5 MHz		7.0	9.0	pF
Output Capacitance	f $\leq$ 5 MHz		2.0	3.0	pF
Output Conductance	f $\leq$ 5 MHz		0.02	0.04	mmho
Noise Figure	f = 30 MHz, R_S = 500 Ω		6.5		dB
	f = 100 MHz, R_S = 500 Ω		8.0		dB
The following specifications apply for -55°C $\leq T_A \leq$ +125°C					
Quiescent Output Current	e_{in} = 0	1.7		3.1	mA
Peak-to-Peak Output Current	e_{in} = 400 mV rms, f = 1 kHz	3.2			mA
Output Saturation Voltage				1.8	V
Forward Transadmittance	e_{in} = 10 mV rms, f $\leq$ 5 MHz	21			mmho
Input Conductance	e_{in} < 10 mV rms, f $\leq$ 5 MHz			1.2	mmho
Output Conductance	f $\leq$ 5 MHz			0.05	mmho

TYPICAL PERFORMANCE CURVES

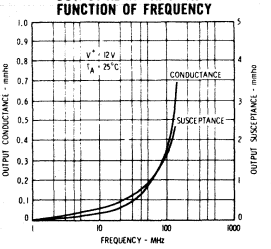
INPUT RESISTANCE AND CAPACITANCE AS A FUNCTION OF INPUT VOLTAGE



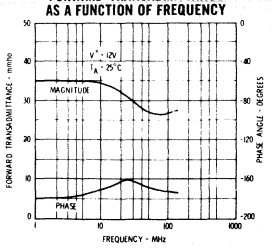
INPUT ADMITTANCE AS A FUNCTION OF FREQUENCY



OUTPUT ADMITTANCE AS A FUNCTION OF FREQUENCY

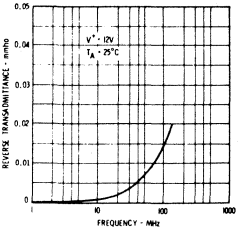


FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY

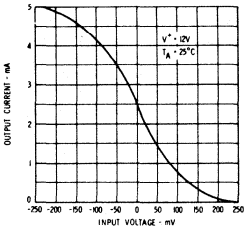


TYPICAL PERFORMANCE CURVES

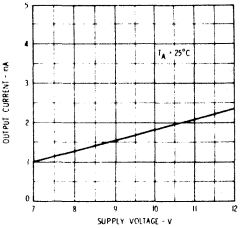
MAXIMUM REVERSE TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



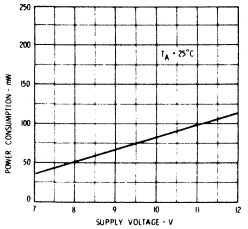
OUTPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE



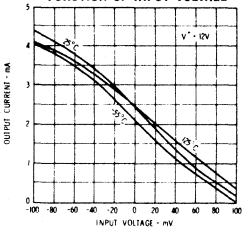
OUTPUT CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



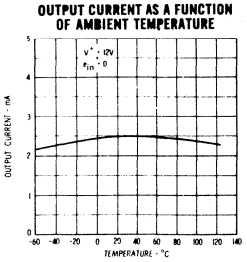
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



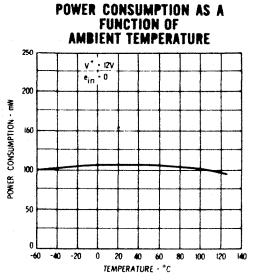
OUTPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE



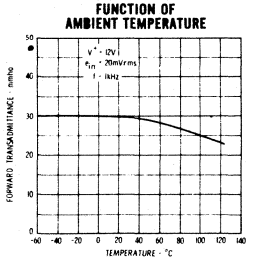
OUTPUT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



TRANSADMITTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



DEFINITION OF TERMS

POWER CONSUMPTION - The DC power required to operate the device with no signal applied.

QUIESCENT OUTPUT CURRENT - The DC current delivered to the load with the input terminals short-circuited.

PEAK-TO-PEAK OUTPUT CURRENT - The short-circuit output current excursion for a large-signal input voltage.

OUTPUT SATURATION VOLTAGE - The minimum voltage to which the output collector may be reduced without degrading circuit performance.

TRANSADMITTANCE - The ratio of the output current to the input voltage.

INPUT ADMITTANCE - The admittance between the input terminals with the output short-circuited.

OUTPUT ADMITTANCE - The admittance between the output terminals with the input short-circuited.

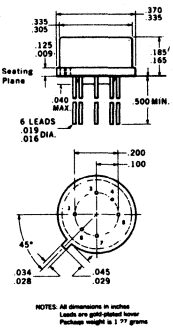
μA703C
RF-IF AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION - The μA703C is an RF-IF amplifier constructed on a single silicon chip and is intended for use as a limiting or non-limiting amplifier, harmonic mixer, or oscillator to 150 MHz. The low internal feedback of the device insures a higher stability-limited gain than that available from conventional circuitry. Including the biasing network in the same package reduces the number of external components required, thereby increasing the reliability and versatility of the device. For full range operation (-55°C to +125°C) see μA703 data sheet.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	20 V
Output Collector Voltage	24 V
Voltage Between Input Terminals	± 5.0 V
Internal Power Dissipation (Note 1)	200 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering - 60 second)	300°C

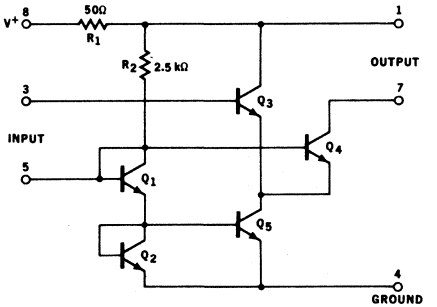
PHYSICAL DIMENSIONS



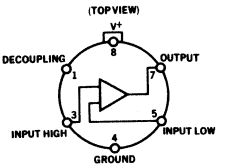
NOTES: All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.77 grams

ORDER PART NO. U5D7703393

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



NOTE: Pin 4 connected to case.

NOTE 1: Rating applies for ambient temperatures to 70°C.

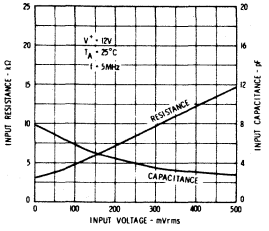
FAIRCHILD SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V^+ = 12 V unless otherwise specified)

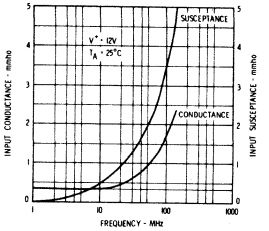
Parameter	Conditions	Min.	Typ.	Max.	Units
Power Consumption	e_{in} = 0		110	170	mW
Quiescent Output Current	e_{in} = 0	1.9	2.5	3.3	mA
Peak-to-Peak Output Current	e_{in} = 400 mV rms, f = 1 kHz	3.6			mA
Output Saturation Voltage				1.7	V
Forward Transadmittance	e_{in} = 10 mV rms, f ≤ 1kHz	23	33		mmho
Input Conductance	e_{in} < 10 mV rms, f ≤ 5 MHz		0.35	0.50	mmho
Input Capacitance	e_{in} < 10 mV rms, f ≤ 5 MHz		9.0	16.0	pF
Output Capacitance	f ≤ 5 MHz		2.0	3.0	pF
Output Conductance	e_o ≤ 100mVrms, f ≤ 5MHz			0.05	mmho
Noise Figure	f = 30 MHz, R_S = 500 Ω		6.5		dB
	f = 100 MHz, R_S = 500 Ω		8.0		dB
The following specifications apply for 0°C ≤ T_A ≤ 70°C:					
Quiescent Output Current	e_{in} = 0	1.7		3.5	mA
Peak-to-Peak Output Current	e_{in} = 400 mV rms, f = 1 kHz	3.2			mA
Output Saturation Voltage				1.8	V
Forward Transadmittance	e_{in} = 10 mV rms f ≤ 1kHz	22			mmho
Input Conductance	e_{in} < 10 mV rms, f ≤ 5 MHz			0.71	mmho
Output Conductance	e_o ≤ 100mVrms, f ≤ 5MHz			0.06	mmho

TYPICAL PERFORMANCE CURVES

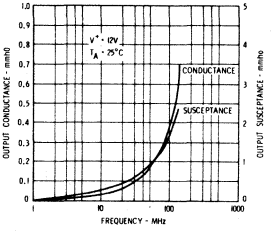
INPUT RESISTANCE AND CAPACITANCE AS A FUNCTION OF INPUT VOLTAGE



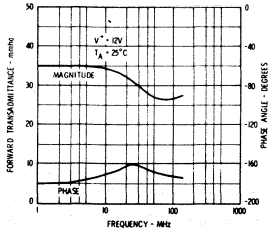
INPUT ADMITTANCE AS A FUNCTION OF FREQUENCY



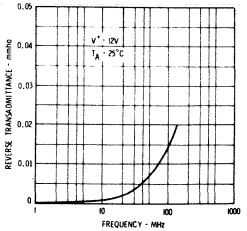
OUTPUT ADMITTANCE AS A FUNCTION OF FREQUENCY



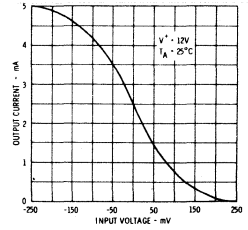
FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



MAXIMUM REVERSE TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



OUTPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE



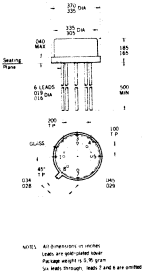
μA703E
RF-IF AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION - The μA703E is a linear integrated circuit with useful unneutralized power gain to frequencies in excess of 100 MHz. It features the capability of nonsaturating limiter operation with a suitable output load, making it ideally suited for FM-IF limiter applications.

Applications include FM-IF limiter-amplifier, TV sound IF amplifier, chroma reference oscillator for color TV, and fixed-gain amplifiers to 100 MHz.

PHYSICAL DIMENSIONS

in accordance with JEDEC (TO-78) outline (50 mil kovar header)

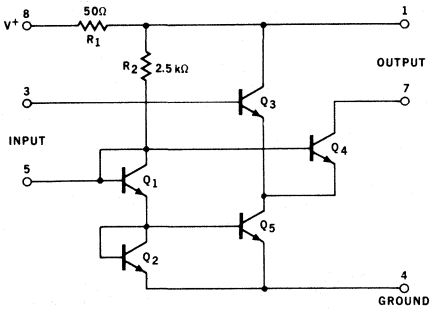


ORDER PART NO. U5Z7703394

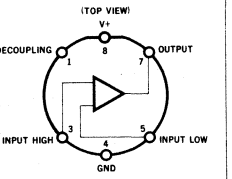
ABSOLUTE MAXIMUM RATINGS

Supply Voltage		20 V
Output Collector Voltage		24 V
Voltage Between Input Terminals		± 5.0 V
Internal Power Dissipation	(Note 1)	200 mW
Operating Temperature Range		0°C to +70°C
Storage Temperature Range		-65°C to +150°C
Lead Temperature (Soldering - 60 seconds)		300°C

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



NOTE 1: Rating applies for ambient temperatures to +70°C.

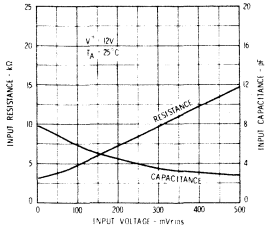
FAIRCHILD SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V^+ = 12 V, f = 10.7 MHz unless otherwise specified)

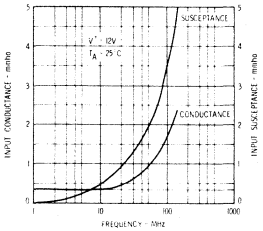
Parameter	Conditions	Min.	Typ.	Max.	Units
Power Consumption	e_{in} = 0		110	170	mW
Quiescent Output Current			2.5	3.3	mA
Peak-to-Peak Output Current	e_{in} = 400 mV rms	3.0	5.0		mA
Output Saturation Voltage			1.4	1.7	Volts
Forward Transadmittance	e_{in} = 10 mV rms	24	35		mmhos
Reverse Transadmittance			0.002		mmho
Input Conductance	e_{in} < 10 mV rms		.33	1.0	mmho
Input Capacitance	e_{in} < 10 mV rms		9.0	12.5	pF
Output Conductance			0.03	0.05	mmho
Output Capacitance			2.6	4.0	pF
Noise Figure	R_S = 500 Ω		6.0		dB
	R_S = 500 Ω, f = 100 MHz		8.0		dB
Maximum Stable Gain			40		dB

TYPICAL PERFORMANCE CURVES

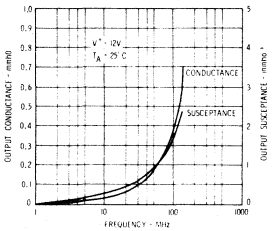
INPUT RESISTANCE AND CAPACITANCE AS A FUNCTION OF INPUT VOLTAGE



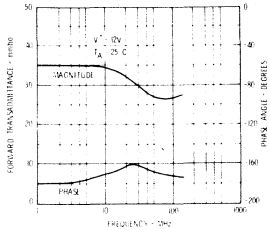
INPUT ADMITTANCE AS A FUNCTION OF FREQUENCY



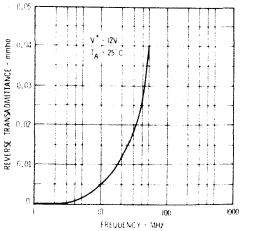
OUTPUT ADMITTANCE AS A FUNCTION OF FREQUENCY



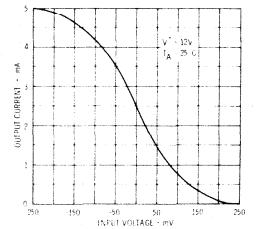
FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



MAXIMUM REVERSE TRANSADMITTANCE AS A FUNCTION OF FREQUENCY

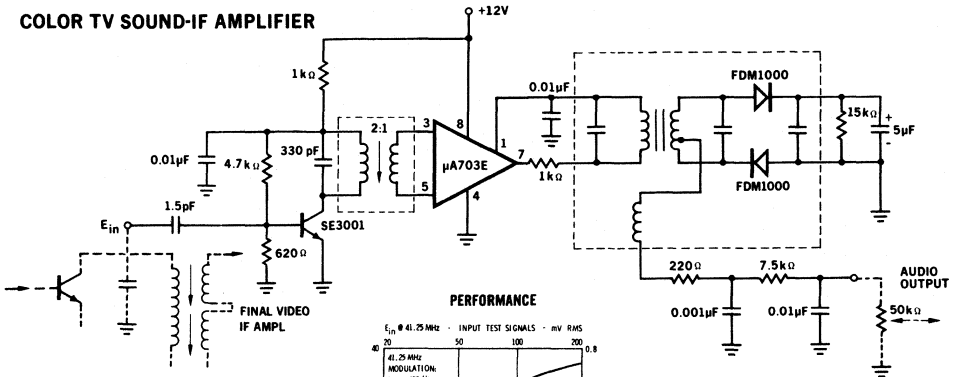


OUTPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE

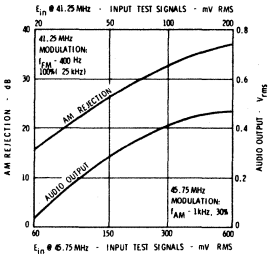


TYPICAL CIRCUIT APPLICATIONS

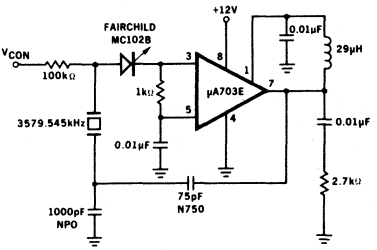
COLOR TV SOUND-IF AMPLIFIER



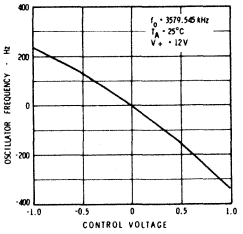
PERFORMANCE



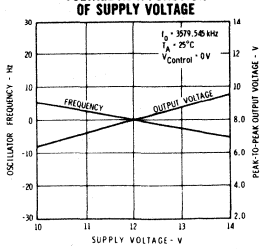
3.58-MHz VOLTAGE-CONTROLLED OSCILLATOR



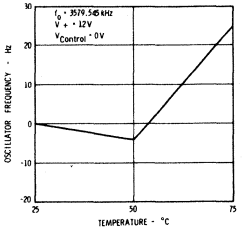
NORMALIZED OSCILLATOR FREQUENCY AS A FUNCTION OF CONTROL VOLTAGE



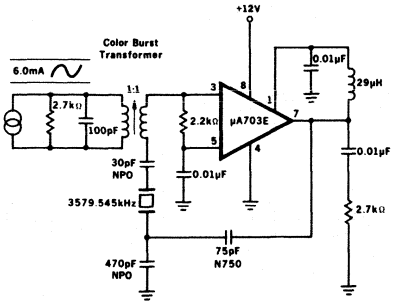
NORMALIZED OSCILLATOR FREQUENCY AND OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE

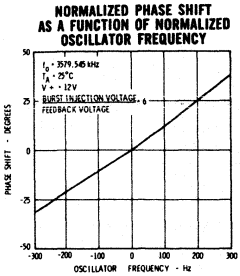


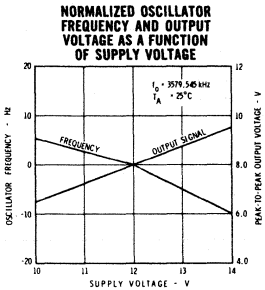
NORMALIZED OSCILLATOR FREQUENCY AS A FUNCTION OF AMBIENT TEMPERATURE

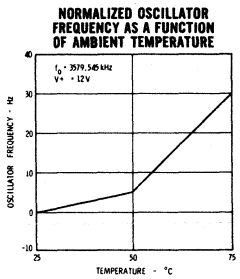


3.58-MHz INJECTION-LOCKED OSCILLATOR

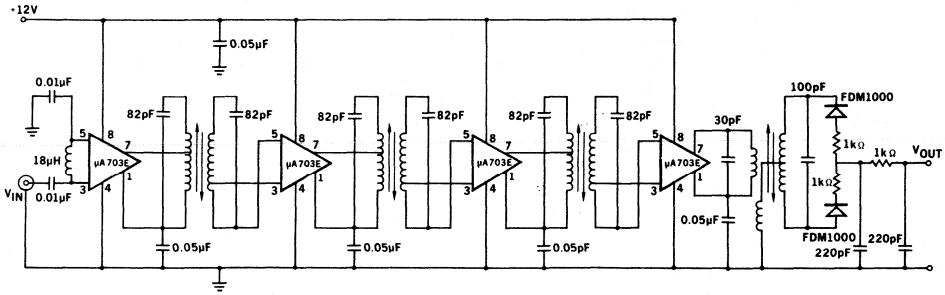








FOUR-STAGE FM-IF AMPLIFIER



Full limiting with $V_{in} < 50\mu V$.
Current consumption 27 mA.
Power gain / stage 26.5 dB.

Peak-to-Peak separation of detector 800 kHz.
THD < 0.8% with ±75 kHz deviation @ 400 Hz.

μA709A

HIGH PERFORMANCE OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

- **2 mV MAXIMUM OFFSET VOLTAGE**
- **50 nA MAXIMUM OFFSET CURRENT**
- **GUARANTEED DRIFT CHARACTERISTICS**

GENERAL DESCRIPTION — The μA709A is a high-gain operational amplifier constructed on a single silicon chip using the Fairchild Planar* epitaxial process. It features low offset, high input impedance, large input common mode range, high output swing under load, and low power consumption. The device displays exceptional temperature stability and will operate over a 14-36 V range of total supply voltage with little degradation of performance. The amplifier is intended for use in DC servo systems, high impedance analog computers, low-level instrumentation applications, and for the generation of special linear and nonlinear transfer functions. Although it features improved performance, the μA709A is a direct plug-in replacement for the μA709 operational amplifier.

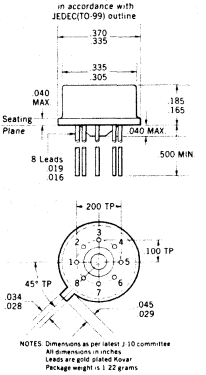
ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage	36 V
Internal Power Dissipation (Note 1)	300 mW
Differential Input Voltage	±5.0 V
Input Voltage	±10 V
Output Short-Circuit Duration ($T_A = +25°C$)	5 sec
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 60 sec)	300°C

NOTES:
(1) Rating applies for case temperatures to +125°C; derate linearly at 5.6 mW/°C for ambient temperatures above +95°C.

PHYSICAL DIMENSIONS

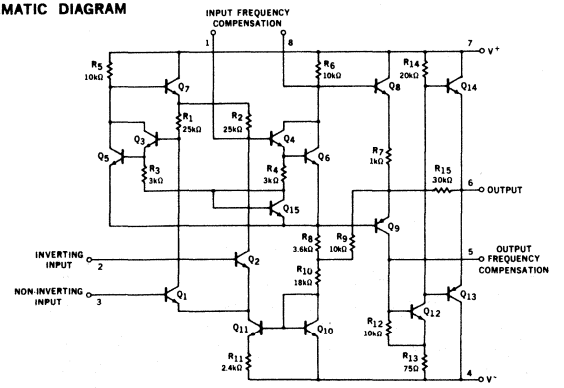
in accordance with JEDEC(TO-99) outline



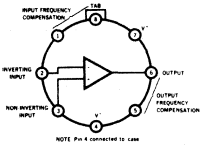
NOTES: Dimensions as per latest JEDEC committee
All dimensions in inches
Leads are gold plated Kovar
Package weight is 1.22 grams

† **ORDER PART NO. U5B7709311**

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



(Top View)

† This device is also available in the Flat Package. Order Part Number U3A7709311.

*Planar is a patented Fairchild process.

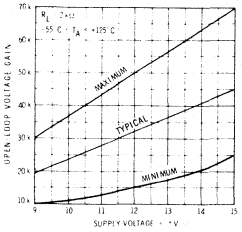
FAIRCHILD SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS ($T_A = +25°C$, $\pm 9\ V \leq V_S \leq \pm 15\ V$ unless otherwise specified)

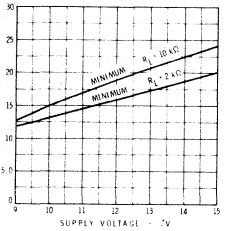
PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10\ k\Omega$		0.6	2.0	mV
Input Offset Current			10	50	nA
Input Bias Current			100	200	nA
Input Resistance		350	700		kΩ
Output Resistance			150		Ω
Supply Current	$V_S = \pm 15\ V$		2.5	3.6	mA
Power Consumption	$V_S = \pm 15\ V$		75	108	mW
Transient Response	$V_S = \pm 15\ V$, $V_{in} = 20\ mV$, $R_L = 2\ k\Omega$, $C_L = 5\ nF$, $R_1 = 1.5\ k\Omega$, $C_2 = 200\ pF$, $R_2 = 50\ \Omega$				
Risetime				1.5	μs
Overshoot	$C_L \leq 100\ pF$			30	%
The following specifications apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage	$R_S \leq 10\ k\Omega$			3.0	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\ \Omega$, $T_A = +25°C$ to $T_A = +125°C$		1.8	10	μV/°C
	$R_S = 50\ \Omega$, $T_A = +25°C$ to $T_A = -55°C$		1.8	10	μV/°C
	$R_S = 10\ k\Omega$, $T_A = +25°C$ to $T_A = +125°C$		2.0	15	μV/°C
	$R_S = 10\ k\Omega$, $T_A = +25°C$ to $T_A = -55°C$		4.8	25	μV/°C
Input Offset Current	$T_A = +125°C$		3.5	50	nA
	$T_A = -55°C$		40	250	nA
Average Temperature Coefficient of Input Offset Current	$T_A = +25°C$ to $T_A = +125°C$		0.08	0.5	nA/°C
	$T_A = +25°C$ to $T_A = -55°C$		0.45	2.8	nA/°C
Input Bias Current	$T_A = -55°C$		300	600	nA
Input Resistance	$T_A = -55°C$	85	170		kΩ
Input Voltage Range	$V_S = \pm 15\ V$	±8.0			V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	80	110		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$		40	100	μV/ V
Large-Signal Voltage Gain	$V_S = \pm 15\ V$, $R_L \geq 2\ k\Omega$, $V_{O-P} = \pm 15\ V$	25,000		70,000	
Output Voltage Swing	$V_S = \pm 15\ V$, $R_L \geq 10\ k\Omega$	±12	±14		V
	$V_S = \pm 15\ V$, $R_L \geq 2\ k\Omega$	±10	±13		V
Supply Current	$T_A = +125°C$, $V_S = \pm 15\ V$		2.1	3.0	mA
	$T_A = -55°C$, $V_S = \pm 15\ V$		2.7	4.5	mA
Power Consumption	$T_A = +125°C$, $V_S = \pm 15\ V$		63	90	mW
	$T_A = -55°C$, $V_S = \pm 15\ V$		81	135	mW

GUARANTEED ELECTRICAL CHARACTERISTICS

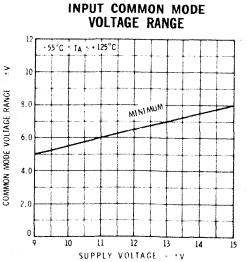
VOLTAGE GAIN



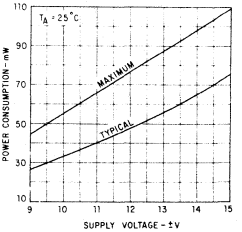
OUTPUT VOLTAGE SWING



INPUT COMMON MODE VOLTAGE RANGE

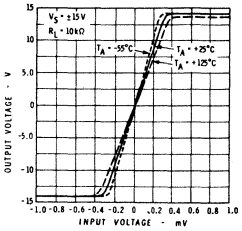


POWER CONSUMPTION

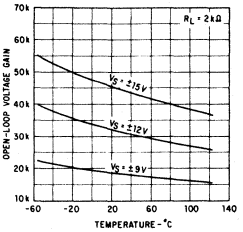


TYPICAL PERFORMANCE CURVES

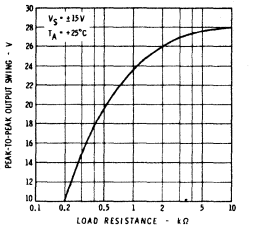
VOLTAGE TRANSFER CHARACTERISTIC



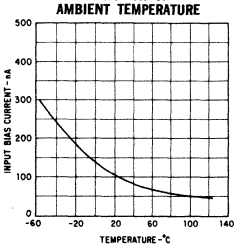
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



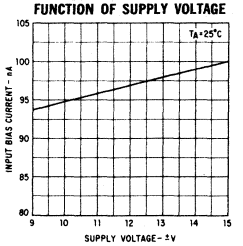
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



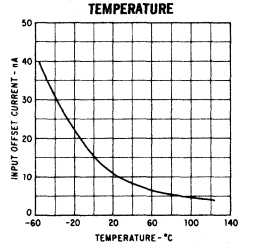
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



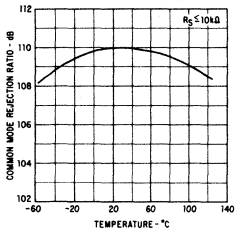
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



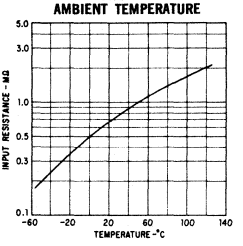
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



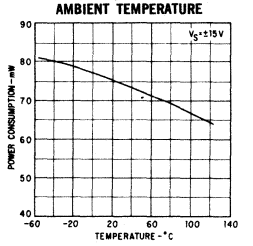
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



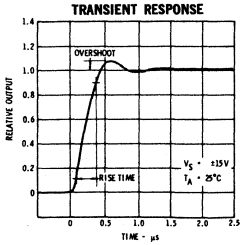
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



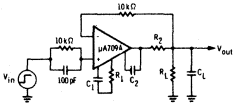
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



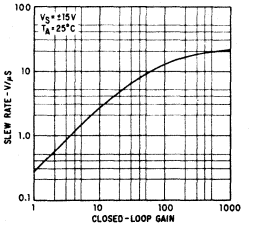
TRANSIENT RESPONSE



TRANSIENT RESPONSE TEST CIRCUIT



SLEW RATE AS A FUNCTION OF CLOSED-LOOP GAIN USING RECOMMENDED COMPENSATION NETWORKS



DEFINITION OF TERMS

INPUT OFFSET VOLTAGE — That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the output at zero volts.

INPUT RESISTANCE — The resistance looking into either input terminal with the other grounded.

INPUT BIAS CURRENT — The average of the two input currents.

INPUT VOLTAGE RANGE — The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

INPUT COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.

SUPPLY VOLTAGE REJECTION RATIO — The ratio of the change in input offset voltage to the change in supply voltage producing it.

LARGE-SIGNAL VOLTAGE GAIN — The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT VOLTAGE SWING — The peak output swing, referred to zero, that can be obtained without clipping.

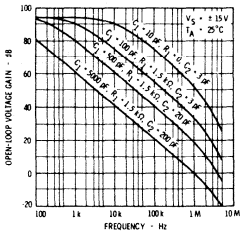
OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

POWER CONSUMPTION — The DC power required to operate the amplifier with the output at zero and with no load current.

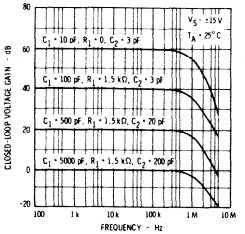
TRANSIENT RESPONSE — The closed-loop step-function response of the amplifier under small-signal conditions.

TYPICAL PERFORMANCE CURVES

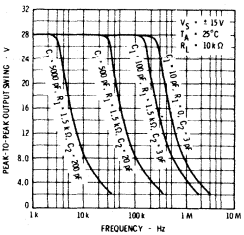
OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF COMPENSATION



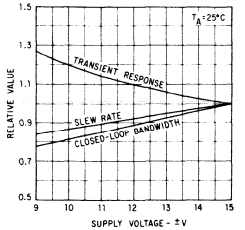
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS



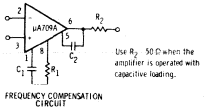
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS COMPENSATION NETWORKS



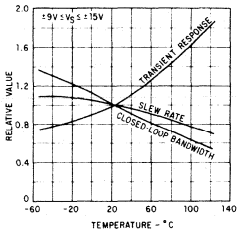
FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE



FREQUENCY COMPENSATION CIRCUIT



FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



μA709

HIGH PERFORMANCE OPERATIONAL AMPLIFIER

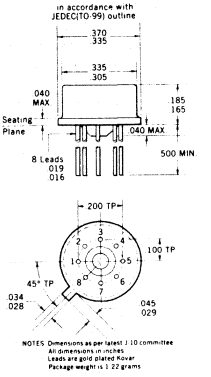
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTIONS - The μA709 is a high-gain operational amplifier constructed on a single silicon chip using the Fairchild Planar epitaxial process. It features low offset, high input impedance, large input common mode range, high output swing under load and low power consumption. The device displays exceptional temperature stability and will operate over a wide range of supply voltages with little degradation of performance. The amplifier is intended for use in DC servo systems, high impedance analog computers, in low-level instrumentation applications and for the generation of special linear and nonlinear transfer functions.

ABSOLUTE MAXIMUM RATINGS

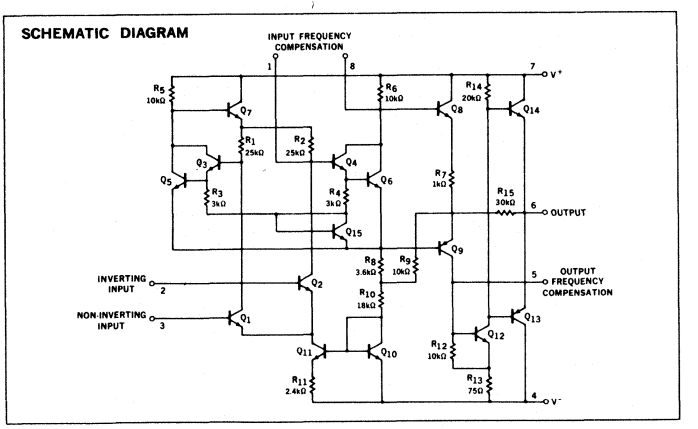
Supply Voltage		± 18 V
Internal Power Dissipation	(Note 1)	300 mW
Differential Input Voltage		± 5.0 V
Input Voltage		± 10 V
Output Short-Circuit Duration	(T_A = 25°C)	5 sec
Storage Temperature Range		-65°C to + 150°C
Operating Temperature Range		-55°C to + 125°C
Lead Temperature (Soldering, 60 sec)		300°C

PHYSICAL DIMENSIONS

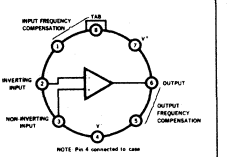


ORDER PART NO.
U5B7709312

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



(Top View)

NOTE 1: Rating applies for case temperatures to + 125°C; derate linearly at 5.6 mW/°C for ambient temperatures above + 95°C.

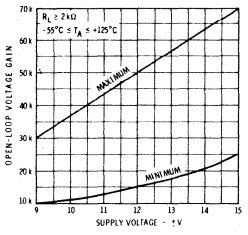
FAIRCHILD SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS (T_A = +25°C, ±9 V ≤ V_S ≤ ±15 V unless otherwise specified)

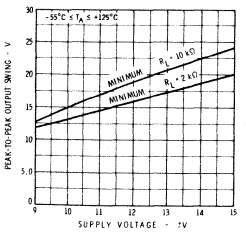
Parameter (see definitions)	Conditions	Min.	Typ.	Max.	Units
Input Offset Voltage	$R_S \leq 10\,k\Omega$		1.0	5.0	mV
Input Offset Current			50	200	nA
Input Bias Current			200	500	nA
Input Resistance		150	400		kΩ
Output Resistance			150		Ω
Power Consumption	V_S = ±15 V		80	165	mW
Transient Response	V_{in} = 20 mV, R_L = 2 kΩ,				
Risetime	C_1 = 5000 pF, R_1 = 1.5 kΩ, C_2 = 200 pF, R_2 = 50 Ω		0.3	1.0	μs
Overshoot	$C_L \leq 100$ pF		10	30	%
The following specifications apply for -55°C ≤ T_A ≤ +125°C:					
Input Offset Voltage	$R_S \leq 10$ kΩ			6.0	mV
Average Temperature Coefficient of Input Offset Voltage	R_S = 50 Ω		3.0		μV/°C
	$R_S \leq 10$ kΩ		6.0		μV/°C
Large-Signal Voltage Gain	V_S = ±15 V, $R_L \geq 2$ kΩ, V_{out} = ±10 V	25,000	45,000	70,000	
Output Voltage Swing	V_S = ±15 V, $R_L \geq 10$ kΩ	±12	±14		V
	V_S = ±15 V, $R_L \geq 2$ kΩ	±10	±13		V
Input Voltage Range	V_S = ±15 V	±8.0	±10		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		25	150	μV/V
Input Offset Current	T_A = +125°C		20	200	nA
	T_A = -55°C		100	500	nA
Input Bias Current	T_A = -55°C		0.5	1.5	μA
Input Resistance		40	100		kΩ

GUARANTEED ELECTRICAL CHARACTERISTICS

VOLTAGE GAIN



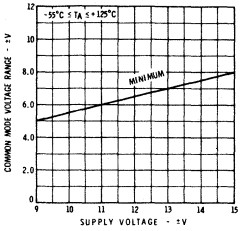
OUTPUT VOLTAGE SWING



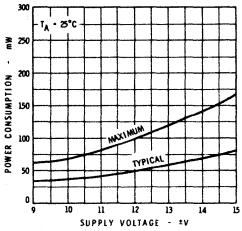
C

GUARANTEED ELECTRICAL CHARACTERISTICS (CONT'D)

INPUT COMMON MODE VOLTAGE RANGE

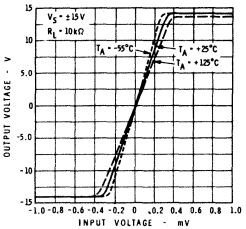


POWER CONSUMPTION

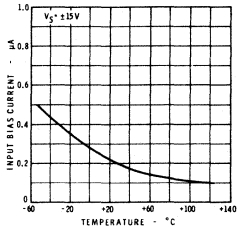


TYPICAL PERFORMANCE CURVES

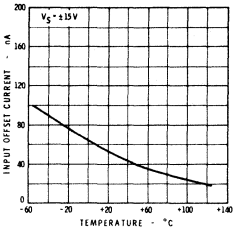
VOLTAGE TRANSFER CHARACTERISTIC



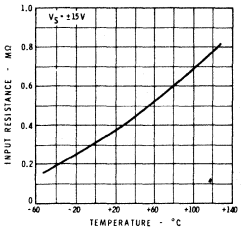
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



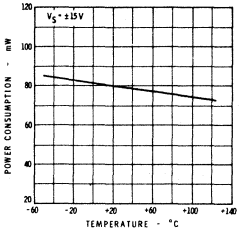
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



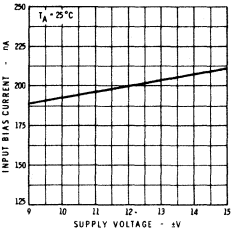
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



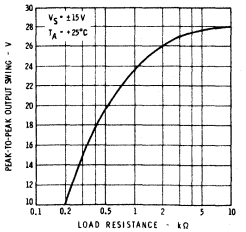
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



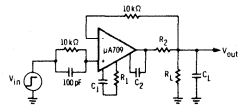
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



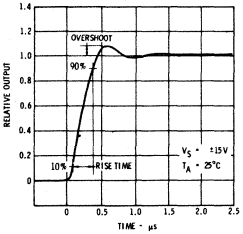
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



TRANSIENT RESPONSE TEST CIRCUIT



TRANSIENT RESPONSE



DEFINITION OF TERMS

INPUT OFFSET VOLTAGE - That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT - The difference in the currents into the two input terminals with the output at zero volts.

INPUT RESISTANCE - The resistance looking into either input terminal with the other grounded.

INPUT BIAS CURRENT - The average of the two input currents.

INPUT VOLTAGE RANGE - A range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

INPUT COMMON MODE REJECTION RATIO - The ratio of the input voltage range to the maximum change in input offset voltage over this range.

LARGE-SIGNAL VOLTAGE GAIN - The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT VOLTAGE SWING - The peak output swing, referred to zero, that can be obtained without clipping.

OUTPUT RESISTANCE - The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

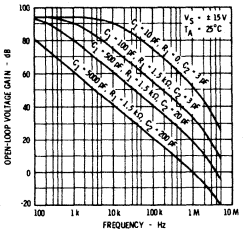
POWER CONSUMPTION - The DC power required to operate the amplifier with the output at zero and with no load current.

SUPPLY VOLTAGE REJECTION RATIO - The ratio of the change in input offset voltage to the change in supply voltage producing it.

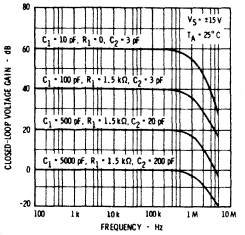
TRANSIENT RESPONSE - The closed-loop step function response of the amplifier under small-signal conditions.

TYPICAL PERFORMANCE CURVES

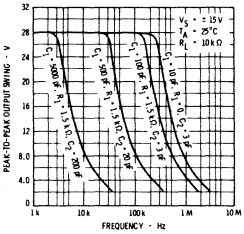
OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF COMPENSATION



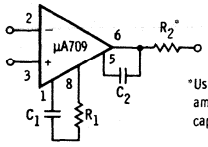
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS



OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS COMPENSATION NETWORKS



FREQUENCY COMPENSATION CIRCUIT



*Use R_2 = 50 Ω when the amplifier is operated with capacitive loading.

μA709B

HIGH PERFORMANCE OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

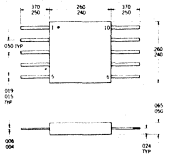
GENERAL DESCRIPTION — The μA709B is a high-gain operational amplifier constructed on a single silicon chip using the Fairchild Planar* epitaxial process. It features low offset, high input impedance, large input common mode range, high output swing under load and low power consumption. The device displays exceptional temperature stability and will operate over a wide range of supply voltages with little degradation of performance. The amplifier is intended for use in DC servo systems, high impedance analog computers, in low-level instrumentation applications and for the generation of special linear and nonlinear transfer functions. For improved specifications, see μA709A or μA709 data sheet.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18 V
Internal Power Dissipation (Note 1)	250 mW
Differential Input Voltage	±5.0 V
Input Voltage	±10 V
Output Short-Circuit Duration ($T_A = 25°C$)	5 sec
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 60 second time limit)	300°C

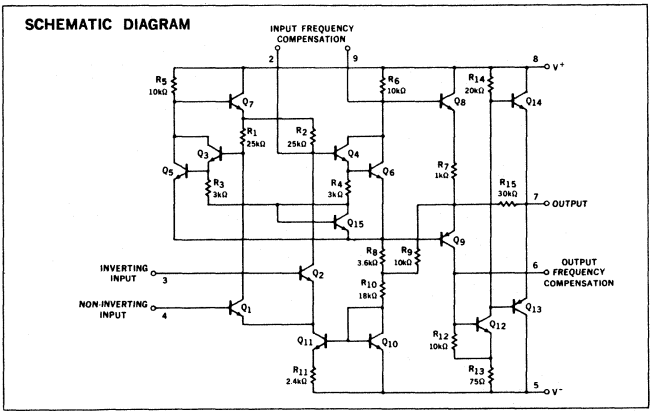
PHYSICAL DIMENSIONS

in accordance with
JEDEC (TO-91) outline
10 Lead Cerpak

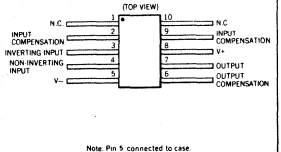


ORDER PART NO. U3F7709313

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



Note: Pin 5 connected to case.

*Planar is a patented Fairchild process.

NOTES:
(1) Rating applies for case temperatures to +125°C; derate linearly at 2.5 mW/°C for ambient temperatures above +60°C.

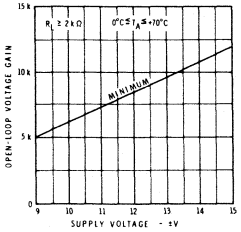
FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified)

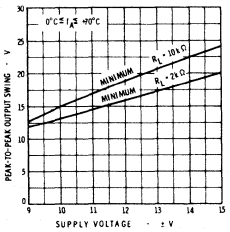
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ, ± 9 V $\leq V_S \leq \pm 15$ V		2.0	7.5	mV
Input Offset Current			100	500	nA
Input Bias Current			0.3	1.5	μA
Input Resistance		50	250		kΩ
Output Resistance			150		Ω
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	15,000	45,000		
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		V
Input Voltage Range		±8.0	±10		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	65	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		25	200	μV/V
Power Consumption			80	200	mW
Transient Response	$V_{in} = 20$ mV, $R_L = 2$ kΩ,				
Risetime	$C_1 = 5000$ pF, $R_1 = 1.5$ kΩ, $C_2 = 200$ pF, $R_2 = 50$ Ω		0.3		μs
Overshoot	$C_L \leq 100$ pF		10		%
The following specifications apply for $0°C \leq T_A \leq +70°C$:					
Input Offset Voltage	$R_S \leq 10$ kΩ, ± 9 V $\leq V_S \leq \pm 15$ V			10	mV
Input Offset Current				750	nA
Input Bias Current				2.0	μA
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	12,000			
Input Resistance		35			kΩ
The following specifications apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage	$R_S \leq 10$ kΩ, ± 9 V $\leq V_S \leq \pm 15$ V			12.5	mV
Input Offset Current				1.2	μA
Input Bias Current				3.0	μA
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	10,000			

GUARANTEED ELECTRICAL CHARACTERISTICS

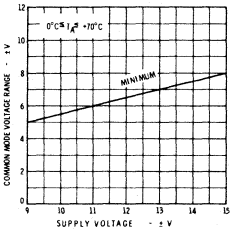
VOLTAGE GAIN



OUTPUT VOLTAGE SWING

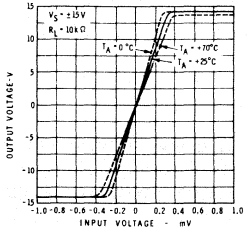


INPUT COMMON MODE VOLTAGE RANGE

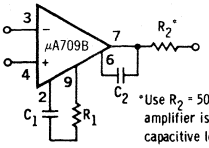


TYPICAL PERFORMANCE CURVES

VOLTAGE TRANSFER CHARACTERISTIC

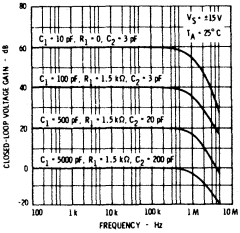


FREQUENCY COMPENSATION CIRCUIT



*Use $R_2 = 50\ \Omega$ when the amplifier is operated with capacitive loading.

FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS



μA709C

HIGH PERFORMANCE OPERATIONAL AMPLIFIER

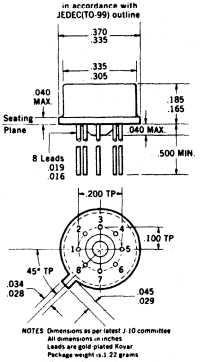
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION - The μA709C is a high-gain operational amplifier constructed on a single silicon chip using the Fairchild Planar epitaxial process. It features low offset, high input impedance, large input common mode range, high output swing under load and low power consumption. The device displays exceptional temperature stability and will operate over a wide range of supply voltages with little degradation of performance. The amplifier is intended for use in DC servo systems, high impedance analog computers, in low-level instrumentation applications and for the generation of special linear and nonlinear transfer functions. For full temperature range operation (-55°C to +125°C) see μA709 or μA709A data sheet.

ABSOLUTE MAXIMUM RATINGS

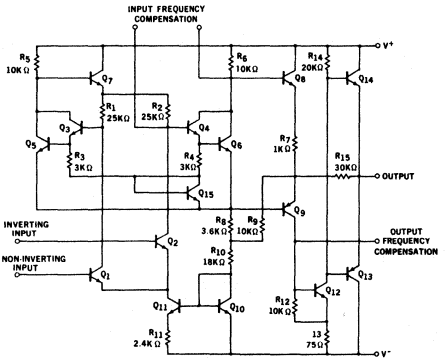
Supply Voltage		± 18 V
Internal Power Dissipation	(Note 1)	250 mW
Differential Input Voltage		± 5.0 V
Input Voltage		± 10 V
Output Short-Circuit Duration	(T_A = 25°C)	5 sec
Storage Temperature Range		-65°C to + 150°C
Operating Temperature Range		0°C to +70°C
Lead Temperature (Soldering, 60 sec)		300°C

PHYSICAL DIMENSIONS

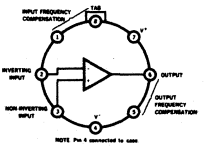


ORDER PART NO.
U5B7709393

SCHEMATIC DIAGRAM

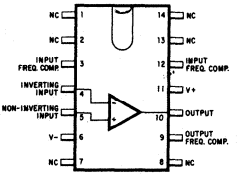


CONNECTION DIAGRAM



(Top View)

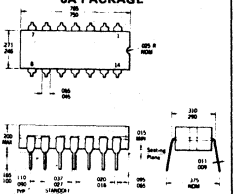
CONNECTION DIAGRAM



PHYSICAL DIMENSIONS

In accordance with JEDEC (TO-116) outline

CERAMIC DIP
6A PACKAGE



NOTES
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers.
They are purposely shipped with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for .020 inch diameter lead.
Leads are tin-plated kovar
Package weight is 2.0 grams

ORDER PART NO.
U6A7709393

NOTE 1: Rating applies for ambient temperatures to +70°C.

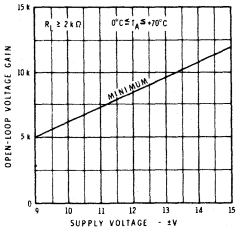
FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_A = 25°C unless otherwise specified)

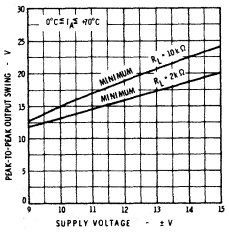
Parameter	Conditions	Min.	Typ.	Max.	Units
Input Offset Voltage	$R_S \leq 10\,k\Omega$, $\pm 9\,V \leq V_S \leq \pm 15\,V$		2.0	7.5	mV
Input Offset Current			100	500	nA
Input Bias Current			0.3	1.5	μA
Input Resistance		50	250		kΩ
Output Resistance			150		Ω
Large-Signal Voltage Gain	$R_L \geq 2\,k\Omega$, $V_{out} = \pm 10\,V$	15,000	45,000		
Output Voltage Swing	$R_L \geq 10\,k\Omega$	±12	±14		V
	$R_L \geq 2\,k\Omega$	±10	±13		V
Input Voltage Range		±8.0	±10		V
Common Mode Rejection Ratio	$R_S \leq 10\,k\Omega$	65	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\,k\Omega$		25	200	μV/V
Power Consumption			80	200	mW
Transient Response	V_{in} = 20 mV, R_L = 2 kΩ,				
Risetime	C_1 = 5000 pF, R_1 = 1.5 kΩ, C_2 = 200 pF, R_2 = 50 Ω		0.3		μs
Overshoot	$C_L \leq 100$ pF		10		%
The following specifications apply for $0°C \leq T_A \leq +70°C$					
Input Offset Voltage	$P_S \leq 10k\Omega$, $\pm 9\,V \leq \pm 15\,V$			10	mV
Input Offset Current				750	nA
Input Bias Current				2.0	μA
Large-Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_{out} = \pm 10\,V$	12,000			
Input Resistance		35			kΩ

GUARANTEED ELECTRICAL CHARACTERISTICS

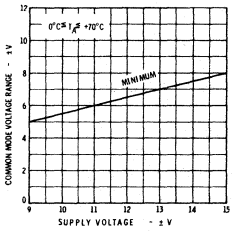
VOLTAGE GAIN



OUTPUT VOLTAGE SWING

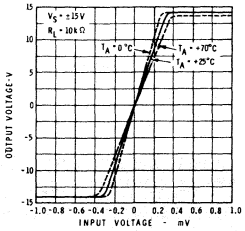


INPUT COMMON MODE VOLTAGE RANGE

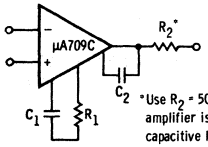


TYPICAL PERFORMANCE CURVES

VOLTAGE TRANSFER CHARACTERISTIC

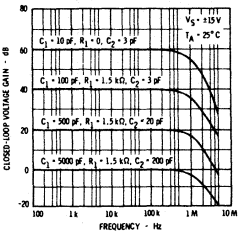


FREQUENCY COMPENSATION CIRCUIT



*Use R_2 = 50 Ω when the amplifier is operated with capacitive loading.

FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS



μA710

HIGH-SPEED DIFFERENTIAL COMPARATOR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

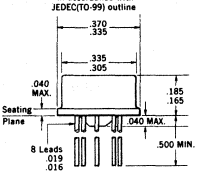
- **IMPROVED SPECIFICATIONS**
- **2 mV MAXIMUM OFFSET VOLTAGE**
- **3 μA MAXIMUM OFFSET CURRENT**
- **1250 MINIMUM VOLTAGE GAIN**
- **10 μV/°C MAXIMUM OFFSET VOLTAGE DRIFT**

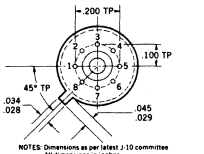
GENERAL DESCRIPTION — The μA710 is a differential voltage comparator intended for applications requiring high accuracy and fast response times. It is constructed on a single silicon chip using the Fairchild Planar* epitaxial process. The device is useful as a variable threshold Schmidt trigger, a pulse height discriminator, a voltage comparator in high-speed A-D converters, a memory sense amplifier or a high-noise immunity line receiver. The output of the comparator is compatible with all integrated logic forms.

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage		+14.0 V
Negative Supply Voltage		−7.0 V
Peak Output Current		10 mA
Differential Input Voltage		±5.0 V
Input Voltage		±7.0 V
Internal Power Dissipation		
TO-99	[Note 1]	300 mW
Flat Package	[Note 2]	200 mW
Operating Temperature Range		−55°C to +125°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)		300°C

PHYSICAL DIMENSIONS
in accordance with JEDEC(TO-99) outline

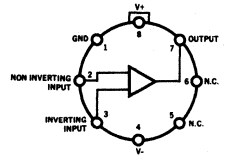




NOTES: Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.22 grams

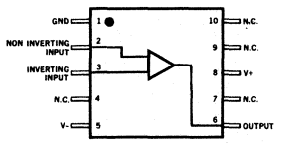
ORDER PART NO.
U5B7710312

TO-99 CONNECTION DIAGRAM
(TOP VIEW)

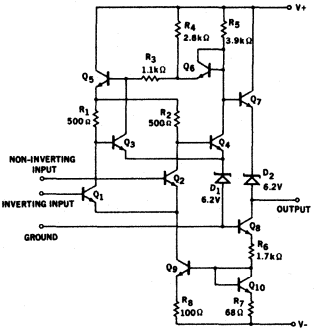


Note: Pin 4 connected to case.

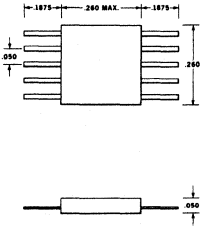
FLAT PACKAGE CONNECTION DIAGRAM
(TOP VIEW)



SCHEMATIC DIAGRAM



PHYSICAL DIMENSIONS
(TYPICAL FLAT PACKAGE)
(TOP VIEW)



ORDER PART NO.
U3F7710312

Notes on page 2

ALSO AVAILABLE IN DIL ORDER PART NO. U6A7710312 * Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS ($T_A = +25°C$, $V^+ = 12.0V$, $V^- = -6.0V$ unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS (Note 4)	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 200\Omega$		0.6	2.0	mV
Input Offset Current			0.75	3.0	μA
Input Bias Current			13	20	μA
Voltage Gain		1250	1700		
Output Resistance			200		Ω
Output Sink Current	$\Delta V_{in} \geq 5$ mV, $V_{out} = 0$	2.0	2.5		mA
Response Time [Note 3]			40		ns
The following specifications apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage	$R_S \leq 200\Omega$			3.0	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$ to $T_A = +125°C$ $R_S = 50\Omega$, $T_A = 25°C$ to $T_A = -55°C$		3.5 2.7	10 10	μV/°C μV/°C
Input Offset Current	$T_A = +125°C$		0.25	3.0	μA
	$T_A = -55°C$		1.8	7.0	μA
Average Temperature Coefficient of Input Offset Current	$T_A = 25°C$ to $T_A = +125°C$ $T_A = 25°C$ to $T_A = -55°C$		5.0 15	25 75	nA/°C nA/°C
Input Bias Current	$T_A = -55°C$		27	45	μA
Input Voltage Range	$V^- = -7.0V$	±5.0			V
Common Mode Rejection Ratio	$R_S \leq 200\Omega$	80	100		dB
Differential Input Voltage Range		±5.0			V
Voltage Gain		1000			
Positive Output Level	$\Delta V_{in} \geq 5$ mV, $0 \leq I_{out} \leq 5.0$ mA	2.5	3.2	4.0	V
Negative Output Level	$\Delta V_{in} \geq 5$ mV	−1.0	−0.5	0	V
Output Sink Current	$T_A = +125°C$, $\Delta V_{in} \geq 5$ mV, $V_{out} = 0$	0.5	1.7		mA
	$T_A = -55°C$, $\Delta V_{in} \geq 5$ mV, $V_{out} = 0$	1.0	2.3		mA
Positive Supply Current	$V_{out} \leq 0$		5.2	9.0	mA
Negative Supply Current			4.6	7.0	mA
Power Consumption			90	150	mW

NOTES:

(1) Rating applies for case temperatures to +125°C; derate linearly at 5.6 mW/°C for ambient temperatures above +105°C.

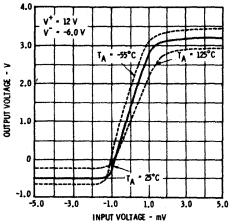
(2) Derate linearly at 4.4 mW/°C for case temperatures above +115°C; derate linearly at 3.3 mW/°C for ambient temperatures above +100°C.

(3) The response time specified (see definitions) is for a 100-mV input step with 5-mV overdrive.

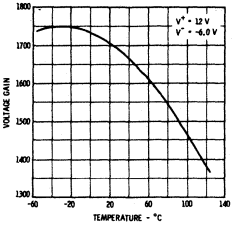
(4) The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage of 1.8V at −55°C, 1.4V at +25°C and 1.0V at +125°C.

TYPICAL PERFORMANCE CURVES

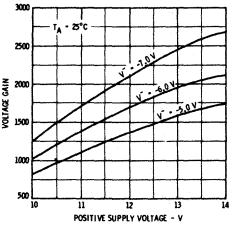
VOLTAGE TRANSFER CHARACTERISTIC



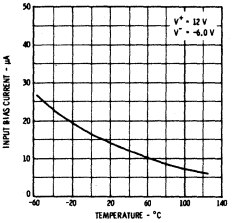
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



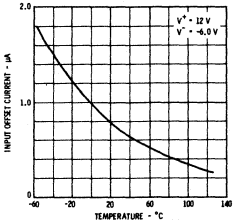
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



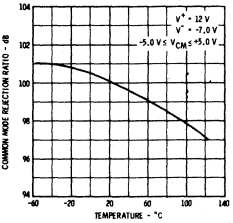
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



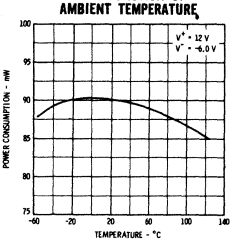
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



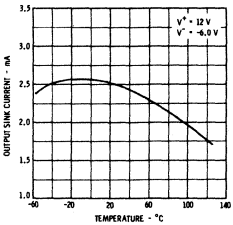
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



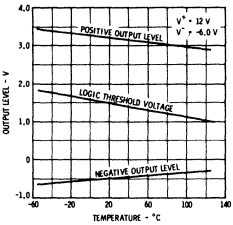
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



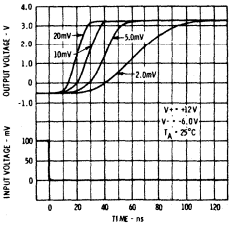
OUTPUT SINK CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



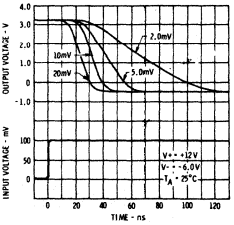
OUTPUT VOLTAGE LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE



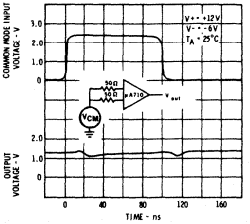
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



COMMON MODE PULSE RESPONSE



DEFINITIONS

LOGIC THRESHOLD VOLTAGE — The approximate voltage at the output of the comparator at which the loading logic circuitry changes its digital state.

INPUT OFFSET VOLTAGE — The voltage between the input terminals when the output is at the logic threshold voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the output at the logic threshold voltage.

INPUT BIAS CURRENT — The average of the two input currents.

INPUT VOLTAGE RANGE — The range of voltage on the input terminals for which the comparator will operate within specifications.

INPUT COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.

DIFFERENTIAL INPUT VOLTAGE RANGE — The range of voltage between the input terminals for which operation within specifications is assured.

VOLTAGE GAIN — The ratio of the change in output voltage to the change in voltage between the input terminals producing it with the DC output level in the vicinity of the logic threshold voltage.

RESPONSE TIME — The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

POSITIVE OUTPUT LEVEL — The DC output voltage in the positive direction with the input voltage equal to or greater than a minimum specified amount.

NEGATIVE OUTPUT LEVEL — The DC output voltage in the negative direction with the input voltage equal to or greater than a minimum specified amount.

OUTPUT SINK CURRENT — The maximum negative current than can be delivered by the comparator.

PEAK OUTPUT CURRENT — The maximum current that may flow into the output load without causing damage to the comparator.

OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the DC output level at the logic threshold voltage.

POWER CONSUMPTION — The DC power into the amplifier with no output load. The DC power will vary with signal level, but is specified as a maximum for the entire range of input-signal conditions.

μA710B
HIGH-SPEED DIFFERENTIAL COMPARATOR
FAIRCHILD LINEAR INTEGRATED CIRCUITS

- **5 mV MAXIMUM OFFSET VOLTAGE**
- **5 μA MAXIMUM OFFSET CURRENT**
- **1000 MINIMUM VOLTAGE GAIN**
- **20 μV/°C MAXIMUM OFFSET VOLTAGE DRIFT**

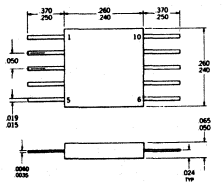
GENERAL DESCRIPTION — The μA710B is a differential voltage comparator intended for applications requiring high accuracy and fast response times. It is constructed on a single silicon chip using the Fairchild Planar* epitaxial process. The device is useful as a variable threshold Schmidt trigger, a pulse height discriminator, a voltage comparator in high-speed A-D converters, a memory sense amplifier or a high-noise immunity line receiver. The output of the comparator is compatible with all integrated logic forms.

For improved specifications, see μA710 data sheet.

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage	+14.0 V
Negative Supply Voltage	−7.0 V
Peak Output Current	10 mA
Differential Input Voltage	±5.0 V
Input Voltage	±7.0 V
Internal Power Dissipation (Note 1)	200 mW
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

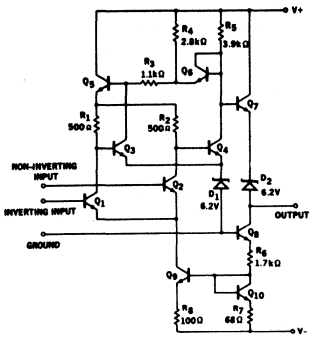
PHYSICAL DIMENSIONS
(TYPICAL FLAT PACKAGE)
(TOP VIEW)



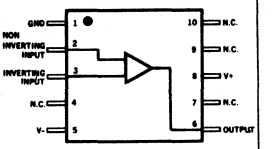
NOTES: All dimensions in inches

ORDER PART NO. U3F7710313

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



(TOP VIEW)

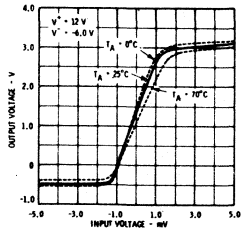
*Planar is a patented Fairchild process.

Notes on page 2

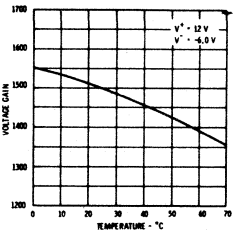
FAIRCHILD
SEMICONDUCTOR

TYPICAL PERFORMANCE CURVES

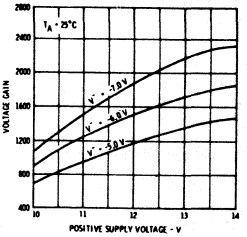
VOLTAGE TRANSFER CHARACTERISTIC



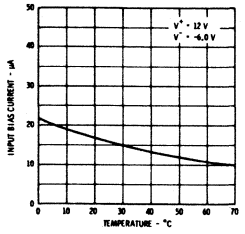
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



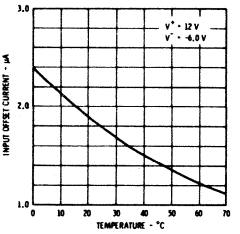
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



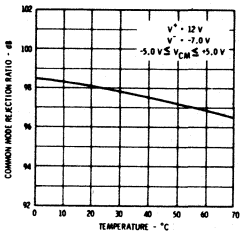
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



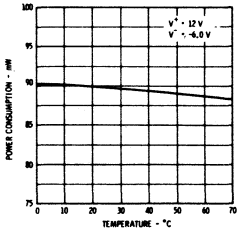
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



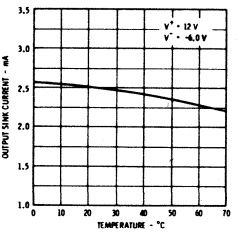
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



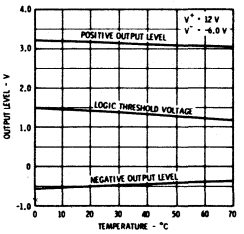
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



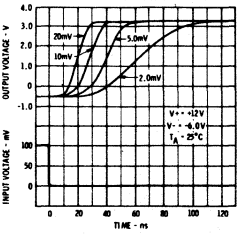
OUTPUT SINK CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



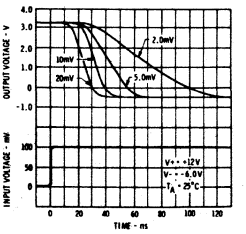
OUTPUT VOLTAGE LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE



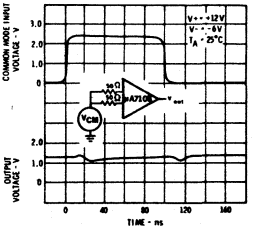
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



COMMON MODE PULSE RESPONSE



ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V^+ = 12.0V$, $V^- = -6.0V$ unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS (Note 3)	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 200\ \Omega$		1.6	5.0	mV
Input Offset Current			1.8	5.0	μA
Input Bias Current			16	25	μA
Voltage Gain		1000	1500		
Output Resistance			200		Ω
Output Sink Current	$\Delta V_{in} \geq 5$ mV, $V_{out} = 0$	1.6	2.5		mA
Response Time (Note 2)			40		ns
The following specifications apply for $0°C \leq T_A \leq +70°C$:					
Input Offset Voltage	$R_S \leq 200\ \Omega$			6.5	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\ \Omega$, $T_A = 0°C$ to $T_A = +70°C$		5.0	20	μV/°C
Input Offset Current				7.5	μA
Average Temperature Coefficient of Input Offset Current	$T_A = 25°C$ to $T_A = +70°C$ $T_A = 25°C$ to $T_A = 0°C$		15 24	50 100	nA/°C nA/°C
Input Bias Current	$T_A = 0°C$		25	40	μA
Voltage Gain		800			
Output Sink Current	$\Delta V_{in} \geq 5$ mV, $V_{out} = 0$	0.5			mA
The following specifications apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage	$R_S \leq 200\ \Omega$			7.5	mV
Input Offset Current	$T_A = +125°C$ $T_A = -55°C$		0.9 3.8	5.0 15	μA μA
Input Bias Current	$T_A = -55°C$		34	80	μA
Input Voltage Range	$V^- = -7.0$ V	±5.0			V
Common Mode Rejection Ratio	$R_S \leq 200\ \Omega$	70	98		dB
Differential Input Voltage Range		±5.0			V
Voltage Gain		500			
Positive Output Level	$\Delta V_{in} \geq 5$ mV, $0 \leq I_{out} \leq 5.0$ mA	2.5	3.2	4.0	V
Negative Output Level	$\Delta V_{in} \geq 5$ mV	−1.0	−0.5	0	V
Positive Supply Current	$V_{out} \leq 0$		5.2	9.0	mA
Negative Supply Current			4.6	7.0	mA
Power Consumption			90	150	mW

NOTES:
(1) Derate linearly at 4.4 mW/°C for case temperatures above +115°C; derate linearly at 3.3 mW/°C for ambient temperatures above +100°C.
(2) The response time specified (see definitions) is for a 100-mV input step with 5-mV overdrive.
(3) The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage of 1.8V at −55°C, 1.5V at 0°C, 1.4V at +25°C, 1.2V at +70°C, and 1.0V at +125°C.

μA710C
HIGH-SPEED DIFFERENTIAL COMPARATOR
FAIRCHILD LINEAR INTEGRATED CIRCUITS

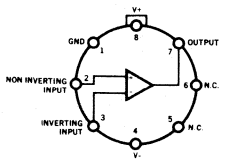
- **IMPROVED SPECIFICATIONS**
- **5mV MAXIMUM OFFSET VOLTAGE**
- **5μA MAXIMUM OFFSET CURRENT**
- **1000 MINIMUM VOLTAGE GAIN**
- **20μV/°C MAXIMUM OFFSET VOLTAGE DRIFT**

GENERAL DESCRIPTION— The μA710C is a differential voltage comparator intended for applications requiring high accuracy and fast response times. It is constructed on a single silicon chip using the Fairchild Planar* epitaxial process. The device is useful as a variable threshold Schmidt trigger, a pulse height discriminator, a voltage comparator in high-speed A-D converters, a memory sense amplifier or a high-noise immunity line receiver. The output of the comparator is compatible with all integrated logic forms.
For full temperature range operation (−55°C to +125°C) see μA710 data sheet.

ABSOLUTE MAXIMUM RATINGS

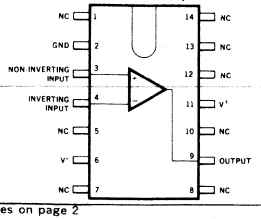
Positive Supply Voltage	+14.0 V
Negative Supply Voltage	−7.0 V
Peak Output Current	10 mA
Differential Input Voltage	±5.0 V
Input Voltage	±7.0 V
Internal Power Dissipation [Note 1]	300 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range TO-99	−65°C to +150°C
Dual-In-Line	−55°C to +125°C
Lead Temperature TO-99 (Soldering, 60 sec)	300°C
Dual-In-Line (Soldering, 10 sec)	260°C

TO-99 CONNECTION DIAGRAM
(TOP VIEW)

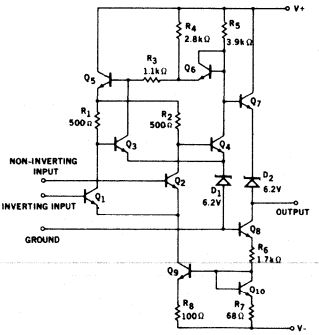


Note: Pin 4 connected to case

CONNECTION DIAGRAM
(TOP VIEW)

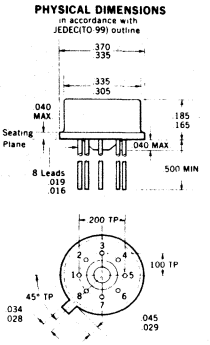


SCHEMATIC DIAGRAM



Notes on page 2

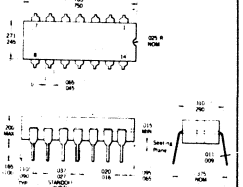
PHYSICAL DIMENSIONS
in accordance with JEDEC(TO 99) outline



NOTES: Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold plated Kovar
Package weight is 1.22 grams

ORDER PART NO.
U5B7710393

PHYSICAL DIMENSIONS
In accordance with JEDEC (TO-116) outline
CERAMIC DIP
6A PACKAGE



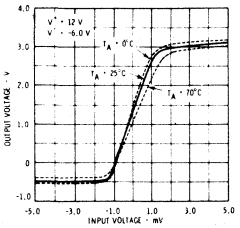
NOTES
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for .020 inch diameter lead.
Leads are tin-plated kovar
Package weight is 2.0 grams

ORDER PART NO.
U6A7710393

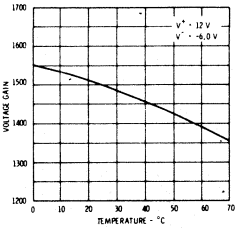
FAIRCHILD
SEMICONDUCTOR

TYPICAL PERFORMANCE CURVES

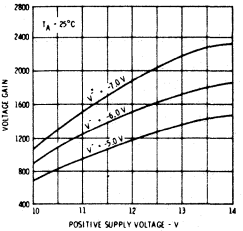
VOLTAGE TRANSFER CHARACTERISTIC



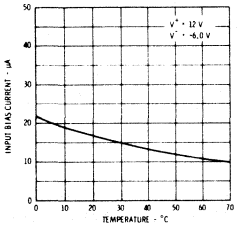
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



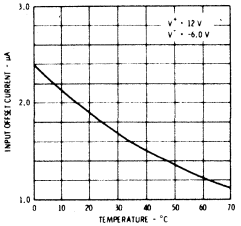
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



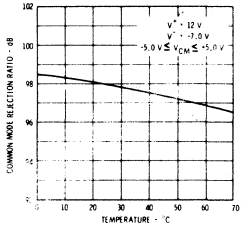
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



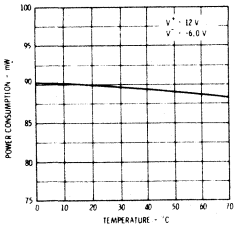
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



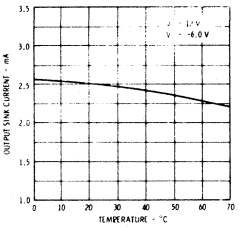
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



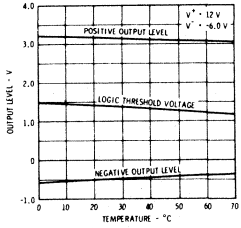
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



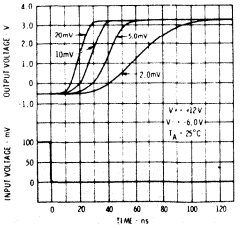
OUTPUT SINK CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



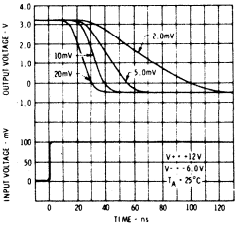
OUTPUT VOLTAGE LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE



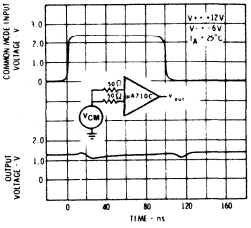
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



COMMON MODE PULSE RESPONSE



ELECTRICAL CHARACTERISTICS (T_A = 25°C, V^+ = 12.0V, V^- = −6.0V unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS (Note 3)	MIN	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 200\Omega$		1.6	5.0	mV
Input Offset Current			1.8	5.0	μA
Input Bias Current			16	25	μA
Voltage Gain		1000	1500		
Output Resistance			200		Ω
Output Sink Current	$\Delta V \geq 5$ mV, $V_{out} = 0$	1.6	2.5		mA
Response Time (Note 2)			40		ns
The following specifications apply for 0°C ≤ T_A ≤ +70°C:					
Input Offset Voltage	$R_S \leq 200\Omega$			6.5	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\Omega$, T_A = 0°C to T_A = +70°C		5.0	20	μV/°C
Input Offset Current				7.5	μA
Average Temperature Coefficient of Input Offset Current	T_A = 25°C to T_A = +70°C T_A = 25°C to T_A = 0°C		15 24	50 100	nA/°C nA/°C
Input Bias Current	T_A = 0°C		25	40	μA
Input Voltage Range	V^- = −7.0V	±5.0			V
Common Mode Rejection Ratio	$R_S \leq 200\Omega$	70	98		dB
Differential Input Voltage Range		±5.0			V
Voltage Gain		800			
Positive Output Level	$\Delta V_{in} \geq 5$ mV, 0 ≤ I_{out} ≤ 5.0 mA	2.5	3.2	4.0	V
Negative Output Level	$\Delta V_{in} \geq 5$ mV	−1.0	−0.5	0	V
Output Sink Current	$\Delta V_{in} \geq 5$ mV, $V_{out} = 0$	0.5			mA
Positive Supply Current	$V_{out} \leq 0$		5.2	9.0	mA
Negative Supply Current			4.6	7.0	mA
Power Consumption			90	150	mW

NOTES:

(1) Ratings apply for ambient temperatures to +70°C.

(2) The response time specified (see definitions) is for a 100-mV input step with 5-mV overdrive.

(3) The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage of 1.5V at 0°C, 1.4V at +25°C and 1.2V at +70°C.

DEFINITIONS

LOGIC THRESHOLD VOLTAGE — The approximate voltage at the output of the comparator at which the loading logic circuitry changes its digital state.

INPUT OFFSET VOLTAGE — The voltage between the input terminals when the output is at the logic threshold voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the output at the logic threshold voltage.

INPUT BIAS CURRENT — The average of the two input currents.

INPUT VOLTAGE RANGE — The range of voltage on the input terminals for which the comparator will operate within specifications.

INPUT COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.

DIFFERENTIAL INPUT VOLTAGE RANGE — The range of voltage between the input terminals for which operation within specifications is assured.

VOLTAGE GAIN — The ratio of the change in output voltage to the change in voltage between the input terminals producing it with the DC output level in the vicinity of the logic threshold voltage.

RESPONSE TIME — The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

POSITIVE OUTPUT LEVEL — The DC output voltage in the positive direction with the input voltage equal to or greater than a minimum specified amount.

NEGATIVE OUTPUT LEVEL — The DC output voltage in the negative direction with the input voltage equal to or greater than a minimum specified amount.

OUTPUT SINK CURRENT — The maximum negative current than can be delivered by the comparator.

PEAK OUTPUT CURRENT — The maximum current that may flow into the output load without causing damage to the comparator.

OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the DC output level at the logic threshold voltage.

POWER CONSUMPTION — The DC power into the amplifier with no output load. The DC power will vary with signal level, but is specified as a maximum for the entire range of input-signal conditions.

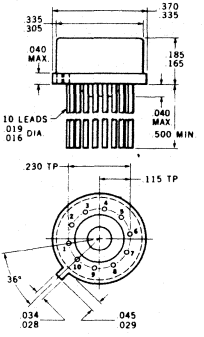
μA711
DUAL COMPARATOR
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION - The μA711 is a dual, differential voltage comparator intended primarily for core-memory sense amplifier applications. The device features high accuracy, fast response times, large input voltage range, low power consumption and compatibility with practically all integrated logic forms. When used as a sense amplifier, the threshold voltage can be adjusted over a wide range, almost independent of the integrated circuit characteristics. Independent strobing of each comparator channel is provided, and pulse stretching on the output is easily accomplished. Other applications of the dual comparator include a window discriminator in pulse height detectors and a double-ended limit detector for automatic Go/No-go test equipment. The μA711, which is similar to the μA710 differential comparator, is constructed on a 40-mil square silicon chip using the Fairchild Planar* epitaxial process.

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage	+14.0 V
Negative Supply Voltage	-7.0 V
Peak Output Current	50 mA
Differential Input Voltage	±5.0 V
Input Voltage	±7.0 V
Strobe Voltage	0 to +6.0 V
Internal Power Dissipation (Note 1)	300 mW
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

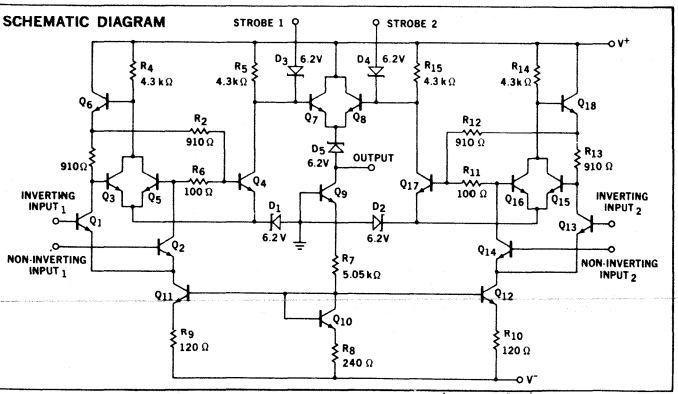
PHYSICAL DIMENSIONS
(In accordance with JEDEC TO-100)



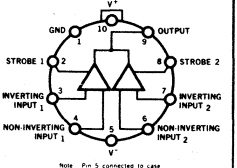
NOTES: All dimensions in inches
Leads are gold plated kovar
Package weight is 1.32 grams

ORDER PART NO.
U5F7711312

SCHEMATIC DIAGRAM



TO-5 CONNECTION DIAGRAM (TOP VIEW)



Note: Pin 5 connected to case

ALSO AVAILABLE IN DIL ORDER PART NO. U6A7711312

Notes on page 2

* Planar is a patented Fairchild process.

FAIRCHILD SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V^+ = 12.0 V, V^- = -6.0 V unless otherwise specified)

Parameter (see definitions)	Conditions	Min.	Typ.	Max.	Units
Input Offset Voltage	V_{out} = +1.4 V, $R_S \leq 200\,\Omega$, V_{CM} = 0		1.0	3.5	mV
	V_{out} = +1.4 V, $R_S \leq 200\,\Omega$		1.0	5.0	mV
Input Offset Current	V_{out} = +1.4 V		0.5	10.0	μA
Input Bias Current			25	75	μA
Voltage Gain		750	1500		
Response Time (Note 2)			40		ns
Strobe Release Time			12		ns
Input Voltage Range	V^- = -7.0 V	±5.0			V
Differential Input Voltage Range		±5.0			V
Output Resistance			200		Ω
Positive Output Level	$V_{in} \geq 10$ mV		4.5	5.0	V
Loaded Positive Output Level	$V_{in} \geq 10$ mV, I_O = 5 mA	2.5	3.5		V
Negative Output Level	$V_{in} \geq 10$ mV	-1.0	-0.5	0	V
Strobed Output Level	$V_{strobe} \leq 0.3$ V	-1.0		0	V
Output Sink Current	$V_{in} \geq 10$ mV, $V_{out} \geq 0$	0.5	0.8		mA
Strobe Current	V_{strobe} = 100 mV		1.2	2.5	mA
Positive Supply Current	$V_{out} \leq 0$		8.6		mA
Negative Supply Current			3.9		mA
Power Consumption			130	200	mW
The following specifications apply for -55°C ≤ T_A ≤ +125°C:					
Input Offset Voltage (Note 3)	$R_S \leq 200\,\Omega$, V_{CM} = 0			4.5	mV
	$R_S \leq 200\,\Omega$			6.0	mV
Input Offset Current (Note 3)				20	μA
Input Bias Current				150	μA
Temperature Coefficient of Input Offset Voltage			5.0		μV/°C
Voltage Gain		500			

NOTES:

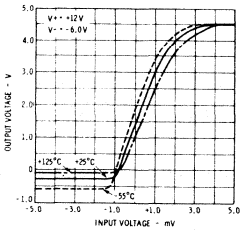
(1) Rating applies for case temperatures to +125°C; derate linearly at 5.6 mW/°C for ambient temperatures above 105°C.

(2) The response time specified (see definitions) is for a 100-mV input step with 5-mV overdrive.

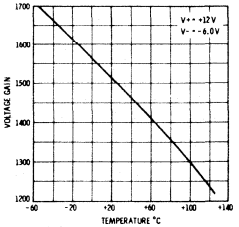
(3) The input offset voltage (see definitions) is specified for a logic threshold voltage of 1.8 V at -55°C, 1.4 V at +25°C and 1.0 V at +125°C.

TYPICAL PERFORMANCE CURVES

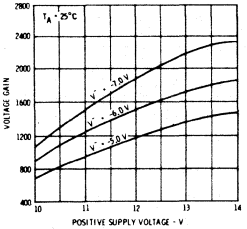
VOLTAGE TRANSFER CHARACTERISTIC



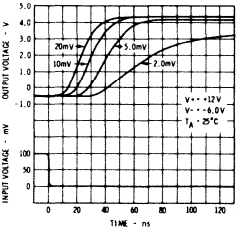
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



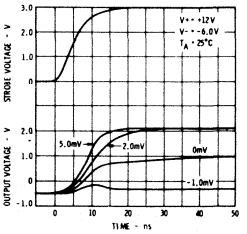
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



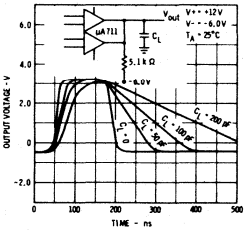
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



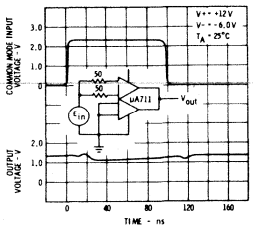
STROBE RELEASE TIME FOR VARIOUS INPUT OVERDRIVES



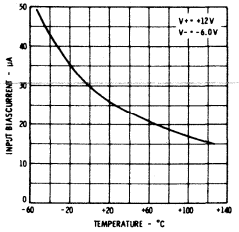
OUTPUT PULSE STRETCHING WITH CAPACITIVE LOADING



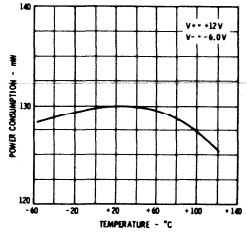
COMMON MODE PULSE RESPONSE



INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



DEFINITIONS

LOGIC THRESHOLD VOLTAGE - The approximate voltage at the output of the comparator at which the loading logic circuitry changes its digital state.

INPUT OFFSET VOLTAGE* - The voltage between the input terminals when the output is at the logic threshold voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT* - The difference in the currents into the two input terminals with the output at the logic threshold voltage.

INPUT BIAS CURRENT* - The average of the two input currents.

INPUT VOLTAGE RANGE* - The range of voltage on the input terminals for which the comparator will operate within specifications.

DIFFERENTIAL INPUT VOLTAGE RANGE* - The range of voltage between the input terminals for which operation within specifications is assured.

VOLTAGE GAIN* - The ratio of the change in output voltage to the change in voltage between the input terminals producing it with the DC output level in the vicinity of the logic threshold voltage.

RESPONSE TIME* - The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

STROBE RELEASE TIME* - The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from the zero to the one logic level. Appropriate input conditions are assumed.

POSITIVE OUTPUT LEVEL* - The DC output voltage in the positive direction with the input voltage equal to or greater than a minimum specified amount.

NEGATIVE OUTPUT LEVEL* - The DC output voltage in the negative direction with the input voltage equal to or greater than a minimum specified amount.

OUTPUT SINK CURRENT - The maximum negative current that can be delivered by the comparator.

PEAK OUTPUT CURRENT - The maximum current that may flow into the output load without causing damage to the comparator.

OUTPUT RESISTANCE* - The resistance seen looking into the output terminal with the DC output level at the logic threshold voltage.

STROBED OUTPUT LEVEL* - The DC output voltage, independent of input voltage, with the voltage on the strobe terminal equal to or less than a minimum specified amount.

STROBE CURRENT - The maximum current drawn by the strobe terminal when it is at the zero logic level.

POWER CONSUMPTION - The DC power into the amplifier with no output load. The DC power will vary with signal level, but is specified as a maximum for the entire range of input-signal conditions.

*These definitions apply for either side with the other disabled with the strobe.

μA711C
DUAL COMPARATOR
FAIRCHILD LINEAR INTEGRATED CIRCUITS

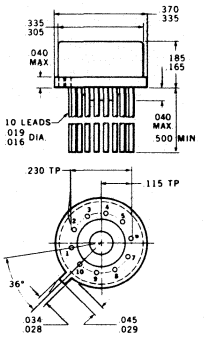
GENERAL DESCRIPTION - The μA711C is a dual, differential voltage comparator intended primarily for core-memory sense amplifier applications. The device features high accuracy, fast response times, large input voltage range, low power consumption and compatibility with practically all integrated logic forms. When used as a sense amplifier, the threshold voltage can be adjusted over a wide range, almost independent of the integrated circuit characteristics. Independent strobing of each comparator channel is provided, and pulse stretching on the output is easily accomplished. Other applications of the dual comparator include a window discriminator in pulse height detectors and a double-ended limit detector for automatic Go/No-go test equipment. The μA711C, which is similar to the μA710C differential comparator, is constructed on a 40-mil square silicon chip using the Fairchild Planar epitaxial process.

For full temperature range operation (-55°C to +125°C) see μA711 data sheet.

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage		+14.0 V
Negative Supply Voltage		-7.0 V
Peak Output Current		50 mA
Differential Input Voltage		±5.0 V
Input Voltage		±7.0 V
Strobe Voltage		0 to +6.0 V
Internal Power Dissipation	(Note 1)	300 mW
Operating Temperature Range		0°C to +70°C
Storage Temperature Range		-65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

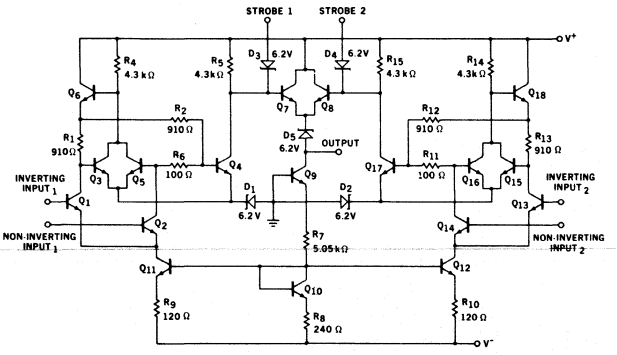
PHYSICAL DIMENSIONS
In accordance with JEDEC (TO-100) outline



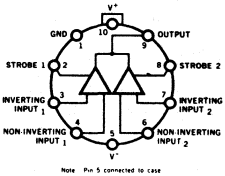
NOTES: All dimensions in inches
Leads are gold plated Kovar
Package weight is 1.02 grams

ORDER PART NO.
U5F7711393

SCHEMATIC DIAGRAM



TO-100 CONNECTION DIAGRAM (TOP VIEW)



Note: Pin 5 connected to case

ALSO AVAILABLE IN DIL ORDER PART NO. U6A7711393

Notes on page 2

FAIRCHILD SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V^+ = 12.0 V, V^- = -6.0 V unless otherwise specified)

Parameter	Conditions	Min.	Typ.	Max	Units
Input Offset Voltage	V_{out} = +1.4 V, $R_S \leq 200\,\Omega$, V_{CM} = 0		1.0	5.0	mV
	V_{out} = +1.4 V, $R_S \leq 200\,\Omega$		1.0	7.5	mV
Input Offset Current	V_{out} = +1.4 V		0.5	15	μA
Input Bias Current			25	100	μA
Voltage Gain		700	1500		
Response Time (Note 2)			40		ns
Strobe Release Time			12		ns
Input Voltage Range	V^- = -7.0 V	±5.0			V
Differential Input Voltage Range		±5.0			V
Output Resistance			200		Ω
Positive Output Level	$V_{in} \geq 10$ mV		4.5	5.0	V
Loaded Positive Output Level	$V_{in} \geq 10$ mV, I_O = 5 mA	2.5	3.5		V
Negative Output Level	$V_{in} \geq 10$ mV	-1.0	-0.5	0	V
Strobed Output Level	$V_{strobe} \leq 0.3$ V	-1.0		0	V
Output Sink Current	$V_{in} \geq 10$ mV, $V_{out} \geq 0$	0.5	0.8		mA
Strobe Current	V_{strobe} = 100 mV		1.2	2.5	mA
Positive Supply Current	$V_{out} \leq 0$		8.6		mA
Negative Supply Current			3.9		mA
Power Consumption			130	230	mW
The following specifications apply for 0°C $\leq T_A \leq$ +70°C:					
Input Offset Voltage (Note 3)	$R_S \leq 200\,\Omega$, V_{CM} = 0			6.0	mV
	$R_S \leq 200\,\Omega$			10	mV
Input Offset Current (Note 3)				25	μA
Input Bias Current				150	μA
Temperature Coefficient of Input Offset Voltage			5.0		μV/°C
Voltage Gain		500			

NOTES:

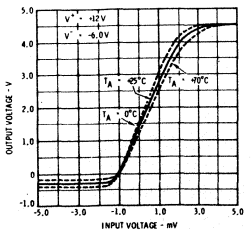
(1) Rating applies for ambient temperatures to +70°C.

(2) The response time specified is for a 100-mV input step with 5-mV overdrive.

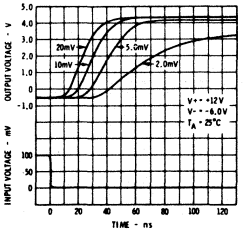
(3) The input offset voltage is specified for a logic threshold voltage of 1.5 V at 0°C, 1.4 V at +25°C and 1.2 V at +70°C.

TYPICAL ELECTRICAL CHARACTERISTICS

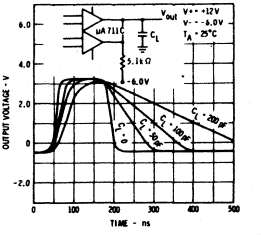
VOLTAGE TRANSFER CHARACTERISTIC



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



OUTPUT PULSE STRETCHING WITH CAPACITIVE LOADING



μA715

HIGH SPEED OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

- **HIGH SLEW RATE . . . . . 100 V/μs**
- **FAST SETTLING TIME . . . 300 ns**
- **WIDE BANDWIDTH . . . . . 65 MHz**
- **WIDE OPERATING SUPPLY RANGE**
- **WIDE INPUT VOLTAGE RANGES**

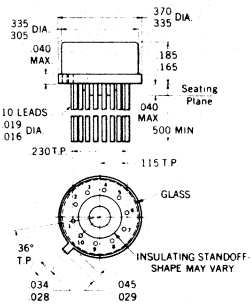
GENERAL DESCRIPTION — The μA715 is a high speed, high gain, monolithic operational amplifier constructed on a single silicon chip using the Fairchild Planar* epitaxial process. It is intended for use in a wide range of applications where fast signal acquisition or wide bandwidth is required. The μA715 features fast settling time, high slew rate, low offsets, and high output swing for large signal applications. In addition, the device displays excellent temperature stability and will operate over a wide range of supply voltages. The μA715 is ideally suited for use in A to D and D to A converters, active filters, deflection amplifiers, video amplifiers, phase locked loops, multiplexed analog gates, precision comparators, sample and holds, and general feedback applications requiring DC wide bandwidth operation. (For other Fairchild operational amplifiers, see table on page 6.)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18 V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±15 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 60 seconds)	300°C

PHYSICAL DIMENSIONS

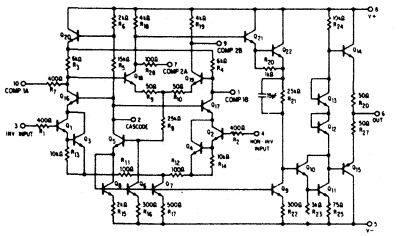
In accordance with JEDEC (TO-100) outline



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.32 grams
Lead 5 is shorted to the can

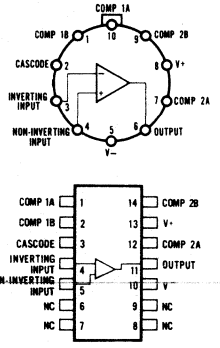
ORDER PART NO. U5F7715312

EQUIVALENT CIRCUIT



CONNECTION DIAGRAM

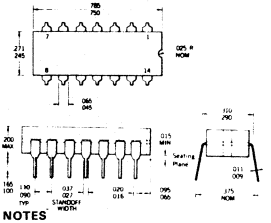
(TOP VIEW)



PHYSICAL DIMENSIONS

In accordance with JEDEC (TO-116) outline

CERAMIC DIP
6A PACKAGE



NOTES
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for .020 inch diameter pad.
Leads are tin-plated kovar
Package weight is 2.0 grams

ORDER PART NO. U6A7715312

*Planar is a patented Fairchild process.

Notes on Page 2

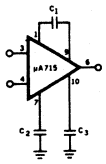
FAIRCHILD SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ		2.0	5.0	mV
Input Offset Current			70	250	nA
Input Bias Current			400	750	nA
Input Resistance			1.0		MΩ
Input Voltage Range		±10	±12		Volts
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	15,000	30,000		
Output Resistance			75		Ω
Supply Current			5.5	7.0	mA
Power Consumption			165	210	mW
Acquisition Time (Unity Gain)	$V_{out} = +5$ V		800		ns
Settling Time (Unity Gain)			300		ns
Transient Response (Unity Gain)	$V_{in} = 400$ mV				
Risetime			30	60	ns
Overshoot			25	40	%
Slew Rate	Av = 100		70		V/μs
	Av = 10		38		V/μs
	Av = 1 (non-inverting)	15	18		V/μs
	Av = 1 (inverting)		100		V/μs
The following apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage	$R_S \leq 10$ kΩ			7.5	mV
Input Offset Current	$T_A = +125°C$			250	nA
	$T_A = -55°C$			800	nA
Input Bias Current	$T_A = +125°C$			750	nA
	$T_A = -55°C$			4.0	μA
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	74	92		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		45	300	μV/V
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	10,000			
Output Voltage Swing	$R_L \geq 2$ kΩ	±10	±13		V

NOTES:
(1) Rating applies for case temperatures to +125°C, derate linearly at 6.5 mW/°C for ambient temperatures above +75°C.
(2) For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

FREQUENCY COMPENSATION CIRCUIT

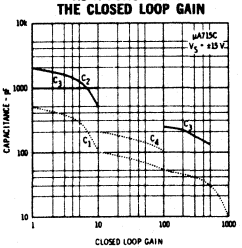


NON-INVERTING COMPENSATION COMPONENTS VALUES

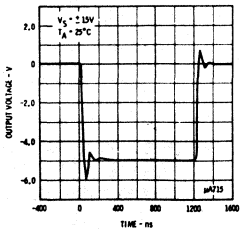
CLOSED LOOP GAIN	C_1	C_2	C_3
1000	10 pF	—	—
100	50 pF	—	250 pF
10	100 pF	500 pF	1000 pF
1	500 pF	2000 pF	1000 pF

*For Gain 10, compensation may be simplified by removing C_2, C_3 and adding a 200 pF capacitor (C_4) between Pin 7 and 10.

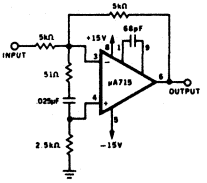
SUGGESTED VALUES OF COMPENSATION CAPACITORS AS A FUNCTION OF THE CLOSED LOOP GAIN



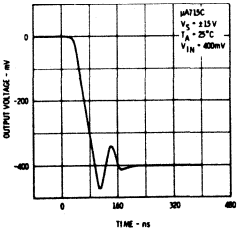
LARGE SIGNAL PULSE RESPONSE UNITY GAIN



INVERTING UNITY GAIN HIGH SLEW RATE CIRCUIT

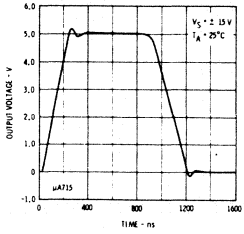


SMALL SIGNAL PULSE RESPONSE INVERTING UNITY GAIN

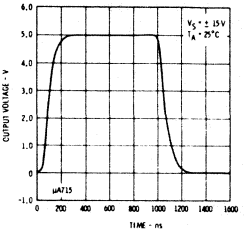


TYPICAL PERFORMANCE CURVES

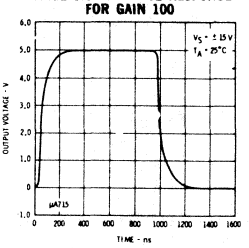
UNITY GAIN LARGE SIGNAL PULSE RESPONSE



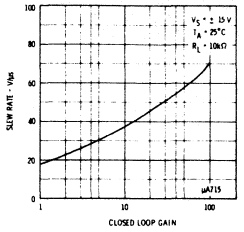
LARGE SIGNAL PULSE RESPONSE FOR GAIN 10



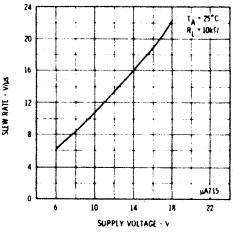
LARGE SIGNAL PULSE RESPONSE FOR GAIN 100



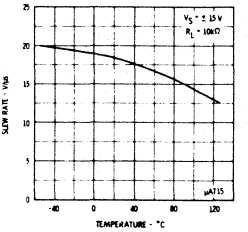
SLEW RATE AS A FUNCTION OF THE CLOSED LOOP GAIN



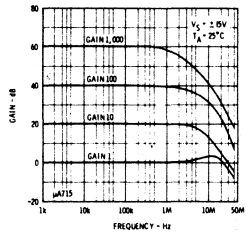
SLEW RATE AS A FUNCTION OF SUPPLY VOLTAGE



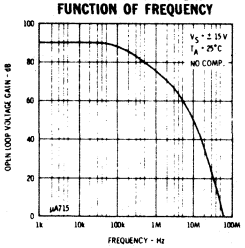
SLEW RATE AS A FUNCTION OF TEMPERATURE



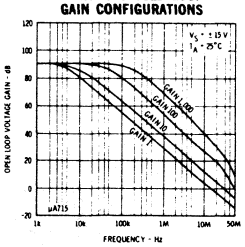
CLOSED LOOP FREQUENCY RESPONSE FOR VARIOUS GAIN CONFIGURATIONS



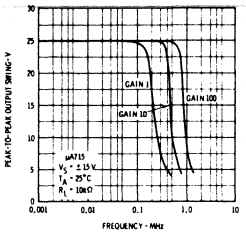
OPEN LOOP GAIN AS A FUNCTION OF FREQUENCY



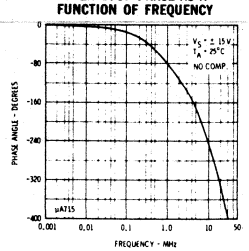
OPEN LOOP RESPONSE WITH COMPENSATION NECESSARY FOR VARIOUS CLOSED LOOP GAIN CONFIGURATIONS



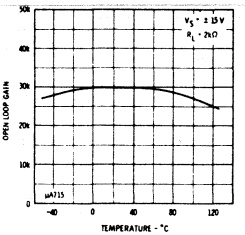
OUTPUT SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS CLOSED LOOP GAIN CONFIGURATIONS



OPEN LOOP PHASE AS A FUNCTION OF FREQUENCY

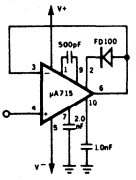


OPEN LOOP GAIN AS A FUNCTION OF AMBIENT TEMPERATURE

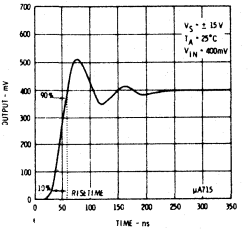


TYPICAL PERFORMANCE CURVES

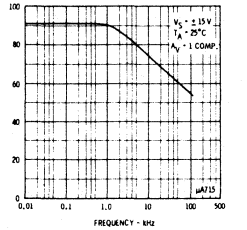
VOLTAGE FOLLOWER



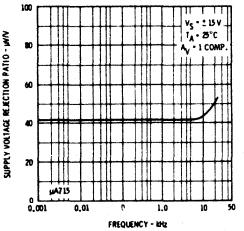
VOLTAGE FOLLOWER TRANSIENT RESPONSE



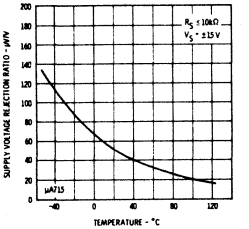
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



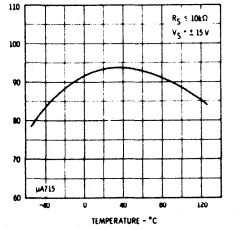
SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF FREQUENCY



SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE

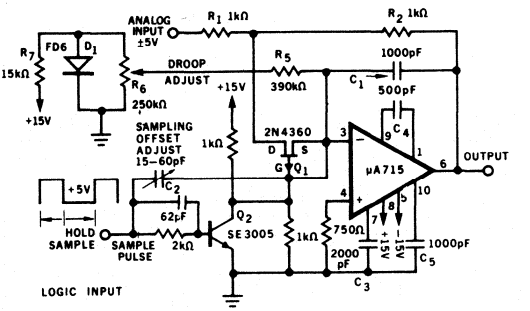


COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



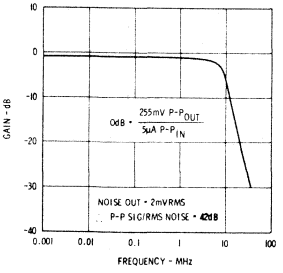
TYPICAL APPLICATIONS

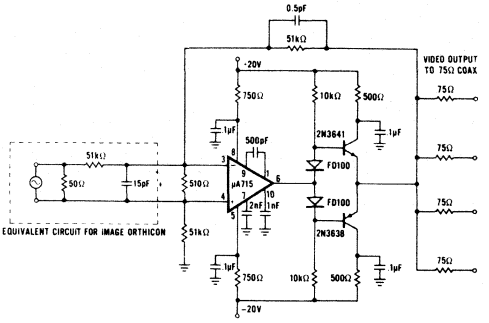
HIGH SPEED SAMPLE AND HOLD



TYPICAL APPLICATIONS

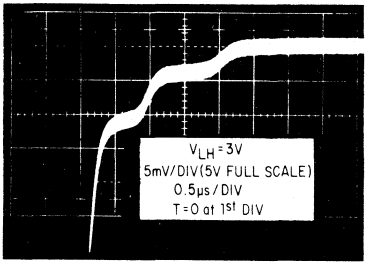
WIDE BAND VIDEO AMPLIFIER WITH 75Ω COAX CABLE DRIVE CAPABILITY



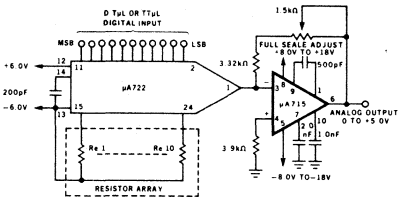


HIGH SPEED 10 BIT DIGITAL TO ANALOG CONVERTER

ANALOG OUTPUT 0 TO +5.0 V



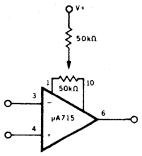
μA722/μA715 op amp switching ON, as it should with typical logic voltage on least significant bits. Note complete absence of ringing.



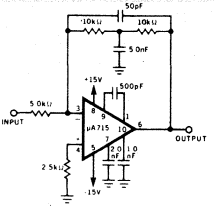
Conversion Rate
6 bits · 300 ns
8 bits · 600 ns
10 bits · 1000 ns

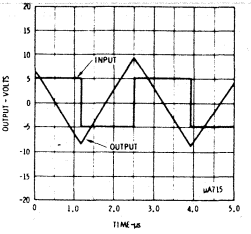
NOTE: See Fairchild App. Note 164 for additional information including how to increase conversion speed by clamping LSB's and how to obtain bipolar outputs.

VOLTAGE OFFSET NULL CIRCUIT



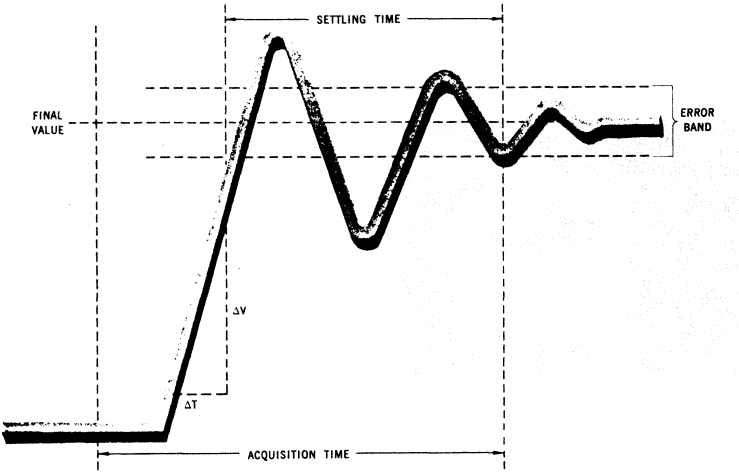
HIGH SPEED INTEGRATOR





DEFINITION OF TERMS

INPUT OFFSET VOLTAGE — That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.
INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the output at zero volts.
INPUT RESISTANCE — The resistance looking into either input terminal with the other grounded.
INPUT BIAS CURRENT — The average of the two input currents.
INPUT VOLTAGE RANGE — The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.
INPUT COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.
SUPPLY VOLTAGE REJECTION RATIO — The ratio of the change in input offset voltage to the change in supply voltage producing it.
LARGE-SIGNAL VOLTAGE GAIN — The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.
OUTPUT VOLTAGE SWING — The peak output swing, referred to zero, that can be obtained without clipping.
OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.
POWER CONSUMPTION — The DC power required to operate the amplifier with the output at zero and with no load current.
TRANSIENT RESPONSE — The closed-loop step-function response of the amplifier under small-signal conditions.
ACQUISITION TIME — The time from change of input until last time output exceeds specified percent of final value.
SLEW RATE — The maximum rate of change of output under large signal condition.
SETTLING TIME — The time from output first reaching final value until last time output exceeds specified percent of final value.



HELPFUL HINTS

LAYOUT — The layout should be such that stray capacitance is minimal.
SUPPLIES — The supplies should be adequately bypassed. Use of 0.1 μF high quality ceramic capacitors is recommended.
RINGING — Excessive ringing (long acquisition time) may occur with large capacitive loads. This may be reduced by isolating the capacitive load with a resistance of 100Ω. Large source resistances may also give rise to the same problem and this may be decreased by the addition of a capacitance across the feedback resistance. A value of around 50 pF for unity gain configuration and around 3.0 pF for gain 10 should be adequate.
LATCH UP — This may occur when the amplifier is used as a voltage follower. The inclusion of a diode between pins 6 and 2 with the cathode towards pin 2 is the recommended preventive.

NOTE: FOR OTHER FAIRCHILD OPERATIONAL AMPLIFIERS, SEE THE FOLLOWING DATA SHEETS:
Instrumentation — μA725, μA725B, μA725C
Temperature Stable Preamps — μA727, μA727B
Micropower — μA735, μA735B, μA735C
FET Input — μA740, μA740C
Frequency Compensated — μA741, μA741C
Duals — μA739C, μA749, μA749C, μA747, μA747C
High Performance — μA748, μA748C, μA101, μA201
Precision — μA777, μA777B, μA777C, μA101A, μA201A, μA301A

μA715C
HIGH SPEED OPERATIONAL AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

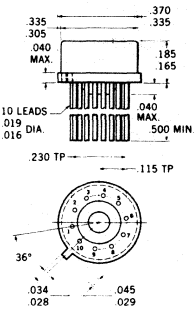
FEATURES
- **FAST SETTLING TIME . . . 300 ns**
- **WIDE BANDWIDTH . . . . . 65 MHz**
- **HIGH SLEW RATE . . . . . 65 V/μs**
- **WIDE OPERATING SUPPLY RANGE**
- **WIDE INPUT VOLTAGE RANGES**

GENERAL DESCRIPTION — The μA715C is a high speed, high gain, monolithic operational amplifier constructed on a single silicon chip using the Fairchild Planar* epitaxial process. It is intended for use in a wide range of applications where fast signal acquisition or wide bandwidth is required. The μA715C features fast settling time, high slew rate, low offsets, and high output swing for large signal applications. In addition, the device displays excellent temperature stability and will operate over a wide range of supply voltages. The μA715C is ideally suited for use in A to D and D to A converters, active filters, deflection amplifiers, video amplifiers, phase locked loops, multiplexed analog gates, precision comparators, sample and holds, and general feedback applications requiring DC wide bandwidth operation. For full temperature range operation (−55°C to +125°C) see μA715 data sheet.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18 V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±15 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 60 seconds)	300°C

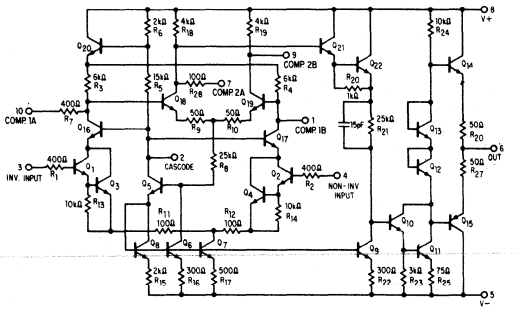
PHYSICAL DIMENSIONS
In accordance with JEDEC (TO-100) outline



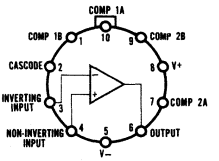
NOTES:
Lead 5 is shorted to the can
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.32 grams

ORDER PART NO. U5F7715393

EQUIVALENT CIRCUIT



CONNECTION DIAGRAM
(TOP VIEW)



Notes on Page 2

ALSO AVAILABLE IN DIL ORDER PART NO. U6A7715393

*Planar is a patented Fairchild process.

FAIRCHILD SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified)

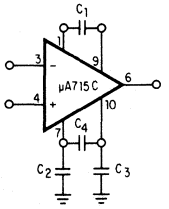
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_s \leq 10$ kΩ		2.0	7.5	mV
Input Offset Current			70	250	nA
Input Bias Current			0.4	1.5	μA
Input Resistance			1.0		MΩ
Input Voltage Range		±10	±12		Volts
Common Mode Rejection Ratio	$R_s \leq 10$ kΩ	74	92		dB
Supply Voltage Rejection Ratio	$R_s \leq 10$ kΩ		70	400	μV/V
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	10,000	30,000		
Output Voltage Swing	$R_L \geq 2$ kΩ	±10	±13		Volts
Output Resistance			75		Ω
Supply Current			5.5	10	mA
Power Consumption			165	300	mW
Acquisition Time (Unity Gain)	$V_{out} = +5$ V		800		ns
Settling Time (Unity Gain)			300		ns
Transient Response (Unity Gain)	$V_{in} = 500$ mV				
Risetime			30	75	ns
Overshoot			30	50	%
Slew Rate	Av = 100		65		V/μs
	Av = 10		40		V/μs
	Av = 1	10	20		V/μs
The following apply for $0°C \leq T_A \leq +70°C$:					
Input Offset Voltage	$R_S = 10$ kΩ			10	mV
Input Offset Current	$T_A = +70°C$			250	nA
	$T_A = 0°C$			750	nA
Input Bias Current	$T_A = +70°C$			1.5	μA
	$T_A = 0°C$			7.5	μA
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	8,000			
Output Voltage Swing	$R_L \geq 2$ kΩ	±10			Volts

NOTES:
(1) Rating applies for ambient temperatures to +70°C.
(2) For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

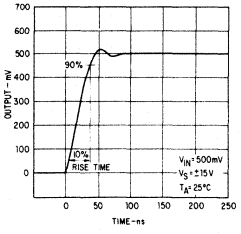
COMPENSATION COMPONENTS VALUES

CLOSED LOOP GAIN	C_1	C_2	C_3	C_4
1000	10 pF	—	—	—
100	50 pF	—	250 pF	—
10	100 pF	—	—	200 pF
1	500 pF	2000 pF	1000 pF	—

FREQUENCY COMPENSATION CIRCUIT



TRANSIENT RESPONSE



μA716C

FIXED-GAIN, LOW DISTORTION AMPLIFIER

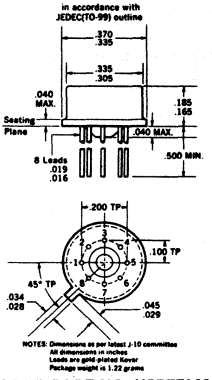
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA716C is a fixed-gain, medium power amplifier intended for use as a telephone system channel amplifier, headset amplifier or general purpose audio amplifier. It provides medium output current capability, low distortion, excellent gain stability, and wide bandwidth. Fixed voltage gains of 10, 20, 100 and 200 are available by selecting external taps.

ABSOLUTE MAXIMUM RATINGS:

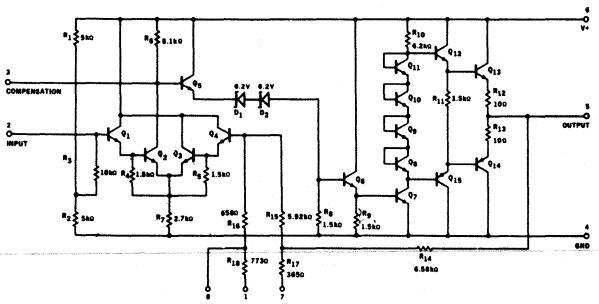
Supply Voltage	27 V
Internal Power Dissipation	600 mW
Input Voltage	±5 V
Peak Output Current ($T_A = 25°C$)	100 mA
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 60 seconds)	300°C

PHYSICAL DIMENSIONS

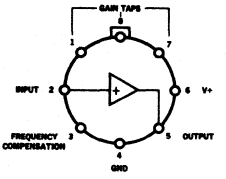


ORDER PART NO. U5B7716393

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



(TOP VIEW)

NOTE: Lead No. 4 internally connected to case

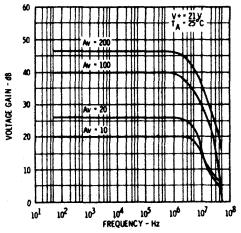
FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V^+ = 21V$ unless otherwise specified)

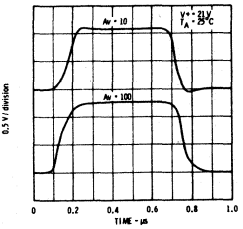
PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Quiescent Power Consumption	$T_A = 25°C$		280	350	mW
Total Harmonic Distortion	$A_V = 10$, $f = 1$ kHz, $P_O = 50$ mW, $R_L = 150\ \Omega$		0.01	0.05	%
	$A_V = 100$, $f = 1$ kHz, $P_O = 50$ mW, $R_L = 150\ \Omega$		0.10	0.50	%
Input Noise Voltage	$R_S = 600\ \Omega$, $T_A = 25°C$, $B_n = 16$ Hz to 150 kHz		8.0		μV_{rms}
Output Voltage Swing	$R_L = 150\ \Omega$	10	14		V_{p-p}
	$R_L \geq 5k\ \Omega$	15	17		V_{p-p}
Input Resistance		9.0	11		kΩ
Output Resistance			1.0		Ω
Voltage Gain	See Table I				
10x		9.0	10	11	
20x		18	20	22	
100x		95	105	115	
200x		185	205	225	
Bandwidth	$T_A = 25°C$		2.0		MHz
Temperature Stability of Voltage Gain	$T_{ref} = 25°C$				
10x			±0.02	±0.25	dB
20x			±0.02	±0.25	dB
100x			±0.02	±0.25	dB
200x			±0.05	±0.50	dB

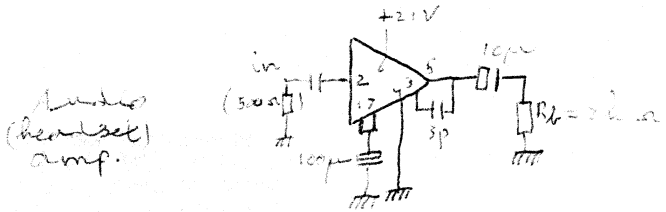
TYPICAL PERFORMANCE CURVES

VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



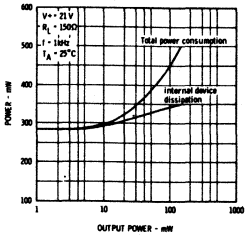
TRANSIENT RESPONSE



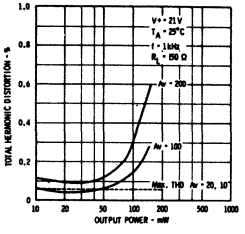


TYPICAL PERFORMANCE CURVES

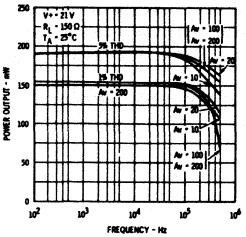
TOTAL POWER CONSUMPTION AND INTERNAL DEVICE DISSIPATION AS A FUNCTION OF OUTPUT POWER



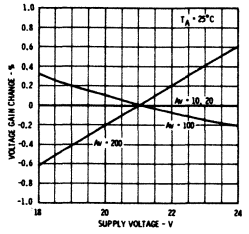
TOTAL HARMONIC DISTORTION AS A FUNCTION OF OUTPUT POWER



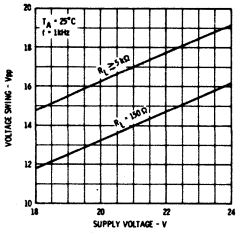
POWER OUTPUT AS A FUNCTION OF FREQUENCY 5% AND 1% THD



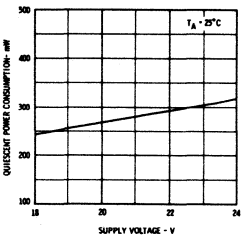
RELATIVE VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



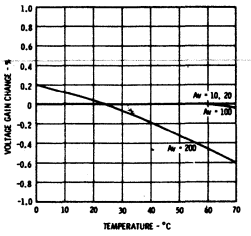
VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



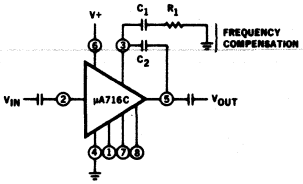
QUIESCENT POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



RELATIVE VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



CONNECTION DIAGRAM AND COMPONENT TABLE FOR AVAILABLE GAIN OPTIONS



Voltage Gain	C_1	C_2	R_1	Decouple Pins:
10	68 pF	39 pF	75 Ω	1
20	50 pF	27 pF	75 Ω	8
100	None	3 pF	None	1, 7
200	None	3 pF	None	7, 8

TABLE I

DEFINITION OF TERMS

Quiescent Power Consumption — The DC power required to operate the amplifier with no signal applied at the input and the load current equal to zero.

Total Harmonic Distortion — The ratio of the sum of the amplitudes of all signals harmonically related to the fundamental, and the amplitude of the fundamental signal.

Input Noise Voltage — The noise voltage at the output of the amplifier, divided by the amplifier voltage gain.

Output Voltage Swing — The maximum output voltage that may be obtained at the output of the amplifier before saturation occurs.

Input Resistance — The small-signal resistance seen looking into the input terminal of the amplifier.

Voltage Gain — The ratio of the small-signal output voltage to the input voltage of the amplifier.

Temperature Stability of Voltage Gain — The maximum variation of the voltage gain over the specified temperature range.

μA719
HIGH GAIN RF AMPLIFIER/FM DETECTOR
FAIRCHILD LINEAR INTEGRATED CIRCUITS

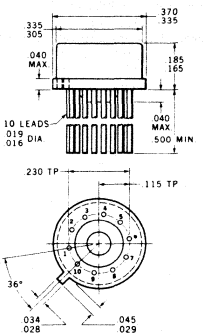
- **HIGH GAIN AT 10.7 MHz**
- **AGC RANGE > 30 dB**
- **TWO SEPARATE AMPLIFIERS**
- **SUPPLY VOLTAGE 5 TO 15 VOLTS**
- **OPTIONAL FM QUADRATURE DETECTOR**

GENERAL DESCRIPTION — The μA719 is a high gain RF amplifier/FM detector which contains two independent amplifier sections designed for IF systems to 50 MHz. Section 1 utilizes three cascaded emitter coupled amplifiers having high gain and a reverse AGC capability. In addition, Section 1 may be used as an amplifier limiter and quadrature detector for FM systems. Section 2 is a single stage amplifier useful from DC to 50 MHz.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±15 V
Output Collector Voltage (Section 1)	20 V
Voltage between "High Input 1" and "Low Input 1" Terminals	±5.0 V
Voltage between "Quad" and "Ground" Terminals	0 to +4.0 V
Voltage between "Input 2" and "Ground" Terminals	±2.0 V
Power Dissipation (Note 1)	350 mW
Maximum Chip Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 60 second time limit)	300°C

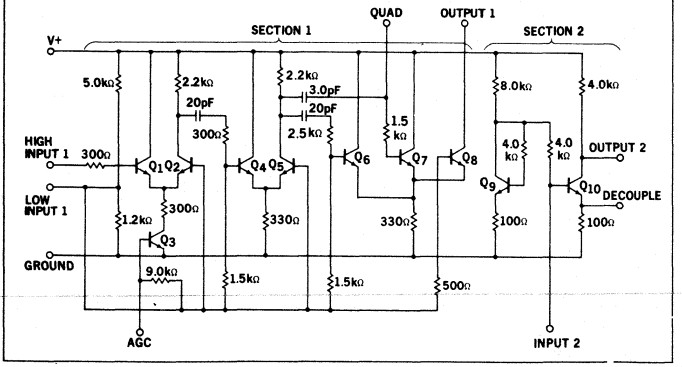
PHYSICAL DIMENSIONS
(In accordance with JEDEC TO−100)



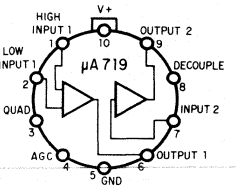
NOTES: All dimensions in inches
Leads are gold plated Kovar
Package weight is 1.02 grams

ORDER PART NO.
U5F7719312

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(TOP VIEW)



NOTE:
(1) Rating applies for ambient temperatures to +125°C if the package case to ambient thermal resistance is lowered to 40°C/Watt by the addition of a heat dissipator. Derate linearly 5.6 mW/°C for ambient temperatures above 87°C.

FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V^+ = 12$ V, Test Circuit 1 unless otherwise specified)

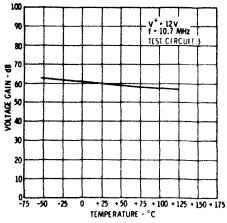
PARAMETER (See Definitions)	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current	$T_A = +25°C$	12	18	25	mA
	$T_A = -55°C$	10	17.5	27	mA
	$T_A = +125°C$*	10	17	25	mA
Supply Current	$V^+ = 9.0$ V	6.0	12.5	18.5	mA
Supply Current	$V^+ = 6.0$ V, $125°C \leq T_A \leq -55°C$	3.0	6.0	10	mA
Power Dissipation	$T_A = +25°C$	144	216	300	mW
	$T_A = -55°C$	120	210	324	mW
	$T_A = +125°C$*	120	204	300	mW
Power Dissipation	$V^+ = 9.0$ V	54	113	167	mW
Power Dissipation	$V^+ = 6.0$ V, $125°C \leq T_A \leq -55°C$	18	36	60	mW
Section 1 Quiescent Output Current		1.0	2.5	4.0	mA
Section 1 DC Voltage at AGC Terminal		0.55	0.73	1.25	V
Section 1 AGC Current For 30 dB AGC	f = 10.7 MHz, Test Circuit 3		170	250	μA
Section 1 Output Current	f = 1.0 MHz, Test Circuit 8		4.4		mA_{p-p}
Section 1 Voltage Gain	f = 10.7 MHz, Test Circuit 3				
	$T_A = +25°C$	53	60	70	dB
	$T_A = -55°C$	50	63	70	dB
	$T_A = +125°C$*	48	58	70	dB
Section 1 Voltage Gain	f = 10.7 MHz, Test Circuit 3, $V^+ = 9.0$ V		53		dB
Section 1 Voltage Gain	f = 10.7 MHz, Test Circuit 3, $V^+ = 6.0$ V		38		dB
Section 1 Input Voltage For −3.0 dB Limiting	f = 4.5 MHz, Test Circuit 4		1.5	5.5	mV
Section 1 Noise Figure	$R_S = 1.0$ kΩ, Test Circuit 5				
	f = 4.5 MHz		7.0		dB
	f = 10.7 MHz		7.0		dB
Sections 1 and 2 Cascaded Voltage Gain	f = 10.7 MHz, Test Circuit 13				
	$V^+ = 6$ V, R = 3 kΩ				
	Pin #8 Unbypassed		51		dB
	Pin #8 Bypassed		56		dB
Section 2 DC Voltage at Output 2		5.2	6.3	7.4	V
Section 2 Voltage Gain	f = 1.0 kHz, Test Circuit 2	22	31	40	dB
Section 2 Voltage at Output 2 Without Clipping	f = 1.0 kHz, Test Circuit 2	7.0	10	11.5	V_{p-p}

PARAMETERS (See Definitions)	TEST CONDITIONS	f = 4.5 MHz TYP.	f = 10.7 MHz TYP.	UNITS
SECTION 1				
Input Conductance	Test Circuit 6, $e_{IN} \leq 20$ mV	170	300	μmho
Input Capacitance	Test Circuit 6, $e_{IN} \leq 20$ mV	7.5	6.3	pF
Output Conductance	Test Circuit 7	50	130	μmho
Output Capacitance	Test Circuit 7	6.7	5.4	pF
Forward Transadmittance	Test Circuit 8	2200	1400	mmho
Forward Transadmittance	Test Circuit 8, $V^+ = 9.0$ V	1000	600	mmho
Forward Transadmittance	Test Circuit 8, $V^+ = 6.0$ V	180	100	mmho
Quad Conductance	Test Circuit 9	200	330	μmho
Quad Capacitance	Test Circuit 9	8.0	7.0	pF
Gain Maximum Available (GMA)	Test Circuit 5	83	71	dB
Gain Maximum Stable (GMS)	Test Circuit 5	85	78	dB
SECTION 2				
Input Conductance	Test Circuit 10			
	Pin #8 Unbypassed	300	300	μmho
	Pin #8 Bypassed	360	460	μmho
Input Capacitance	Test Circuit 10			
	Pin #8 Unbypassed	3.3	3.3	pF
	Pin #8 Bypassed	10.4	8.7	pF
Output Conductance	Test Circuit 11			
	Pin #8 Unbypassed	250	260	μmho
	Pin #8 Bypassed	270	340	μmho
Output Capacitance	Test Circuit 11			
	Pin #8 Unbypassed	5.2	5.2	pF
	Pin #8 Bypassed	8.9	8.0	pF
Forward Transadmittance	Test Circuit 12			
	Pin #8 Unbypassed	8.0	8.0	mmho
	Pin #8 Bypassed	34	34	mmho
Gain Maximum Available (GMA)	Pin #8 Unbypassed	24	24	dB
	Pin #8 Bypassed	35	32	dB

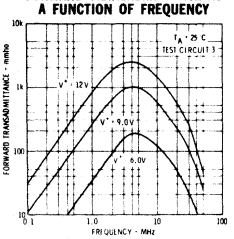
*NOTE 2: Test to be performed with a heat dissipator of not greater than 40°C/Watt case to ambient thermal resistance.

TYPICAL PERFORMANCE CURVES

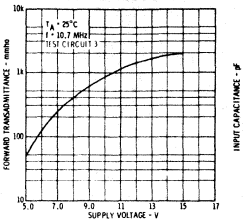
SECTION 1
VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



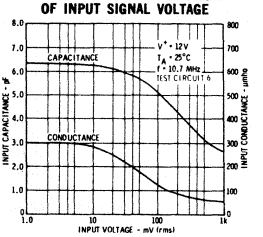
SECTION 1
FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



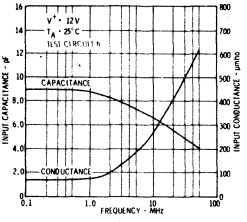
SECTION 1
FORWARD TRANSADMITTANCE AS A FUNCTION OF SUPPLY VOLTAGE



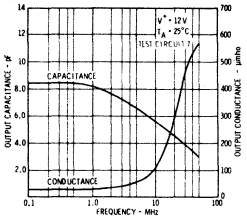
SECTION 1
INPUT CAPACITANCE AND CONDUCTANCE AS A FUNCTION OF INPUT SIGNAL VOLTAGE



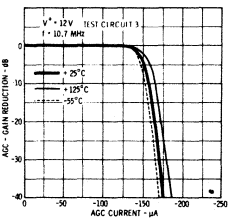
SECTION 1
INPUT CAPACITANCE AND CONDUCTANCE AS A FUNCTION OF FREQUENCY



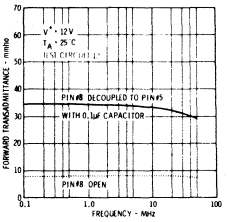
SECTION 1
OUTPUT CAPACITANCE AND CONDUCTANCE AS A FUNCTION OF FREQUENCY



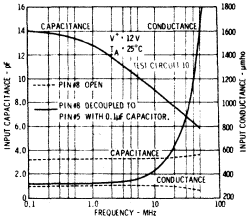
SECTION 1
AGC AS A FUNCTION OF AGC CURRENT



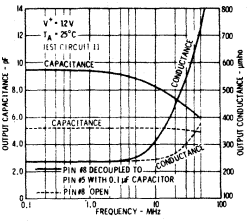
SECTION 2
FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



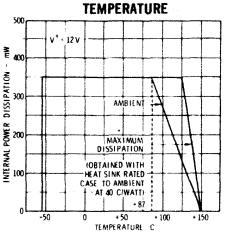
SECTION 2
INPUT CAPACITANCE AND CONDUCTANCE AS A FUNCTION OF FREQUENCY



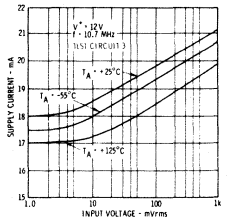
SECTION 2
OUTPUT CAPACITANCE AND CONDUCTANCE AS A FUNCTION OF FREQUENCY



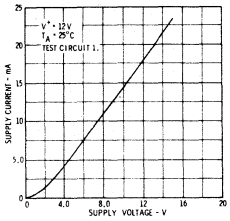
SECTIONS 1 AND 2
MAXIMUM INTERNAL DISSIPATION AS A FUNCTION OF TEMPERATURE



SECTIONS 1 AND 2
SUPPLY CURRENT AS A FUNCTION OF INPUT 1 SIGNAL VOLTAGE

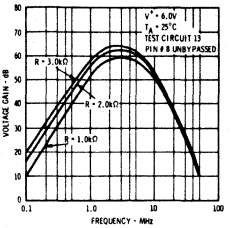


SECTIONS 1 AND 2
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

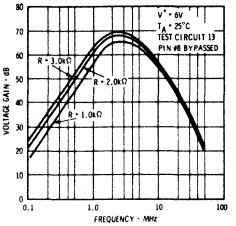


TYPICAL PERFORMANCE CURVES

SECTIONS 1 AND 2 CASCADED VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



SECTIONS 1 AND 2 CASCADED VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



DEFINITION OF TERMS

Gain Maximum Available (GMA) — This gain figure is the theoretical maximum power gain of an amplifier with conjugate matching at both the input and the output terminals and assumes no reverse transadmittance (feedback component) in the amplifier.

$$GMA = \frac{|\text{forward transadmittance}|^2}{4 \times \text{input conductance} \times \text{output conductance}}$$

Gain Maximum Stable (GMS) — This gain figure gives the maximum possible gain based on stability criteria only. This gain figure does not necessarily represent the realizable power gain of an amplifier. For unneutralized amplifiers, the maximum power gain realizable based on normal circuit tolerances is either (GMS - 6.0 dB) or GMA, whichever is smaller.

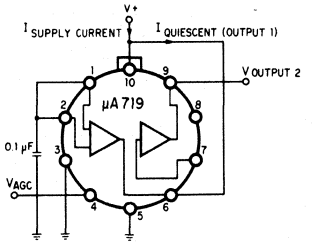
$$GMS = \frac{|\text{forward transadmittance}|}{|\text{reverse transadmittance}|}$$

Input Voltage For —3.0 dB Limiting — Refer to Test Circuit 4 which shows the μA719 being used as an amplifier, limiter, and FM detector (simple quadrature type with the LC tank circuit connected between pins No. 3 and No. 2). An input FM signal (carrier frequency 4.5 MHz, ±25 kHz deviation at 400 Hz) of 50 mV rms is applied to the μA719 and the value of the recovered audio output signal (400 Hz) at pin No. 6 is noted. The —3.0 dB input limiting voltage is defined as the value of the input voltage to produce an output voltage 3dB below the output level obtained with 50 mV rms of input signal.

TEST CIRCUITS

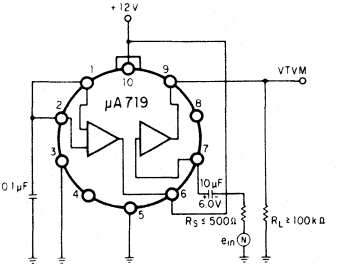
TEST CIRCUIT 1

DC MEASUREMENTS



TEST CIRCUIT 2

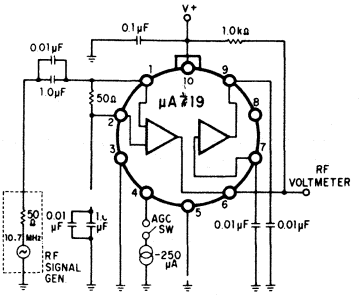
SECTION 2 GAIN AND OUTPUT VOLTAGE SWING



TEST CIRCUITS

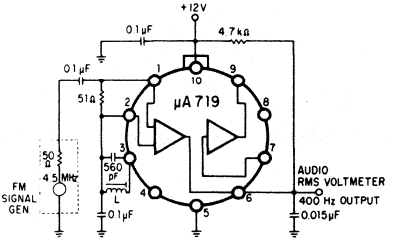
TEST CIRCUIT 3

10.7 MHz VOLTAGE GAIN AND AGC



TEST CIRCUIT 4

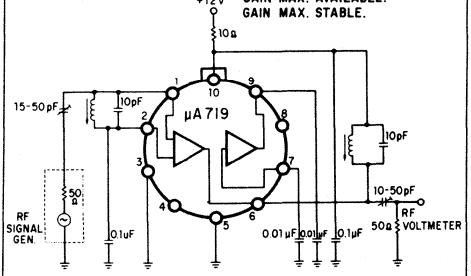
-3.0 dB LIMITING AT 4.5 MHz USING A QUADRATURE DETECTOR*



INPUT SIGNAL 4.5 MHz 25kHz DEVIATION AT 400Hz UNLOADED QUALITY FACTOR OF QUADRATURE TANK INDUCTOR IS 22.
*SEE DEFINITIONS

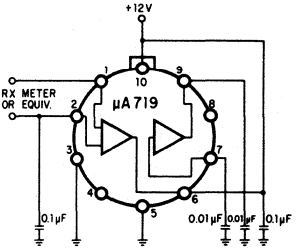
TEST CIRCUIT 5

SECTION 1: NOISE FIGURE.
GAIN MAX. AVAILABLE.
GAIN MAX. STABLE.



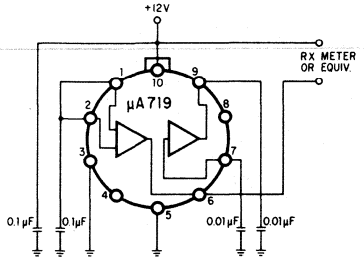
TEST CIRCUIT 6

SECTION 1 INPUT PARAMETERS



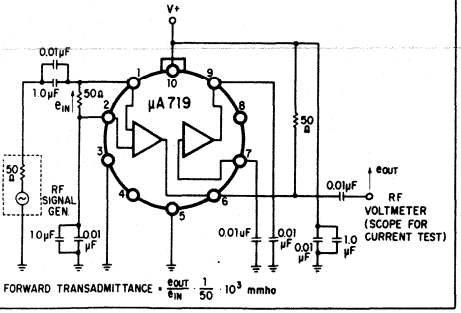
TEST CIRCUIT 7

SECTION 1 OUTPUT PARAMETERS



TEST CIRCUIT 8

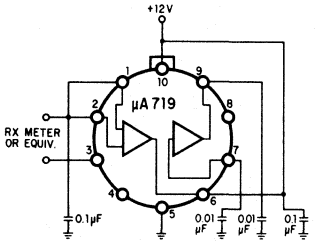
SECTION 1 FORWARD TRANSADMITTANCE OUTPUT CURRENT



FORWARD TRANSADMITTANCE = $\frac{e_{OUT}}{e_{IN}} \cdot \frac{1}{50} \cdot 10^3$ mmho

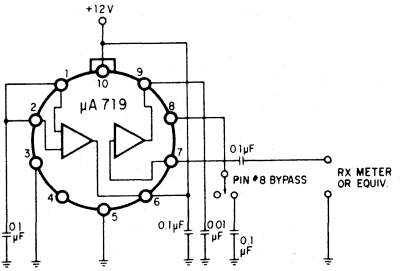
TEST CIRCUIT 9

SECTION 1 QUAD PARAMETERS



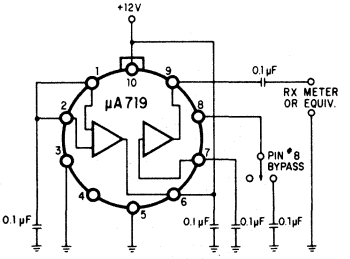
TEST CIRCUIT 10

SECTION 2 INPUT PARAMETERS



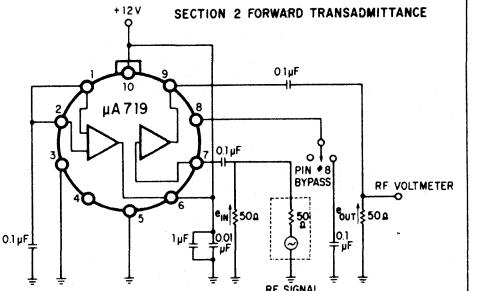
TEST CIRCUIT 11

SECTION 2 OUTPUT PARAMETERS



TEST CIRCUIT 12

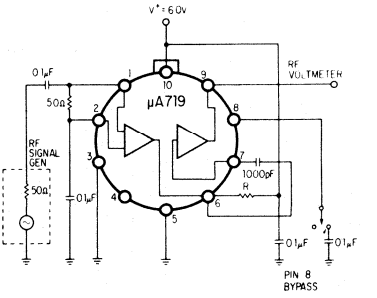
SECTION 2 FORWARD TRANSADMITTANCE



FORWARD TRANSADMITTANCE = $\frac{e_{OUT}}{e_{IN}} \cdot \frac{1}{50} \cdot 10^3$ mmho

TEST CIRCUIT 13

SECTION 1 AND 2 CASCADED VOLTAGE GAIN



μA719C
HIGH GAIN RF AMPLIFIER/FM DETECTOR
FAIRCHILD LINEAR INTEGRATED CIRCUITS

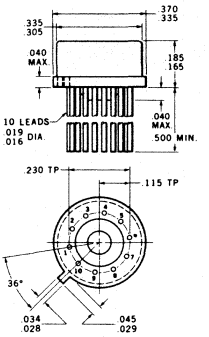
- **HIGH GAIN AT 10.7 MHz**
- **AGC RANGE > 30 dB**
- **TWO SEPARATE AMPLIFIERS**
- **SUPPLY VOLTAGE 5 TO 15 VOLTS**
- **OPTIONAL FM QUADRATURE DETECTOR**

GENERAL DESCRIPTION — The μA719C is a high gain RF amplifier/FM detector which contains two independent amplifier sections designed for IF systems to 50 MHz. Section 1 utilizes three cascaded emitter coupled amplifiers having high gain and a reverse AGC capability. In addition, Section 1 may be used as an amplifier limiter and quadrature detector for FM systems. Section 2 is a single stage amplifier useful from DC to 50 MHz.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	15 V
Output Collector Voltage (Section 1)	20 V
Voltage between "High Input 1" and "Low Input 1" Terminals	±5.0 V
Voltage between "Quad" and "Ground" Terminals	0 to +4.0 V
Voltage between "Input 2" and "Ground" Terminals	±2.0 V
Power Dissipation	350 mW
Maximum Chip Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 60 second time limit)	300°C

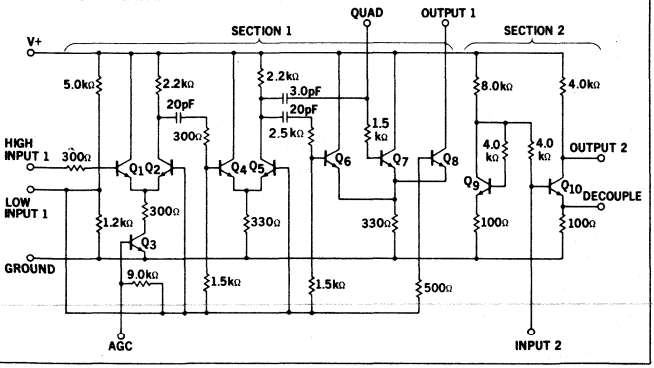
PHYSICAL DIMENSIONS
(In accordance with JEDEC TO-100)



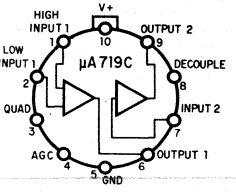
NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.02 grams

ORDER PART NO.
U5F7719393

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(TOP VIEW)



FAIRCHILD
SEMICONDUCTOR

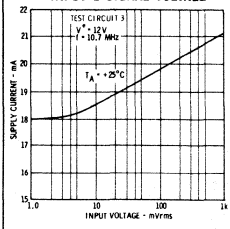
ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V^+ = 12$ V, Test Circuit 1 unless otherwise specified)

PARAMETER (See Definitions)	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current	$T_A = +25°C$	12	18	25	mA
	$T_A = 0°C$	10	17.5	27	mA
	$T_A = +70°C$	10	17	25	mA
Supply Current	$V^+ = 9.0$ V	6.0	12.5	18.5	mA
Supply Current	$V^+ = 6.0$ V, $70°C \leq T_A \leq 0°C$	3.0	6.0	10	mA
Power Dissipation	$T_A = +25°C$	144	216	300	mW
	$T_A = 0°C$	120	210	324	mW
	$T_A = +70°C$	120	204	300	mW
Power Dissipation	$V^+ = 9.0$ V	54	113	167	mW
Power Dissipation	$V^+ = 6.0$ V, $70°C \leq T_A \leq 0°C$	18	36	60	mW
Section 1 Quiescent Output Current		1.0	2.5	4.0	mA
Section 1 DC Voltage at AGC Terminal		0.55	0.73	1.25	V
Section 1 AGC Current For 30 dB AGC	f = 10.7 MHz, Test Circuit 3		170	250	μA
Section 1 Output Current	f = 1.0 MHz, Test Circuit 8		4.4		mA_{p-p}
Section 1 Voltage Gain	f = 10.7 MHz, Test Circuit 3				
	$T_A = +25°C$	50	60	70	dB
	$T_A = 0°C$	50	61	70	dB
	$T_A = +70°C$	48	59	70	dB
Section 1 Voltage Gain	f = 10.7 MHz, Test Circuit 3, $V^+ = 9.0$ V		53		dB
Section 1 Voltage Gain	f = 10.7 MHz, Test Circuit 3, $V^+ = 6.0$ V		38		dB
Section 1 Input Voltage For −3.0 dB Limiting	f = 4.5 MHz, Test Circuit 4		1.5	6.5	mV
Section 1 Noise Figure	$R_S = 1.0$ kΩ, Test Circuit 5				
	f = 4.5 MHz		7.0		dB
	f = 10.7 MHz		7.0		dB
Sections 1 and 2 Cascaded Voltage Gain	f = 10.7 MHz, Test Circuit 13				
	$V^+ = 6.0$ V, R = 3.0 kΩ				
	Pin #8 Unbypassed		51		dB
	Pin #8 Bypassed		56		dB
Section 2 DC Voltage at Output 2		5.2	6.3	7.4	V
Section 2 Voltage Gain	f = 1.0 kHz, Test Circuit 2	22	31	40	dB
Section 2 Voltage at Output 2 Without Clipping	f = 1.0 kHz, Test Circuit 2	7.0	10	11.5	V_{p-p}

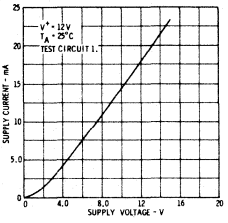
PARAMETERS (See Definitions)	TEST CONDITIONS	f = 4.5 MHz TYP.	f = 10.7 MHz TYP.	UNITS
SECTION 1				
Input Conductance	Test Circuit 6, $e_{IN} \leq 20$ mV	170	300	μmho
Input Capacitance	Test Circuit 6, $e_{IN} \leq 20$ mV	7.5	6.3	pF
Output Conductance	Test Circuit 7	50	130	μmho
Output Capacitance	Test Circuit 7	6.7	5.4	pF
Forward Transadmittance	Test Circuit 8	2200	1400	mmho
Forward Transadmittance	Test Circuit 8, $V^+ = 9.0$ V	1000	600	mmho
Forward Transadmittance	Test Circuit 8, $V^+ = 6.0$ V	180	100	mmho
Quad Conductance	Test Circuit 9	200	330	μmho
Quad Capacitance	Test Circuit 9	8.0	7.0	pF
Gain Maximum Available (GMA)	Test Circuit 5	83	71	dB
Gain Maximum Stable (GMS)	Test Circuit 5	85	78	dB
SECTION 2				
Input Conductance	Test Circuit 10			
	Pin #8 Unbypassed	300	300	μmho
	Pin #8 Bypassed	360	460	μmho
Input Capacitance	Test Circuit 10			
	Pin #8 Unbypassed	3.3	3.3	pF
	Pin #8 Bypassed	10.4	8.7	pF
Output Conductance	Test Circuit 11			
	Pin #8 Unbypassed	250	260	μmho
	Pin #8 Bypassed	270	340	μmho
Output Capacitance	Test Circuit 11			
	Pin #8 Unbypassed	5.2	5.2	pF
	Pin #8 Bypassed	8.9	8.0	pF
Forward Transadmittance	Test Circuit 12			
	Pin #8 Unbypassed	8.0	8.0	mmho
	Pin #8 Bypassed	34	34	mmho
Gain Maximum Available (GMA)	Pin #8 Unbypassed	24	24	dB
	Pin #8 Bypassed	35	32	dB

TYPICAL PERFORMANCE CURVES

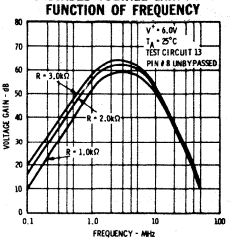
SECTIONS 1 AND 2 SUPPLY CURRENT AS A FUNCTION OF INPUT 1 SIGNAL VOLTAGE



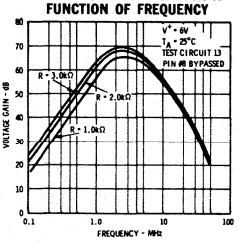
SECTIONS 1 AND 2 SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



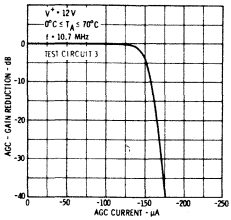
SECTIONS 1 AND 2 CASCADED VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



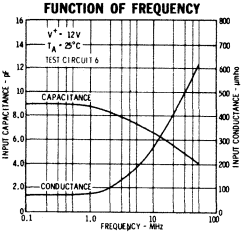
SECTIONS 1 AND 2 CASCADED VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



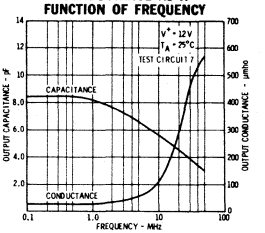
SECTION 1 AGC AS A FUNCTION OF AGC CURRENT



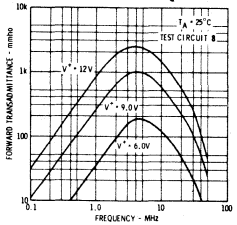
SECTION 1 INPUT CAPACITANCE AND CONDUCTANCE AS A FUNCTION OF FREQUENCY



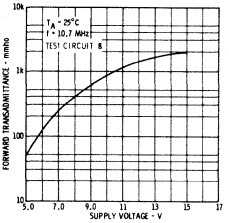
SECTION 1 OUTPUT CAPACITANCE AND CONDUCTANCE AS A FUNCTION OF FREQUENCY



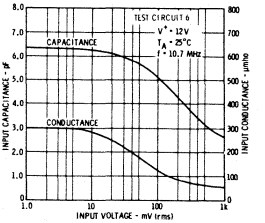
SECTION 1 FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



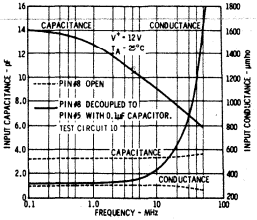
SECTION 1 FORWARD TRANSADMITTANCE AS A FUNCTION OF SUPPLY VOLTAGE



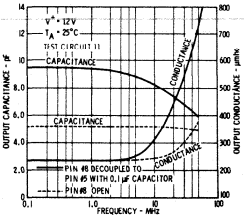
SECTION 1 INPUT CAPACITANCE AND CONDUCTANCE AS A FUNCTION OF INPUT SIGNAL VOLTAGE



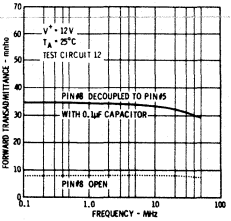
SECTION 2 INPUT CAPACITANCE AND CONDUCTANCE AS A FUNCTION OF FREQUENCY



SECTION 2 OUTPUT CAPACITANCE AND CONDUCTANCE AS A FUNCTION OF FREQUENCY



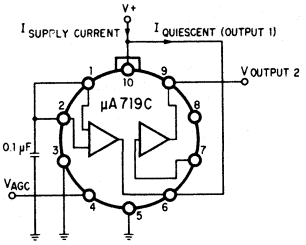
SECTION 2 FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



TEST CIRCUITS

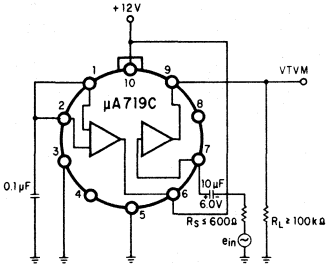
TEST CIRCUIT 1

DC MEASUREMENTS



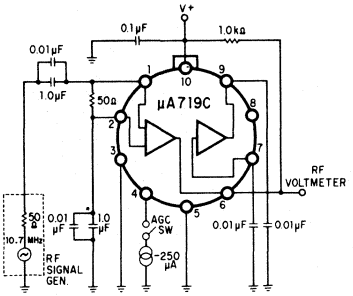
TEST CIRCUIT 2

SECTION 2 GAIN AND OUTPUT VOLTAGE SWING



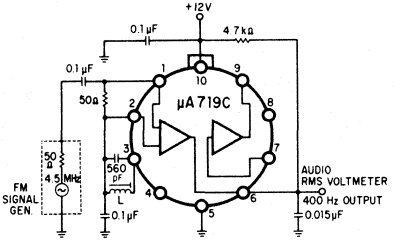
TEST CIRCUIT 3

10.7 MHz VOLTAGE GAIN AND AGC



TEST CIRCUIT 4

-3.0dB LIMITING AT 4.5 MHz USING A QUADRATURE DETECTOR*

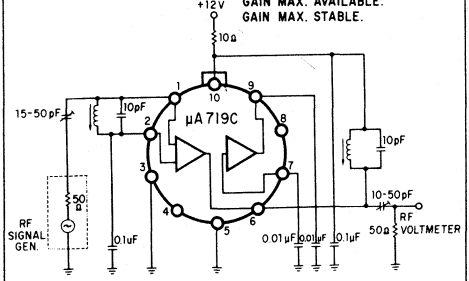


INPUT SIGNAL 4.5 MHz 25kHz DEVIATION AT 400 Hz UNLOADED QUALITY FACTOR OF QUADRATURE TANK INDUCTOR IS 22

*SEE DEFINITIONS

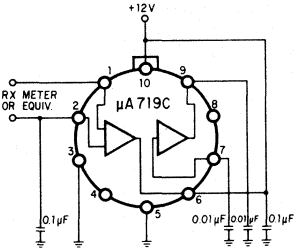
TEST CIRCUIT 5

SECTION 1: NOISE FIGURE.
GAIN MAX. AVAILABLE.
GAIN MAX. STABLE.



TEST CIRCUIT 6

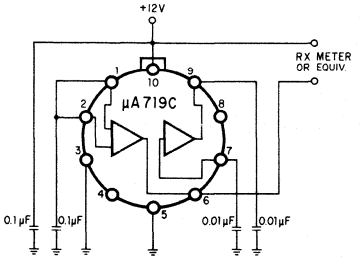
SECTION 1 INPUT PARAMETERS



TEST CIRCUITS

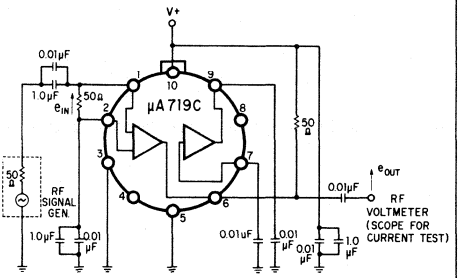
TEST CIRCUIT 7

SECTION 1 OUTPUT PARAMETERS



TEST CIRCUIT 8

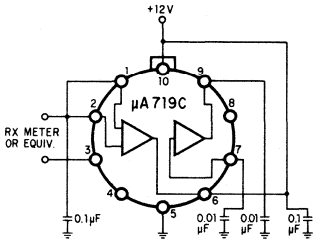
SECTION 1 FORWARD TRANSADMITTANCE OUTPUT CURRENT



FORWARD TRANSADMITTANCE = $\frac{e_{OUT}}{e_{IN}} \cdot \frac{1}{50} \cdot 10^3$ mmho

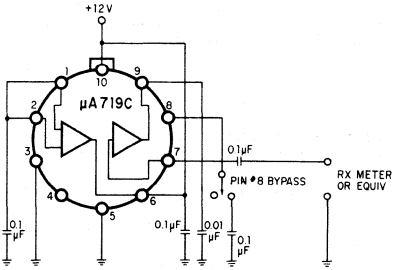
TEST CIRCUIT 9

SECTION 1 QUAD PARAMETERS



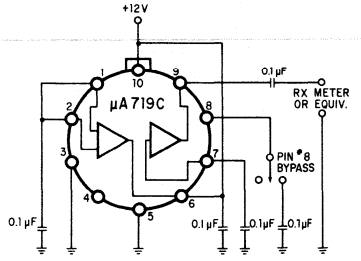
TEST CIRCUIT 10

SECTION 2 INPUT PARAMETERS



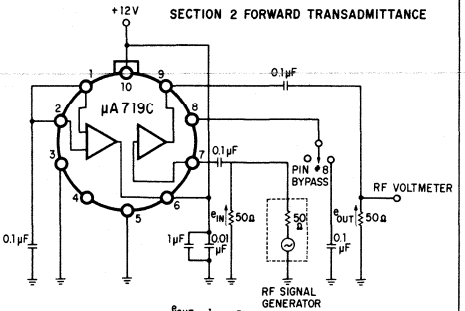
TEST CIRCUIT 11

SECTION 2 OUTPUT PARAMETERS



TEST CIRCUIT 12

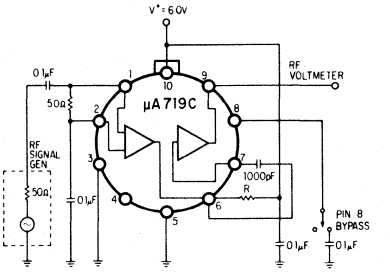
SECTION 2 FORWARD TRANSADMITTANCE



FORWARD TRANSADMITTANCE = $\frac{e_{OUT}}{e_{IN}} \cdot \frac{1}{50} \cdot 10^3$ mmho

TEST CIRCUIT 13

SECTION 1 AND 2 CASCADED VOLTAGE GAIN



DEFINITION OF TERMS

Gain Maximum Available (GMA) — This gain figure is the theoretical maximum power gain of an amplifier with conjugate matching at both the input and the output terminals and assumes no reverse transadmittance (feedback component) in the amplifier.

$$GMA = \frac{|\text{forward transadmittance}|^2}{4 \times \text{input conductance} \times \text{output conductance}}$$

Gain Maximum Stable (GMS) — This gain figure gives the maximum possible gain based on stability criteria only. This gain figure does not necessarily represent the realizable power gain of an amplifier. For unneutralized amplifiers, the maximum power gain realizable based on normal circuit tolerances is either (GMS - 6.0 dB) or GMA, whichever is smaller.

$$GMS = \frac{|\text{forward transadmittance}|}{|\text{reverse transadmittance}|}$$

Input Voltage For −3.0 dB Limiting — Refer to Test Circuit 4 which shows the μA719C being used as an amplifier, limiter, and FM detector (simple quadrature type with the LC tank circuit connected between pins No. 3 and No. 2). An input FM signal (carrier frequency 4.5 MHz, ±25 kHz deviation at 400 Hz) of 50 mV rms is applied to the μA719C and the value of the recovered audio output signal (400 Hz) at pin No. 6 is noted. The −3.0 dB input limiting voltage is defined as the value of the input voltage to produce an output voltage 3dB below the output level obtained with 50 mV rms of input signal.

μA722
10-BIT CURRENT SOURCE
FAIRCHILD LINEAR INTEGRATED CIRCUITS

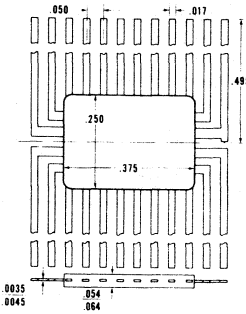
- **8 ± ½ BIT ACCURACY FROM 0°C TO +55°C**
- **7±½ BIT ACCURACY FROM −20°C TO +85°C**
- **600 ns SWITCHING SPEED**
- **INTERNAL PRECISION REFERENCE**
- **CCSL COMPATIBLE**

GENERAL DESCRIPTION — The μA722 is a high-speed, 10-bit precision current source intended for use in current-summing digital-to-analog converters or as the feedback element in successive approximation analog-to-digital converters. It is constructed on a single silicon chip, using the Fairchild Planar* epitaxial process, and consists of a reference supply, 10 current sources connected to a single output summing line, and associated logic switches. The full-scale current and coding format are set by an external resistor array, which may be preselected and fixed for general usage or trimmed for greater accuracy. The μA722 is compatible with the Fairchild families of linear and digital circuits.

ABSOLUTE MAXIMUM RATINGS

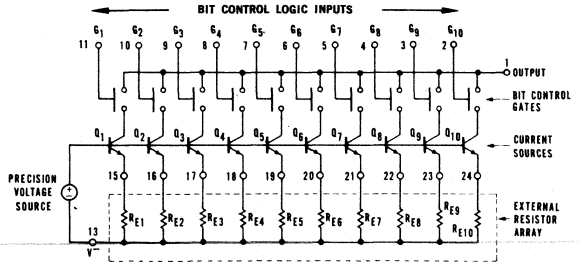
Voltage from V^+ to V^-	−0.5 V to +18 V
Voltage from Output to V^+	−12 V to +6 V
Voltage from Output to V^-	0 V to +12 V
Voltage from Logic Inputs to Output	−9 V to +7 V
Voltage from Logic Inputs to V^+	−18 V to 0 V
Voltage from Logic Inputs to V^-	0 V to +12 V
Internal Power Dissipation (Note 1)	450 mW
Operating Temperature Range	−20°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

PHYSICAL DIMENSIONS
(TYPICAL FLAT PACKAGE)
(TOP VIEW)

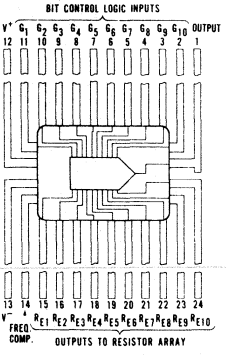


ORDER PART NO. U3M7722333

EQUIVALENT CIRCUIT



CONNECTION DIAGRAM
(TOP VIEW)



NOTE: PIN 13 INTERNALLY CONNECTED TO CASE.

Notes on Page 2

*Planar is a patented Fairchild process.

FAIRCHILD SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS

PARAMETER (See Definitions)	CONDITIONS (Note 2)	MIN.	TYP.	MAX.	UNITS
Resolution				10	Bits
Absolute Error	$T_A = 25°C$		±.07	±.20	%
	$0°C \leq T_A \leq +55°C$		±.10	±.20	%
	$-20°C \leq T_A \leq +85°C$		±.13	±.39	%
Output Current					
Full-Scale	Logic Inputs = 0.4 V	2160	2560	3000	μA
Zero-Scale	Logic Inputs = 2.5 V		±.002	±.25	μA
Power Supply Rejection	$\Delta V' = \Delta V = \pm 5\%$		±.06	±0.1	%/%
Output Resistance		0.2	1.2		MΩ
Switching Speed			600		ns
Logic Input High Voltage		2.1	2.5		V
Logic Input Low Voltage			0.4	0.7	V
Power Consumption			165	250	mW

NOTES:

(1) Rating applies for ambient temperatures to +85°C.
(2) Unless otherwise specified, $T_A = 25°C$, $V' = 6.0$ V ±.01 V, V = −6.0 V ±.01 V, $V_{Out} = 0$ V, $C_1 = 200$ pF, and external resistor array as per Table 1.
(3) In Table 1, the maximum absolute value tolerance for $R_{E1} = \pm 10\%$.

TYPICAL FULL-SCALE OUTPUT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

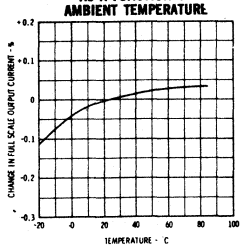
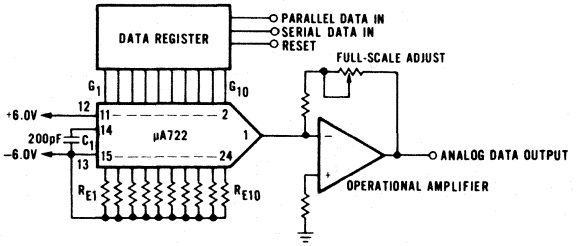


TABLE 1

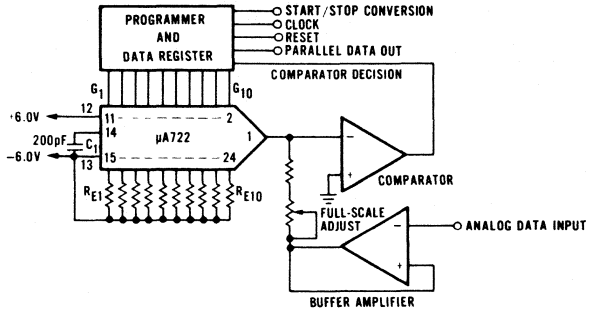
BINARY CODE RESISTOR ARRAY FOR 8 ± ½ BIT ACCURACY

Resistor Number (R_{Ej})	Nominal Value (kΩ)	Nominal Ratio (R_{Ej}/R_{E1})	Max. Ratio Tolerance ($T_A = 25°C$) (%)	Max. Ratio Temp. Coeff. (ppm/°C)
R_{E1}	2.547	1.000	Note 3	±5
R_{E2}	5.094	2.000	±0.02	±5
R_{E3}	10.245	4.022	±0.05	±10
R_{E4}	20.60	8.088	±0.10	±20
R_{E5}	41.43	16.265	±0.20	±20
R_{E6}	81.93	32.17	±0.20	±50
R_{E7}	163.4	64.16	±0.50	±100
R_{E8}	325.7	127.9	±1.0	±200
R_{E9}	644.9	253.2	±2.0	±500
R_{E10}	1275	500.8	±2.0	±500

TYPICAL DIGITAL-TO-ANALOG CONVERTER



TYPICAL ANALOG-TO-DIGITAL CONVERTER



DEFINITION OF TERMS

FULL SCALE OUTPUT CURRENT — The output current for all bits turned on.

ZERO SCALE OUTPUT CURRENT — The output current for all bits turned off.

ABSOLUTE ERROR — The worst-case deviation from a straight line drawn through zero and the 25°C value of the full-scale output current.

POWER SUPPLY REJECTION — The ratio of the percentage change in full-scale output current to the percentage change in supply voltage producing it.

OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the output at virtual ground and all bits turned on.

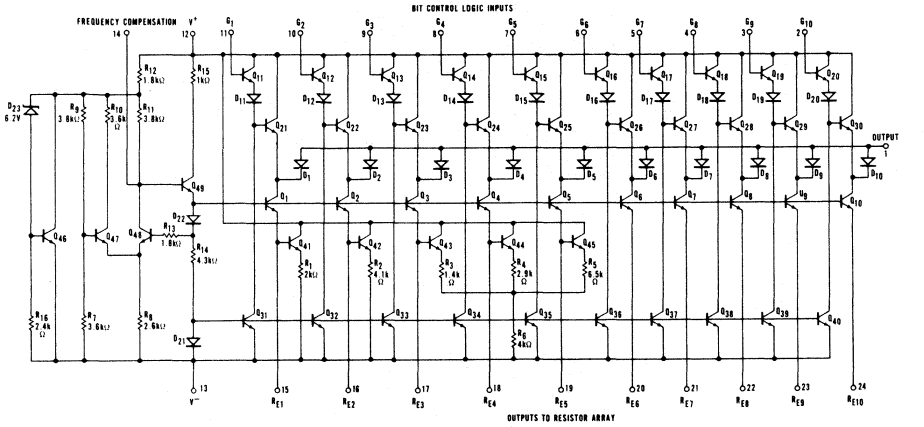
SWITCHING SPEED — The time required to turn on the least significant bit.

LOGIC INPUT HIGH VOLTAGE — The minimum voltage allowed at a bit control gate to hold the bit off.

LOGIC INPUT LOW VOLTAGE — The maximum voltage allowed at a bit control gate to hold the bit on.

POWER CONSUMPTION — The DC power required to operate the device; the power will vary with logic condition, but is specified as a maximum for the entire range of signal conditions.

SCHEMATIC DIAGRAM



μA722B
10-BIT CURRENT SOURCE
FAIRCHILD LINEAR INTEGRATED CIRCUITS

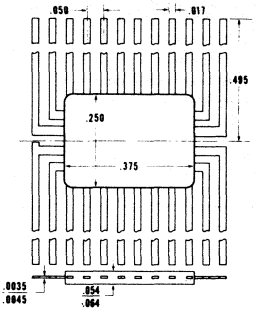
- 7 ±½ BIT ACCURACY FROM 0°C TO +55°C
- 6 ± ½ BIT ACCURACY FROM −20°C TO +85°C
- 600 ns SWITCHING SPEED
- INTERNAL PRECISION REFERENCE
- CCSL COMPATIBLE

GENERAL DESCRIPTION — The μA722B is a high-speed, 10-bit precision current source intended for use in current-summing digital-to-analog converters or as the feedback element in successive approximation analog-to-digital converters. It is constructed on a single silicon chip, using the Fairchild Planar* epitaxial process, and consists of a reference supply, 10 current sources connected to a single output summing line, and associated logic switches. The full-scale current and coding format are set by an external resistor array, which may be preselected and fixed for general usage or trimmed for greater accuracy. The μA722B is compatible with the Fairchild families of linear and digital circuits. For higher accuracy, see μA722 data sheet.

ABSOLUTE MAXIMUM RATINGS

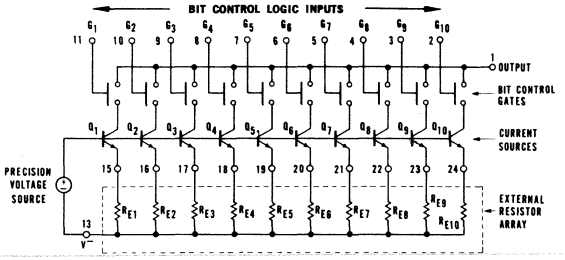
Voltage from V^+ to V^-	−0.5 V to +18 V
Voltage from Output to V^+	−12 V to +6 V
Voltage from Output to V^-	0 V to +12 V
Voltage from Logic Inputs to Output	−9 V to +7 V
Voltage from Logic Inputs to V^+	−18 V to 0 V
Voltage from Logic Inputs to V^-	0 V to +12 V
Internal Power Dissipation (Note 1)	450 mW
Operating Temperature Range	−20°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

PHYSICAL DIMENSIONS
(TYPICAL FLAT PACKAGE)
(TOP VIEW)

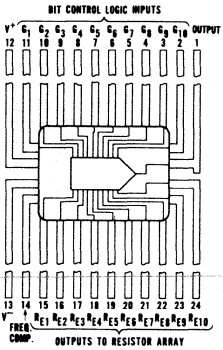


ORDER PART NO. U3M7722334

EQUIVALENT CIRCUIT



CONNECTION DIAGRAM
(TOP VIEW)



NOTE: PIN 13 INTERNALLY CONNECTED TO CASE.

Notes on Page 2

*Planar is a patented Fairchild process.

FAIRCHILD SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS

PARAMETER (See Definitions)	CONDITIONS (Note 2)	MIN.	TYP.	MAX.	UNITS
Resolution				10	Bits
Absolute Error	$T_A = 25°C$		±.08	±.39	%
	$0°C \leq T_A \leq +55°C$		±.17	±.39	%
	$-20°C \leq T_A \leq +85°C$		±.22	±.78	%
Output Current					
Full-Scale	Logic Inputs = 0.4 V	2160	2560	3000	μA
Zero-Scale	Logic Inputs = 2.5 V		±.002	±.25	μA
Power Supply Rejection	$\Delta V^+ = \Delta V^- = \pm 5\%$		±.06	±0.1	%/%
Output Resistance		0.2	1.2		MΩ
Switching Speed			600		ns
Logic Input High Voltage		2.1	2.5		V
Logic Input Low Voltage			0.4	0.7	V
Power Consumption			165	250	mW

NOTES:

(1) Rating applies for ambient temperatures to +85°C.
(2) Unless otherwise specified, $T_A = 25°C$, $V^+ = 6.00\ V \pm .01\ V$, $V^- = -6.00\ V \pm .01\ V$, $V_{out} = 0\ V$, $C_L = 200\ pF$, and external resistor array as per Table 1.
(3) In Table 1, the maximum absolute value tolerance for $R_{E1} = \pm 10\%$.

TYPICAL FULL-SCALE OUTPUT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

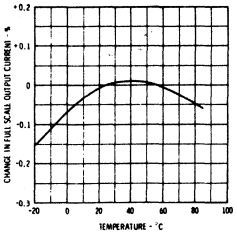
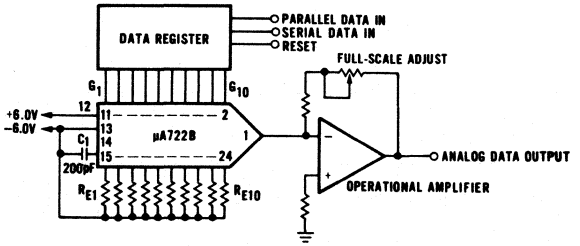


TABLE 1

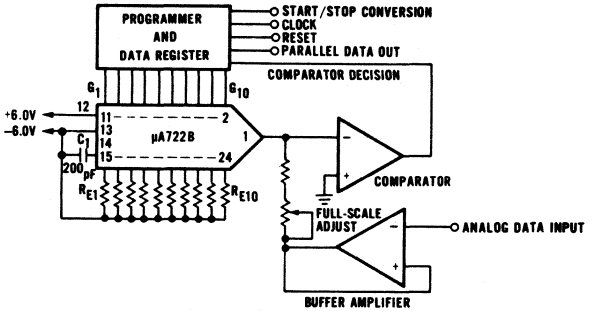
BINARY CODE RESISTOR ARRAY FOR 6 ± ½ BIT ACCURACY

Resistor Number (R_{Ej})	Nominal Value (kΩ)	Nominal Ratio (R_{Ej}/R_{E1})	Max. Ratio Tolerance ($T_A = 25°C$) (%)	Max. Ratio Temp. Coeff. (ppm/°C)
R_{E1}	2.547	1.000	Note 3	±20
R_{E2}	5.094	2.000	±0.10	±20
R_{E3}	10.245	4.022	±0.20	±50
R_{E4}	20.60	8.088	±0.20	±50
R_{E5}	41.43	16.265	±0.50	±100
R_{E6}	81.93	32.17	±0.50	±100
R_{E7}	163.4	64.16	±1.0	±500
R_{E8}	325.7	127.9	±1.0	±500
R_{E9}	644.9	253.2	±5.0	±1000
R_{E10}	1275	500.8	±5.0	±1000

TYPICAL DIGITAL-TO-ANALOG CONVERTER



TYPICAL ANALOG-TO-DIGITAL CONVERTER



DEFINITION OF TERMS

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ZERO SCALE OUTPUT CURRENT — The output current for all bits turned off.

ABSOLUTE ERROR — The worst-case deviation from a straight line drawn through zero and the 25°C value of the full-scale output current.

POWER SUPPLY REJECTION — The ratio of the percentage change in full-scale output current to the percentage change in supply voltage producing it.

OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the output at virtual ground and all bits turned on.

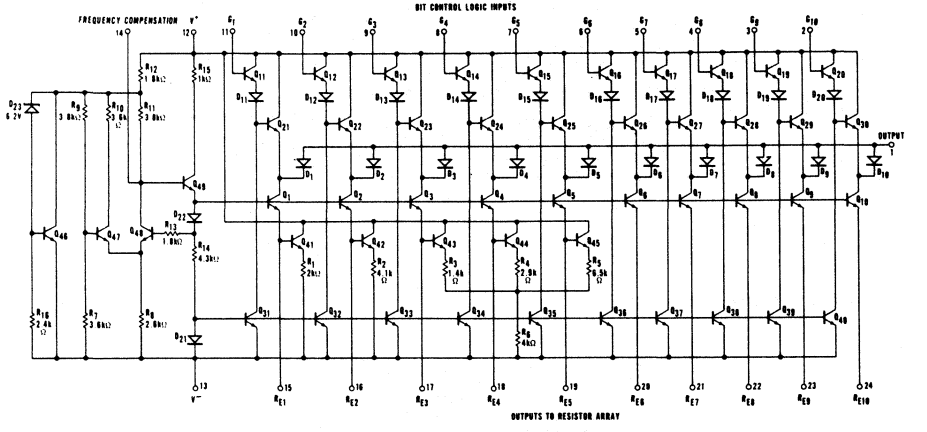
SWITCHING SPEED — The time required to turn on the least significant bit.

LOGIC INPUT HIGH VOLTAGE — The minimum voltage allowed at a bit control gate to hold the bit off.

LOGIC INPUT LOW VOLTAGE — The maximum voltage allowed at a bit control gate to hold the bit on.

POWER CONSUMPTION — The DC power required to operate the device; the power will vary with logic condition, but is specified as a maximum for the entire range of signal conditions.

SCHEMATIC DIAGRAM



μA723
PRECISION VOLTAGE REGULATOR
FAIRCHILD LINEAR INTEGRATED CIRCUITS

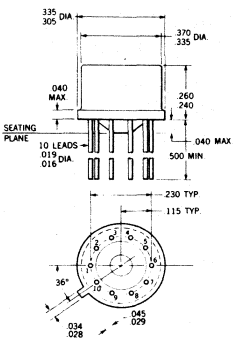
- **POSITIVE OR NEGATIVE SUPPLY OPERATION**
- **SERIES, SHUNT, SWITCHING OR FLOATING OPERATION**
- **.01% LINE AND LOAD REGULATION**
- **OUTPUT VOLTAGE ADJUSTABLE FROM 2 TO 37 VOLTS**
- **OUTPUT CURRENT TO 150 mA WITHOUT EXTERNAL PASS TRANSISTOR**

GENERAL DESCRIPTION — The μA723 is a monolithic voltage regulator constructed on a single silicon chip using the Fairchild Planar® epitaxial process. The device consists of a temperature compensated reference amplifier, error amplifier, power series pass transistor and current limit circuitry. Additional NPN or PNP pass elements may be used when output currents exceeding 150 mA are required. Provisions are made for adjustable current limiting and remote shutdown. In addition to the above, the device features low standby current drain, low temperature drift and high ripple rejection. The μA723 is intended for use with positive or negative supplies as a series, shunt, switching or floating regulator. Applications include laboratory power supplies, isolation regulators for low level data amplifiers, logic card regulators, small instrument power supplies, airborne systems and other power supplies for digital and linear circuits.

ABSOLUTE MAXIMUM RATINGS

Pulse Voltage from V^+ to V^- (50 msec)	50 V
Continuous Voltage from V^+ to V^-	40 V
Input-Output Voltage Differential	40 V
Maximum Output Current	150 mA
Current from V_{REF}	15 mA
Internal Power Dissipation (Note 1)	800 mW
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

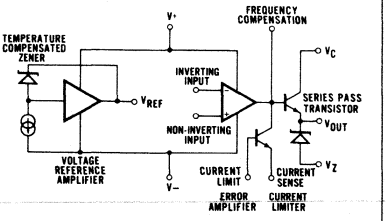
PHYSICAL DIMENSIONS



NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.32 grams

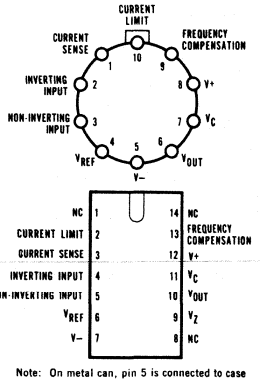
ORDER PART NO. U5R772312

EQUIVALENT CIRCUIT



CONNECTION DIAGRAMS

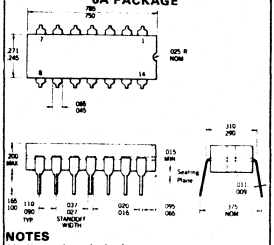
TOP VIEWS



Note: On metal can, pin 5 is connected to case

PHYSICAL DIMENSIONS

In accordance with JEDEC (TO-116) outline **CERAMIC DIP 6A PACKAGE**



NOTES

All dimensions in inches

Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion.

Board-drilling dimensions should equal your practice for .020 inch diameter lead.

Leads are tin-plated kovar

Package weight is 2.0 grams

ORDER PART NO. U6A7723312

FAIRCHILD SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Line Regulation	$V_{IN} = 12$ V to $V_{IN} = 15$ V		.01	0.1	% V_{OUT}
	$V_{IN} = 12$ V to $V_{IN} = 40$ V		.02	0.2	% V_{OUT}
	$-55°C \leq T_A \leq +125°C$, $V_{IN} = 12$ V to $V_{IN} = 15$ V			0.3	% V_{OUT}
Load Regulation	$I_L = 1$ mA to $I_L = 50$ mA		.03	0.15	% V_{OUT}
	$-55°C \leq T_A \leq +125°C$, $I_L = 1$ mA to $I_L = 50$ mA			0.6	% V_{OUT}
Ripple Rejection	f = 50 Hz to 10 kHz, $C_{REF} = 0$		74		dB
	f = 50 Hz to 10 kHz, $C_{REF} = 5$ μF		86		dB
Average Temperature Coefficient of Output Voltage	$-55°C \leq T_A \leq +125°C$		.002	.015	%/°C
Short Circuit Current Limit	$R_{SC} = 10\ \Omega$, $V_{OUT} = 0$		65		mA
Reference Voltage		6.95	7.15	7.35	V
Output Noise Voltage	BW = 100 Hz to 10 kHz, $C_{REF} = 0$		20		μV_{rms}
	BW = 100 Hz to 10 kHz, $C_{REF} = 5$ μF		2.5		μV_{rms}
Long Term Stability			0.1		%/1000 hrs
Standby Current Drain	$I_L = 0$, $V_{IN} = 30$ V		2.3	3.5	mA
Input Voltage Range		9.5		40	V
Output Voltage Range		2.0		37	V
Input-Output Voltage Differential		3.0		38	V

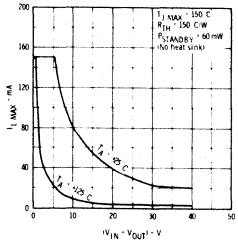
DEFINITION OF TERMS

LINE REGULATION — The percentage change in output voltage for a specified change in input voltage.
LOAD REGULATION — The percentage change in output voltage for a specified change in load current.
RIPPLE REJECTION — The ratio of the peak to peak input ripple voltage to the peak to peak output ripple voltage.
AVERAGE TEMPERATURE COEFFICIENT OF OUTPUT VOLTAGE — The percentage change in output voltage for a specified change in ambient temperature.
SHORT CIRCUIT CURRENT LIMIT — The output current of the regulator with the output shorted to the negative supply.
REFERENCE VOLTAGE — The output of the reference amplifier measured with respect to the negative supply.
OUTPUT NOISE VOLTAGE — The rms output noise voltage with constant load and no input ripple.
STANDBY CURRENT DRAIN — The supply current drawn by the regulator with no output load and no reference voltage load.
INPUT VOLTAGE RANGE — The range of supply voltage over which the regulator will operate.
OUTPUT VOLTAGE RANGE — The range of output voltage over which the regulator will operate.
INPUT-OUTPUT VOLTAGE DIFFERENTIAL — The range of voltage difference between the supply voltage and the regulated output voltage over which the regulator will operate.
SENSE VOLTAGE — The voltage between current sense and current limit terminals necessary to cause current limiting.
TRANSIENT RESPONSE — The closed-loop step function response of the regulator under small-signal conditions.

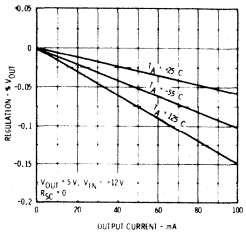
NOTES:
(1) Derate linearly at 6.8 mW/°C for operation at ambient temperatures above 25°C.
(2) Unless otherwise specified, $T_A = 25°C$, $V_{IN} = V^+ = V_C = 12$ V, $V^- = 0$, $V_{OUT} = 5$ V, $I_L = 1$ mA, $R_{SC} = 0$, $C_1 = 100$ pF, $C_{REF} = 0$ and divider impedance as seen by error amplifier ≤ 10 KΩ connected as shown in Fig. 1.
(3) L_1 is 40 turns of #20 enameled copper wire wound on Ferroxcube P36/22-3B7 pot core or equivalent with 0.009" air gap.
(4) Figures in parentheses may be used if R_1/R_2 divider is placed on opposite of error amp.
(5) Replace R_1/R_2 in figures with divider shown in figure 13.
(6) V^+ must be connected to a +3 V or greater supply.

TYPICAL PERFORMANCE CURVES

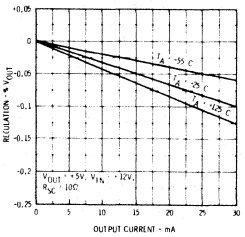
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



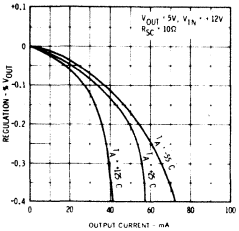
LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING



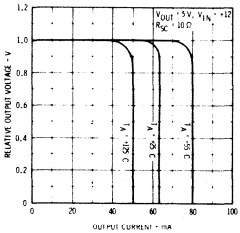
LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING



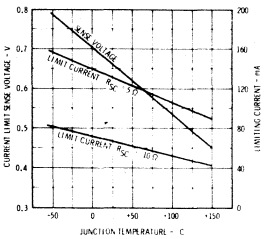
LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING



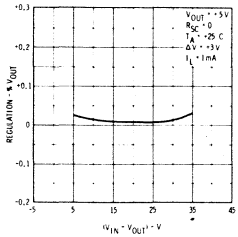
CURRENT LIMITING CHARACTERISTICS



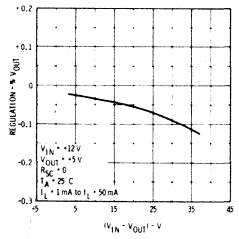
CURRENT LIMITING CHARACTERISTICS AS A FUNCTION OF JUNCTION TEMPERATURE



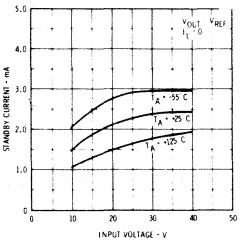
LINE REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



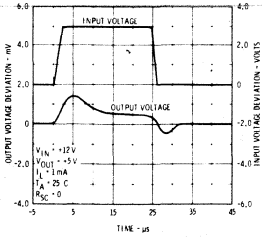
LOAD REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



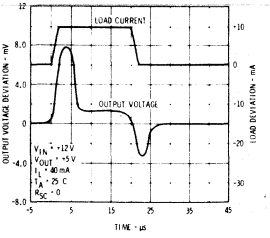
STANDBY CURRENT DRAIN AS A FUNCTION OF INPUT VOLTAGE



LINE TRANSIENT RESPONSE



LOAD TRANSIENT RESPONSE



OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY

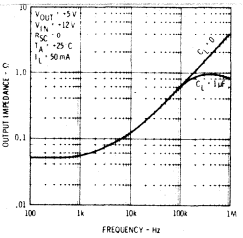


TABLE I
RESISTOR VALUES (kΩ) FOR STANDARD OUTPUT VOLTAGES

POSITIVE OUTPUT VOLTAGE	APPLICABLE FIGURES	FIXED OUTPUT ±5%		OUTPUT ADJUSTABLE ±10% (Note 5)			NEGATIVE OUTPUT VOLTAGE	APPLICABLE FIGURES	FIXED OUTPUT ±5%		5% OUTPUT ADJUSTABLE ±10%		
	(Note 4)	R_1	R_2	R_1	P_1	R_2			R_1	R_2	R_1	P_1	R_2
+3.0	1, 5, 6, 9, 12 (4)	4.12	3.01	1.8	0.5	1.2	+100	7	3.57	102	2.2	10	91
+3.6	1, 5, 6, 9, 12 (4)	3.57	3.65	1.5	0.5	1.5	+250	7	3.57	255	2.2	10	240
+5.0	1, 5, 6, 9, 12 (4)	2.15	4.99	.75	0.5	2.2	−6 (note 6)	3, (10)	3.57	2.43	1.2	0.5	.75
+6.0	1, 5, 6, 9, 12 (4)	1.15	6.04	0.5	0.5	2.7	−9	3, 10	3.48	5.36	1.2	0.5	2.0
+9.0	2, 4, (5, 6, 12, 9)	1.87	7.15	.75	1.0	2.7	−12	3, 10	3.57	8.45	1.2	0.5	3.3
+12	2, 4, (5, 6, 9, 12)	4.87	7.15	2.0	1.0	3.0	−15	3, 10	3.65	11.5	1.2	0.5	4.3
+15	2, 4, (5, 6, 9, 12)	7.87	7.15	3.3	1.0	3.0	−28	3, 10	3.57	24.3	1.2	0.5	10
+28	2, 4, (5, 6, 9, 12)	21.0	7.15	5.6	1.0	2.0	−45	8	3.57	41.2	2.2	10	33
+45	7	3.57	48.7	2.2	10	39	−100	8	3.57	97.6	2.2	10	91
+75	7	3.57	78.7	2.2	10	68	−250	8	3.57	249	2.2	10	240

TABLE II
FORMULAE FOR INTERMEDIATE OUTPUT VOLTAGES

Outputs from +2 to +7 volts
[Figures 1, 5, 6, 9, 12, (4)]

$$V_{OUT} = [V_{REF} \times \frac{R_2}{R_1 + R_2}]$$

Outputs from +4 to +250 volts
[Figure 7]

$$V_{OUT} = [\frac{V_{REF}}{2} \times \frac{R_2 - R_1}{R_1}]\ ;\ R_3 = R_4$$

Current Limiting

$$I_{LIMIT} = \frac{V_{SENSE}}{R_{sc}}$$

Outputs from +7 to +37 volts
[Figures 2, 4, (5, 6, 9, 12)]

$$V_{OUT} = [V_{REF} \times \frac{R_1 + R_2}{R_2}]$$

Outputs from −6 to −250 volts
[Figures 3, 8, 10]

$$V_{OUT} = [\frac{V_{REF}}{2} \times \frac{R_1 + R_2}{R_1}]\ ;\ R_3 = R_4$$

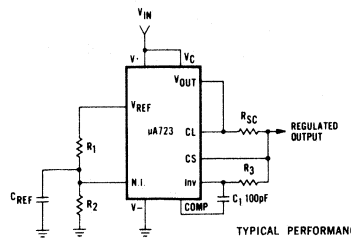
Foldback Current Limiting

$$I_{KNEE} = [\frac{V_{OUT} R_3}{R_{sc} R_4} + \frac{V_{SENSE}(R_3 + R_4)}{R_{sc} R_4}]$$

$$I_{SHORT\ CKT} = [\frac{V_{SENSE}}{R_{sc}} \times \frac{R_3 + R_4}{R_4}]$$

Figure 1

BASIC LOW VOLTAGE REGULATOR
(V_{out} = 2 to 7 Volts)



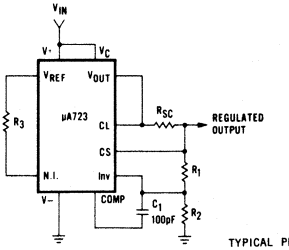
TYPICAL PERFORMANCE

Regulated Output Voltage	5 V
Line Regulation (ΔV_{IN} = 3 V)	0.5 mV
Load Regulation (ΔI_L=50 mA)	1.5 mV

Note: $R_3 = \frac{R_1 R_2}{R_1 + R_2}$ for minimum temperature drift.

Figure 2

BASIC HIGH VOLTAGE REGULATOR
(V_{out} = 7 to 37 Volts)

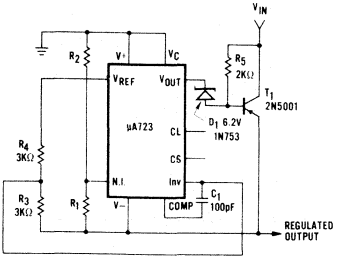


TYPICAL PERFORMANCE

Regulated Output Voltage	15 V
Line Regulation (ΔV_{IN} = 3 V)	1.5 mV
Load Regulation (ΔI_L=50 mA)	4.5 mV

Note: $R_3 = \frac{R_1 R_2}{R_1 + R_2}$ for minimum temperature drift.
R_3 may be eliminated for minimum component count.

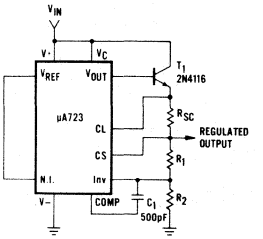
Figure 3
NEGATIVE VOLTAGE REGULATOR



TYPICAL PERFORMANCE

Regulated Output Voltage	−15 V
Line Regulation ($\Delta V_{IN} = 3$ V)	1 mV
Load Regulation ($\Delta I_L = 100$ mA)	2 mV

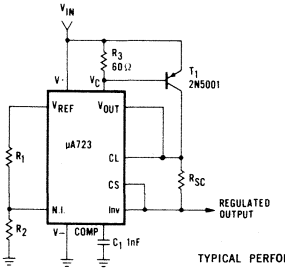
Figure 4
POSITIVE VOLTAGE REGULATOR
(External NPN Pass Transistor)



TYPICAL PERFORMANCE

Regulated Output Voltage	+15 V
Line Regulation ($\Delta V_{IN} = 3$ V)	1.5 mV
Load Regulation ($\Delta I_L = 1$ A)	15 mV

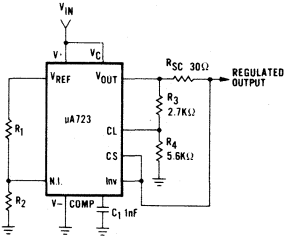
Figure 5
POSITIVE VOLTAGE REGULATOR
(External PNP Pass Transistor)



TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation ($\Delta V_{IN} = 3$ V)	0.5 mV
Load Regulation ($\Delta I_L = 1$ A)	5 mV

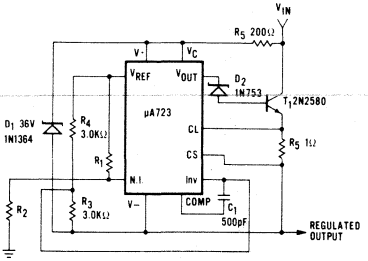
Figure 6
FOLDBACK CURRENT LIMITING



TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation ($\Delta V_{IN} = 3$ V)	0.5 mV
Load Regulation ($\Delta I_L = 10$ mA)	1 mV
Current Limit Knee	20 mA

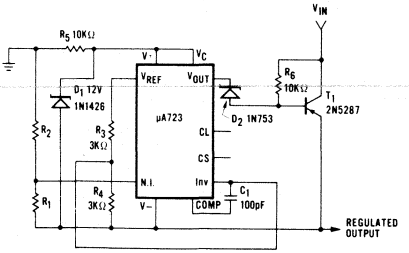
Figure 7
POSITIVE FLOATING REGULATOR



TYPICAL PERFORMANCE

Regulated Output Voltage	+50 V
Line Regulation ($\Delta V_{IN} = 20$ V)	15 mV
Load Regulation ($\Delta I_L = 50$ mA)	20 mV

Figure 8
NEGATIVE FLOATING REGULATOR

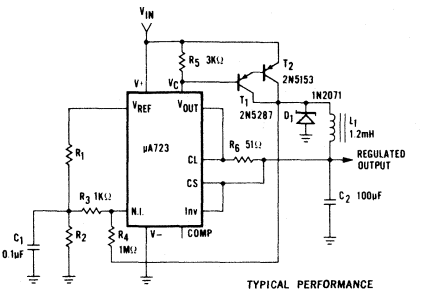


TYPICAL PERFORMANCE

Regulated Output Voltage	−100 V
Line Regulation ($\Delta V_{IN} = 20$ V)	30 mV
Load Regulation (ΔI_L=100 mA)	20 mV

Figure 9

POSITIVE SWITCHING REGULATOR



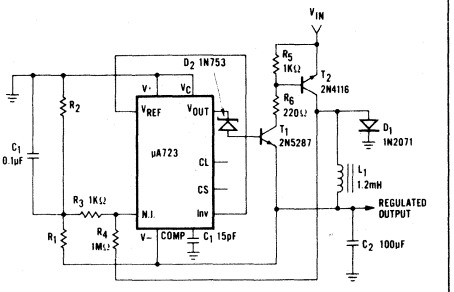
TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation (ΔV_{IN} = 30 V)	10 mV
Load Regulation (ΔI_L = 2 A)	80 mV

Note 3

Figure 10

NEGATIVE SWITCHING REGULATOR



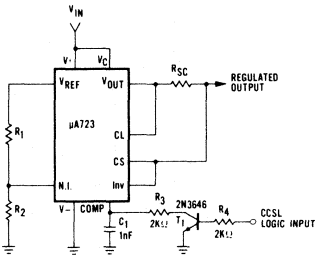
TYPICAL PERFORMANCE

Regulated Output Voltage	−15 V
Line Regulation (ΔV_{IN} = 20 V)	8 mV
Load Regulation (ΔI_L = 2 A)	6 mV

Note 3

Figure 11

REMOTE SHUTDOWN REGULATOR WITH CURRENT LIMITING



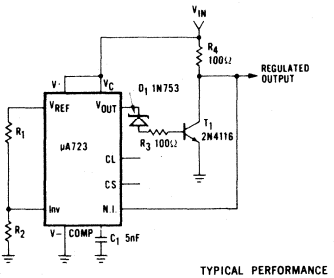
TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation (ΔV_{IN} = 3 V)	0.5 mV
Load Regulation (ΔI_L=50 mA)	1.5 mV

Note: Current limit transistor may be used for shutdown if current limiting is not required.

Figure 12

SHUNT REGULATOR

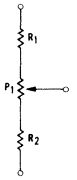


TYPICAL PERFORMANCE

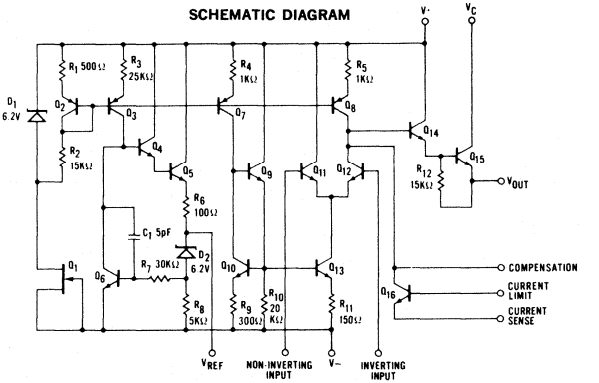
Regulated Output Voltage	+5 V
Line Regulation (ΔV_{IN} = 10 V)	0.5 mV
Load Regulation (ΔI_L = 100 mA)	1.5 mV

Figure 13

OUTPUT VOLTAGE ADJUST



SCHEMATIC DIAGRAM



μA723C
PRECISION VOLTAGE REGULATOR
FAIRCHILD LINEAR INTEGRATED CIRCUITS

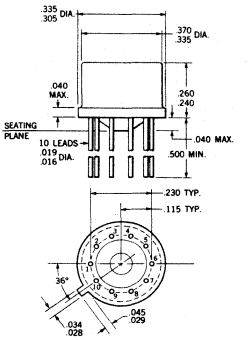
- **POSITIVE OR NEGATIVE SUPPLY OPERATION**
- **SERIES, SHUNT, SWITCHING OR FLOATING OPERATION**
- **.01% LINE AND LOAD REGULATION**
- **OUTPUT VOLTAGE ADJUSTABLE FROM 2 TO 37 VOLTS**
- **OUTPUT CURRENT TO 150 mA WITHOUT EXTERNAL PASS TRANSISTOR**

GENERAL DESCRIPTION — The μA723C is a monolithic voltage regulator constructed on a single silicon chip using the Fairchild Planar* epitaxial process. The device consists of a temperature compensated reference amplifier, error amplifier, power series pass transistor and current limit circuitry. Additional NPN or PNP pass elements may be used when output currents exceeding 150 mA are required. Provisions are made for adjustable current limiting and remote shutdown. In addition to the above, the device features low standby current drain, low temperature drift and high ripple rejection. The μA723C is intended for use with positive or negative supplies as a series, shunt, switching or floating regulator. Applications include laboratory power supplies, isolation regulators for low level data amplifiers, logic card regulators, small instrument power supplies, airborne systems and other power supplies for digital and linear circuits. For full temperature range operation (−55°C to +125°C), see μA723 data sheet.

ABSOLUTE MAXIMUM RATINGS

Voltage from V^+ to V^-	40 V
Input-Output Voltage Differential	40 V
Maximum Output Current	150 mA
Current from V_Z	25 mA
Current from V_{REF}	15 mA
Internal Power Dissipation—Metal Can (Note 1)	800 mW
Internal Power Dissipation—DIP (Note 1)	900 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 second time limit)	300°C

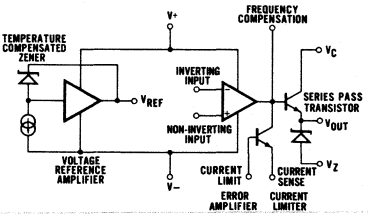
PHYSICAL DIMENSIONS



NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.32 grams

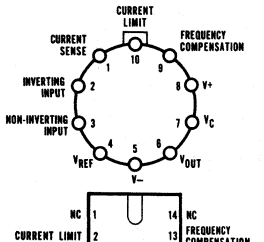
ORDER PART NO. U6A7723393

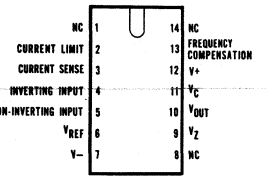
EQUIVALENT CIRCUIT



CONNECTION DIAGRAMS

TOP VIEWS

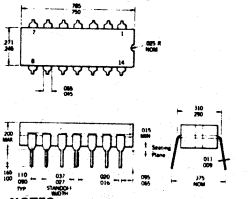




Note: On metal can, pin 5 is connected to case

PHYSICAL DIMENSIONS

In accordance with JEDEC (TO-116) outline **CERAMIC DIP 6A PACKAGE**



NOTES

All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers.
They are purposely shipped with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for .020 inch diameter lead.
Leads are tin-plated kovar
Package weight is 2.0 grams.

ORDER PART NO. U6A77233[Z

Notes on Page 2.

*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Line Regulation	$V_{IN} = 12$ V to $V_{IN} = 15$ V		01	0.1	% V_{OUT}
	$V_{IN} = 12$ V to $V_{IN} = 40$ V		0.1	0.5	% V_{OUT}
	$0°C \leq T_A \leq 70°C$, $V_{IN} = 12$ V to $V_{IN} = 15$ V			0.3	% V_{OUT}
Load Regulation	$I_L = 1$ mA to $I_L = 50$ mA		.03	0.2	% V_{OUT}
	$0°C \leq T_A \leq 70°C$, $I_L = 1$ mA to $I_L = 50$ mA			0.6	% V_{OUT}
Ripple Rejection	f = 50 Hz to 10 kHz, $C_{REF} = 0$		74		dB
	f = 50 Hz to 10 kHz, $C_{REF} = 5$ μF		86		dB
Average Temperature Coefficient of Output Voltage	$0°C \leq T_A \leq 70°C$		.003	.015	%/°C
Short Circuit Current Limit	$R_{SC} = 10\ \Omega$, $V_{OUT} = 0$		65		mA
Reference Voltage		6.80	7.15	7.50	V
Output Noise Voltage	BW = 100 Hz to 10 kHz, $C_{REF} = 0$		20		μV_{rms}
	BW = 100 Hz to 10 kHz, $C_{REF} = 5$ μF		2.5		μV_{rms}
Long Term Stability			0.1		%/1000 hrs
Standby Current Drain	$I_L = 0$, $V_{IN} = 30$ V		2.3	4.0	mA
Input Voltage Range		9.5		40	V
Output Voltage Range		2.0		37	V
Input-Output Voltage Differential		3.0		38	V

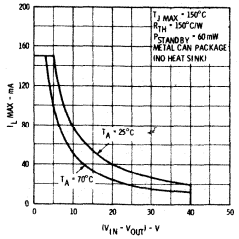
DEFINITION OF TERMS

LINE REGULATION — The percentage change in output voltage for a specified change in input voltage.
LOAD REGULATION — The percentage change in output voltage for a specified change in load current.
RIPPLE REJECTION — The ratio of the peak to peak input ripple voltage to the peak to peak output ripple voltage.
AVERAGE TEMPERATURE COEFFICIENT OF OUTPUT VOLTAGE — The percentage change in output voltage for a specified change in ambient temperature.
SHORT CIRCUIT CURRENT LIMIT — The output current of the regulator with the output shorted to the negative supply.
REFERENCE VOLTAGE — The output of the reference amplifier measured with respect to the negative supply.
OUTPUT NOISE VOLTAGE — The rms output noise voltage with constant load and no input ripple.
STANDBY CURRENT DRAIN — The supply current drawn by the regulator with no output load and no reference voltage load.
INPUT VOLTAGE RANGE — The range of supply voltage over which the regulator will operate.
OUTPUT VOLTAGE RANGE — The range of output voltage over which the regulator will operate.
INPUT-OUTPUT VOLTAGE DIFFERENTIAL — The range of voltage difference between the supply voltage and the regulated output voltage over which the regulator will operate.
SENSE VOLTAGE — The voltage between current sense and current limit terminals necessary to cause current limiting.
TRANSIENT RESPONSE — The closed-loop step function response of the regulator under small-signal conditions.

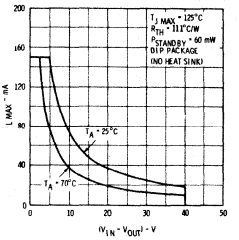
NOTES:
(1) Derate metal can package at 6.8 mW/°C and dual in-line package at 9 mW/°C for operation at ambient temperatures above 25°C.
(2) Unless otherwise specified, $T_A = 25°C$, $V_{IN} = V^+ = V_C = 12$ V, $V^- = 0$, $V_{out} = 5$ V, $I_L = 1$ mA, $R_{SC} = 0$, $C_1 = 100$ pF, $C_{REF} = 0$, divider impedance as seen by error amplifier ≤ 10 kΩ, and connected as shown in Figure 1.
(3) For metal can applications where V_Z is required, an external 6.2 zener should be connected in series with V_{out}.
(4) Figures in parentheses may be used if R_1/R_2 divider is placed on opposite side of error amp.
(5) Replace R_1/R_2 in figures with divider shown in figure 13.
(6) V^+ must be connected to a +3 V or greater supply.
(7) L_1 is 40 turns of #20 enameled copper wire wound on Ferroxcube P36/22-3B7 pot core or equivalent with 0.009" air gap.

TYPICAL PERFORMANCE CURVES

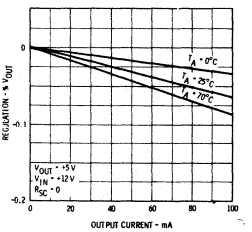
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



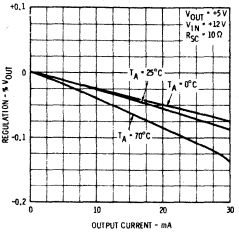
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



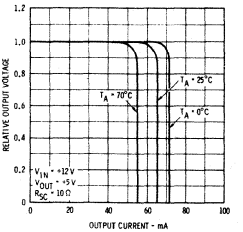
LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING



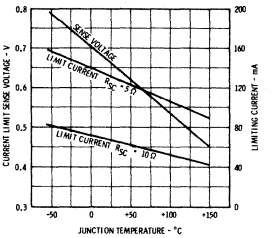
LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING



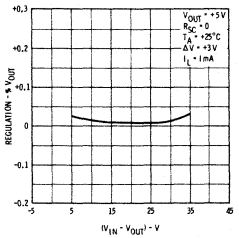
CURRENT LIMITING CHARACTERISTICS



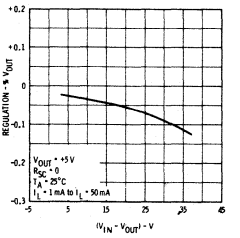
CURRENT LIMITING CHARACTERISTICS AS A FUNCTION OF JUNCTION TEMPERATURE



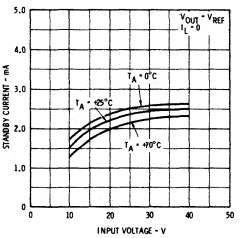
LINE REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



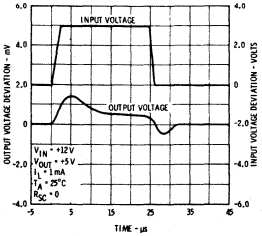
LOAD REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



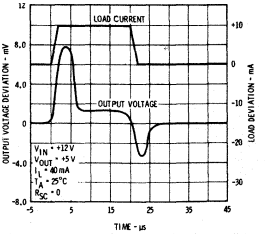
STANDBY CURRENT DRAIN AS A FUNCTION OF INPUT VOLTAGE



LINE TRANSIENT RESPONSE



LOAD TRANSIENT RESPONSE



OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY

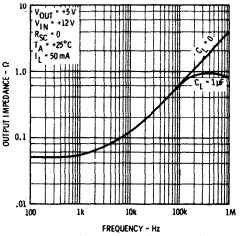


TABLE I
RESISTOR VALUES (kΩ) FOR STANDARD OUTPUT VOLTAGES

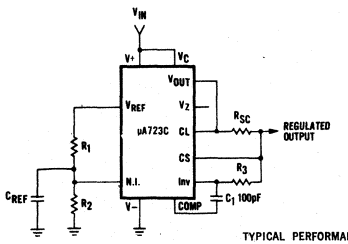
POSITIVE OUTPUT VOLTAGE	APPLICABLE FIGURES	FIXED OUTPUT ±5%		OUTPUT ADJUSTABLE ±10% (Note 5)			NEGATIVE OUTPUT VOLTAGE	APPLICABLE FIGURES	FIXED OUTPUT ±5%		5% OUTPUT ADJUSTABLE ±10%		
	(Note 4)	R_1	R_2	R_1	P_1	R_2			R_1	R_2	R_1	P_1	R_2
+3.0	1, 5, 6, 9, 12 (4)	4.12	3.01	1.8	0.5	1.2	+100	7	3.57	102	2.2	10	91
+3.6	1, 5, 6, 9, 12 (4)	3.57	3.65	1.5	0.5	1.5	+250	7	3.57	255	2.2	10	240
+5.0	1, 5, 6, 9, 12 (4)	2.15	4.99	.75	0.5	2.2	−6 (note 6)	3, (10)	3.57	2.43	1.2	0.5	.75
+6.0	1, 5, 6, 9, 12 (4)	1.15	6.04	0.5	0.5	2.7	−9	3, 10	3.48	5.36	1.2	0.5	2.0
+9.0	2, 4, (5, 6, 12, 9)	1.87	7.15	.75	1.0	2.7	−12	3, 10	3.57	8.45	1.2	0.5	3.3
+12	2, 4, (5, 6, 9, 12)	4.87	7.15	2.0	1.0	3.0	−15	3, 10	3.65	11.5	1.2	0.5	4.3
+15	2, 4, (5, 6, 9, 12)	7.87	7.15	3.3	1.0	3.0	−28	3, 10	3.57	24.3	1.2	0.5	10
+28	2, 4, (5, 6, 9, 12)	21.0	7.15	5.6	1.0	2.0	−45	8	3.57	41.2	2.2	10	33
+45	7	3.57	48.7	2.2	10	39	−100	8	3.57	97.6	2.2	10	91
+75	7	3.57	78.7	2.2	10	68	−250	8	3.57	249	2.2	10	240

TABLE II
FORMULAE FOR INTERMEDIATE OUTPUT VOLTAGES

Outputs from +2 to +7 volts [Figures 1, 5, 6, 9, 12, (4)] $V_{OUT} = [V_{REF} \times \frac{R_2}{R_1 + R_2}]$	Outputs from +4 to +250 volts [Figure 7] $V_{OUT} = [\frac{V_{REF}}{2} \times \frac{R_2 - R_1}{R_1}]$; $R_3 = R_4$	Current Limiting $I_{LIMIT} = \frac{V_{SENSE}}{R_{SC}}$
Outputs from +7 to +37 volts [Figures 2, 4, (5, 6, 9, 12)] $V_{OUT} = [V_{REF} \times \frac{R_1 + R_2}{R_2}]$	Outputs from −6 to −250 volts [Figures 3, 8, 10] $V_{OUT} = [\frac{V_{REF}}{2} \times \frac{R_1 + R_2}{R_1}]$; $R_3 = R_4$	Foldback Current Limiting $I_{KNEE} = [\frac{V_{OUT} R_3}{R_{SC} R_4} + \frac{V_{SENSE}(R_3 + R_4)}{R_{SC} R_4}]$ $I_{SHORT\ CKT} = [\frac{V_{SENSE}}{R_{SC}} \times \frac{R_3 + R_4}{R_4}]$

Figure 1

BASIC LOW VOLTAGE REGULATOR
(V_{out} = 2 to 7 Volts)



TYPICAL PERFORMANCE

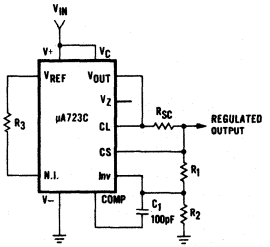
Regulated Output Voltage	5 V
Line Regulation (ΔV_{IN} = 3 V)	0.5 mV
Load Regulation (ΔI_L=50 mA)	1.5 mV

Note: $R_3 = \frac{R_1 R_2}{R_1 + R_2}$ *for minimum temperature drift.*

R_3 may be eliminated for minimum component count.

Figure 2

BASIC HIGH VOLTAGE REGULATOR
(V_{out} = 7 to 37 Volts)



TYPICAL PERFORMANCE

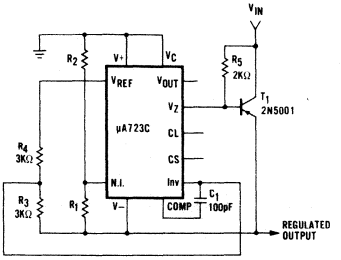
Regulated Output Voltage	15 V
Line Regulation (ΔV_{IN} = 3 V)	1.5 mV
Load Regulation (ΔI_L=50 mA)	4.5 mV

Note: $R_3 = \frac{R_1 R_2}{R_1 + R_2}$ *for minimum temperature drift.*

R_3 may be eliminated for minimum component count.

Figure 3

NEGATIVE VOLTAGE REGULATOR



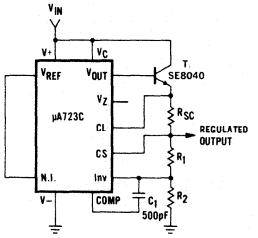
TYPICAL PERFORMANCE

Regulated Output Voltage	−15 V
Line Regulation ($\Delta V_{IN} = 3$ V)	1 mV
Load Regulation ($\Delta I_L = 100$ mA)	2 mV

Note 3

Figure 4

POSITIVE VOLTAGE REGULATOR
(External NPN Pass Transistor)

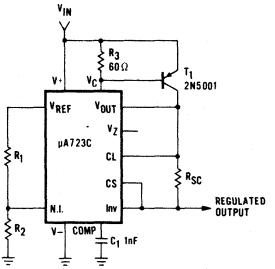


TYPICAL PERFORMANCE

Regulated Output Voltage	+15 V
Line Regulation ($\Delta V_{IN} = 3$ V)	1.5 mV
Load Regulation ($\Delta I_L = 1$ A)	15 mV

Figure 5

POSITIVE VOLTAGE REGULATOR
(External PNP Pass Transistor)

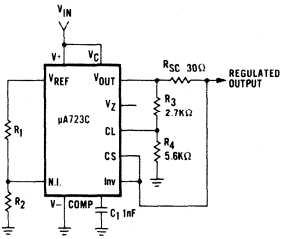


TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation ($\Delta V_{IN} = 3$ V)	0.5 mV
Load Regulation ($\Delta I_L = 1$ A)	5 mV

Figure 6

FOLDBACK CURRENT LIMITING

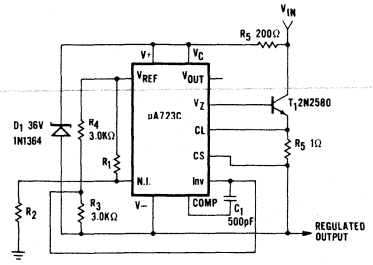


TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation ($\Delta V_{IN} = 3$ V)	0.5 mV
Load Regulation ($\Delta I_L = 10$ mA)	1 mV
Current Limit Knee	20 mA

Figure 7

POSITIVE FLOATING REGULATOR



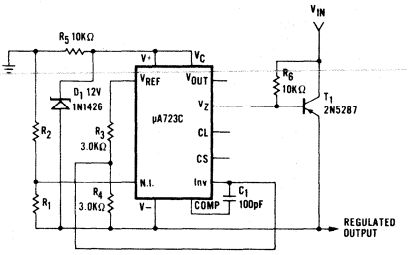
TYPICAL PERFORMANCE

Regulated Output Voltage	+50 V
Line Regulation ($\Delta V_{IN} = 20$ V)	15 mV
Load Regulation ($\Delta I_L = 50$ mA)	20 mV

Note 3

Figure 8

NEGATIVE FLOATING REGULATOR

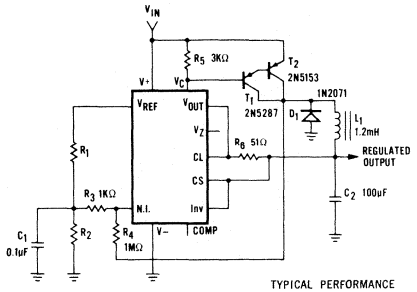


TYPICAL PERFORMANCE

Regulated Output Voltage	−100 V
Line Regulation ($\Delta V_{IN} = 20$ V)	30 mV
Load Regulation (ΔI_L=100 mA)	20 mV

Note 3

Figure 9
POSITIVE SWITCHING REGULATOR

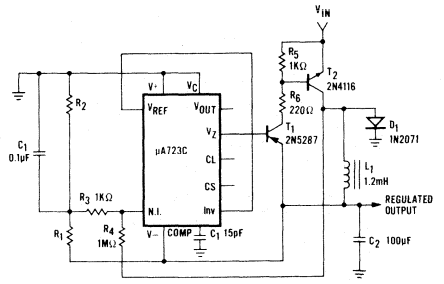


TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation ($\Delta V_{IN} = 30$ V)	10 mV
Load Regulation ($\Delta I_L = 2$ A)	80 mV

Note 7

Figure 10
NEGATIVE SWITCHING REGULATOR

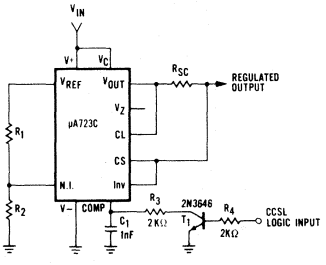


TYPICAL PERFORMANCE

Regulated Output Voltage	−15 V
Line Regulation ($\Delta V_{IN} = 20$ V)	8 mV
Load Regulation ($\Delta I_L = 2$ A)	6 mV

Note 3
Note 7

Figure 11
REMOTE SHUTDOWN REGULATOR WITH CURRENT LIMITING

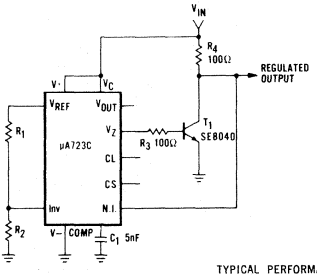


TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation ($\Delta V_{IN} = 3$ V)	0.5 mV
Load Regulation (ΔI_L=50 mA)	1.5 mV

Note: Current limit transistor may be used for shutdown if current limiting is not required.

Figure 12
SHUNT REGULATOR

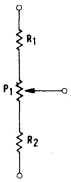


TYPICAL PERFORMANCE

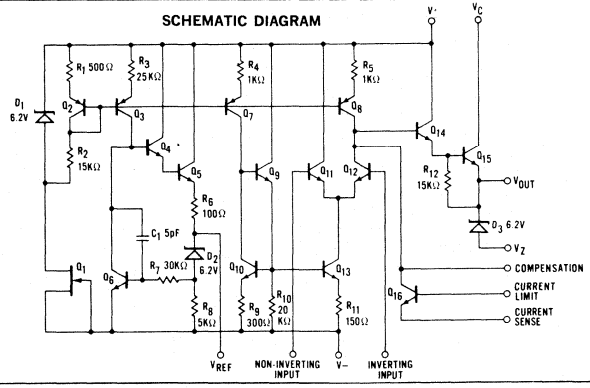
Regulated Output Voltage	+5 V
Line Regulation ($\Delta V_{IN} = 10$ V)	0.5 mV
Load Regulation ($\Delta I_L = 100$ mA)	1.5 mV

Note 3

Figure 13
OUTPUT VOLTAGE ADJUST



SCHEMATIC DIAGRAM



μA725

INSTRUMENTATION OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

FEATURES

- **LOW INPUT NOISE CURRENT . . . . . 0.15 pA/$\sqrt{Hz}$**
- **HIGH OPEN LOOP GAIN 3,000,000**
- **LOW INPUT OFFSET CURRENT . . . . . 2 nA**
- **LOW INPUT VOLTAGE DRIFT . . . . . 0.6 μV/°C**
- **HIGH COMMON MODE REJECTION . . . 120 dB**
- **HIGH INPUT VOLTAGE RANGE . . . . . ±14 V**
- **WIDE POWER SUPPLY RANGE . . . . . ±3 V TO ±22 V**
- **OFFSET NULL CAPABILITY**

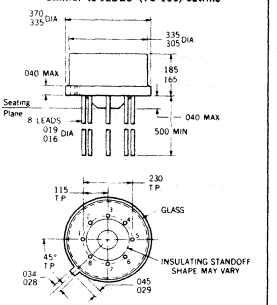
GENERAL DESCRIPTION — The μA725 is an instrumentation operational amplifier constructed on a single silicon chip using the Fairchild Planar* epitaxial process. It is intended for precise, low level signal amplification applications where low noise, low drift, and accurate closed loop gain are required. The offset null capability, low power consumption, very high voltage gain as well as wide power supply voltage range provide superior performance for a wide range of instrumentation applications. The μA725 is pin compatible with the popular μA741 operational amplifier. (For other Fairchild Operational Amplifiers, see listing on page 5.)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22 V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage (Note 2)	±22 V
Input Voltage (Note 3)	±22 V
Voltage between Offset Null and V^+	±0.5 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 60 seconds)	300°C

PHYSICAL DIMENSIONS

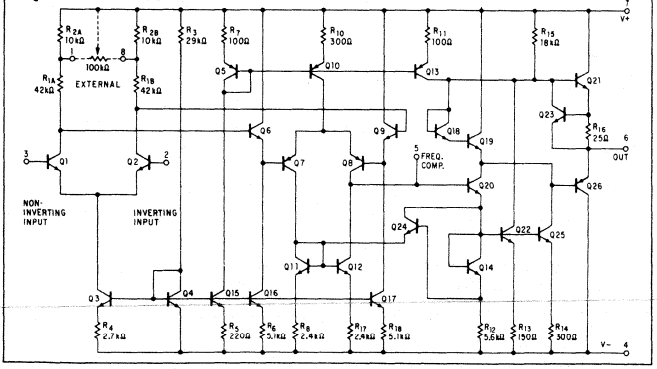
Similar to JEDEC (TO-100) outline



NOTES:
All dimensions in inches
Leads are gold-plated kovar
No leads connected to case
Package weight is 1.22 grams

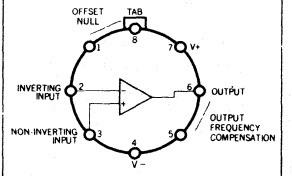
ORDER PART NO. U5T7725312

EQUIVALENT CIRCUIT



CONNECTION DIAGRAM

(Top View)



NOTE: Pin 4 connected to case

NOTES:
(1) Rating applies for case temperatures to +125°C; derate linearly at 6.5 mW/°C for ambient temperatures above 75°C.
(2) Rating applies for 5 ms pulses with 10% duty cycle, derate to ±5 V for continuous operation.
(3) For supply voltages less than ±22 V, the absolute maximum input voltage is equal to the supply voltage.

*Planar is a patented Fairchild process.

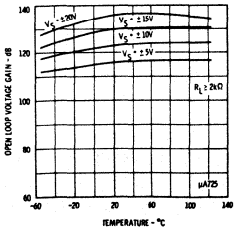
FAIRCHILD SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified)

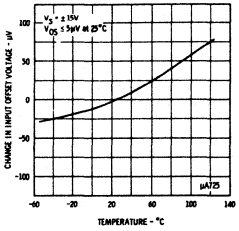
PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage (Without external trim)	$R_S \leq 10$ kΩ		0.5	1.0	mV
Input Offset Current			2.0	20	nA
Input Bias Current			42	100	nA
Input Noise Voltage	$f_o = 10$ Hz		15		nV/$\sqrt{\text{Hz}}$
	$f_o = 100$ Hz		9.0		nV/$\sqrt{\text{Hz}}$
	$f_o = 1$ kHz		8.0		nV/$\sqrt{\text{Hz}}$
Input Noise Current	$f_o = 10$ Hz		1.0		pA/$\sqrt{\text{Hz}}$
	$f_o = 100$ Hz		0.3		pA/$\sqrt{\text{Hz}}$
	$f_o = 1$ kHz		0.15		pA/$\sqrt{\text{Hz}}$
Input Resistance			1.5		MΩ
Input Voltage Range		±13.5	±14		V
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	1,000,000	3,000,000		
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	110	120		dB
Power Supply Rejection Ratio	$R_S \leq 10$ kΩ		2.0	10	μV/V
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±13.5		V
	$R_L \geq 2$ kΩ	±10	±13.5		V
Output Resistance			150		Ω
Power Consumption			80	105	mW
The following specifications apply for $-55°C \leq T_A \leq +125°C$ unless otherwise specified:					
Input Offset Voltage (Without external trim)	$R_S \leq 10$ kΩ			1.5	mV
Average Input Offset Voltage Drift (Without external trim)	$R_S = 50$ Ω		2.0	5.0	μV/°C
Average Input Offset Voltage Drift (With external trim)	$R_S = 50$ Ω		0.6		μV/°C
Input Offset Current	$T_A = +125°C$		1.2	20	nA
	$T_A = -55°C$		7.5	40	nA
Average Input Offset Current Drift			35	150	pA/°C
Input Bias Current	$T_A = +125°C$		20	100	nA
	$T_A = -55°C$		80	200	nA
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, $T_A = +125°C$	1,000,000			
	$R_L \geq 2$ kΩ, $T_A = -55°C$	250,000			
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	100			dB
Power Supply Rejection Ratio	$R_S \leq 10$ kΩ			20	μV/V
Output Voltage Swing	$R_L \geq 2$ kΩ	±10			V

TYPICAL PERFORMANCE CURVES

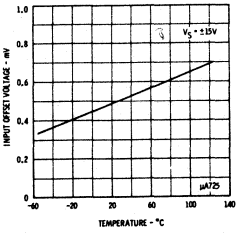
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE FOR VARIOUS SUPPLY VOLTAGES



NULLED INPUT OFFSET VOLTAGE AS A FUNCTION OF TEMPERATURE

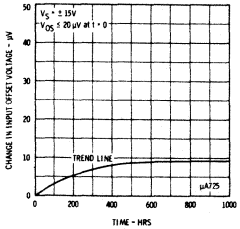


UNNULLED INPUT OFFSET VOLTAGE AS A FUNCTION OF TEMPERATURE

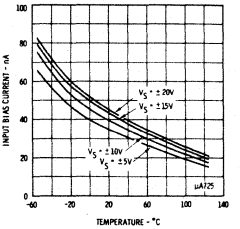


TYPICAL PERFORMANCE CURVES

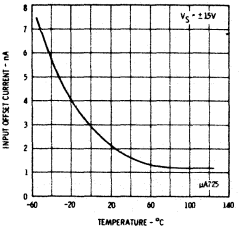
INPUT OFFSET VOLTAGE DRIFT AS A FUNCTION OF TIME



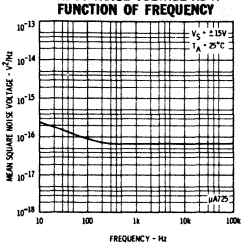
INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE



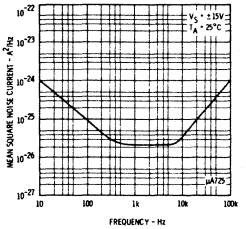
INPUT OFFSET CURRENT AS A FUNCTION OF TEMPERATURE



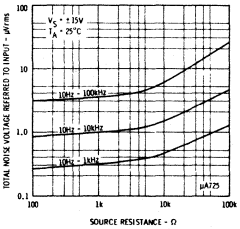
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



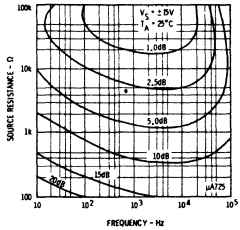
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



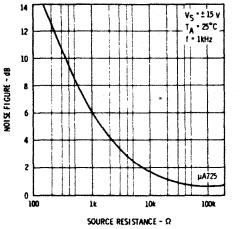
BROADBAND NOISE FOR VARIOUS BANDWIDTHS



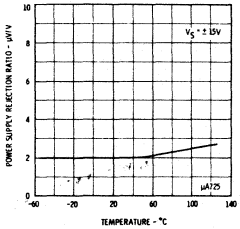
NARROW BAND SPOT NOISE FIGURE CONTOURS



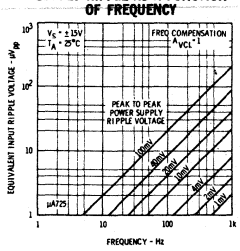
NOISE FIGURE AS A FUNCTION OF SOURCE RESISTANCE



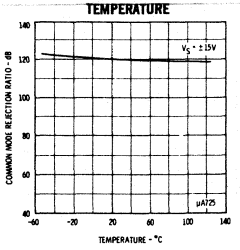
SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF TEMPERATURE



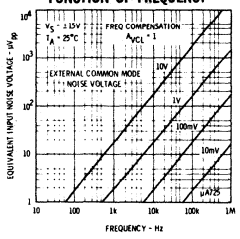
EQUIVALENT INPUT RIPPLE VOLTAGE DUE TO POWER SUPPLY RIPPLE AS A FUNCTION OF FREQUENCY



COMMON MODE REJECTION RATIO AS A FUNCTION OF TEMPERATURE

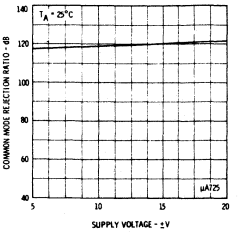


EQUIVALENT INPUT NOISE VOLTAGE DUE TO EXTERNAL COMMON MODE NOISE AS A FUNCTION OF FREQUENCY

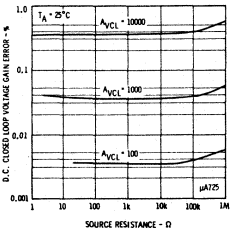


TYPICAL PERFORMANCE CURVES

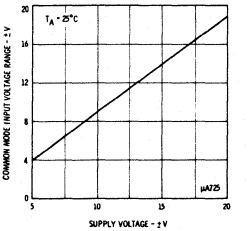
COMMON MODE REJECTION RATIO AS A FUNCTION OF SUPPLY VOLTAGE



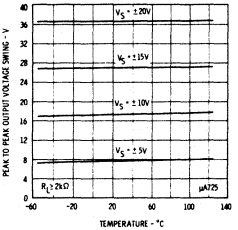
D.C. CLOSED LOOP VOLTAGE GAIN ERROR AS A FUNCTION OF SOURCE RESISTANCE



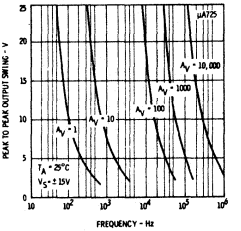
COMMON MODE INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



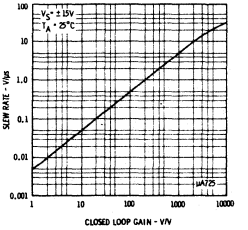
OUTPUT VOLTAGE SWING AS A FUNCTION OF TEMPERATURE



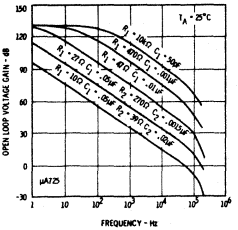
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR RECOMMENDED COMPENSATION NETWORKS



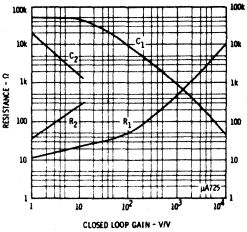
SLEW RATE AS A FUNCTION OF CLOSED-LOOP GAIN USING RECOMMENDED COMPENSATION NETWORKS



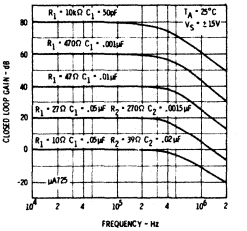
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY USING RECOMMENDED COMPENSATION NETWORKS



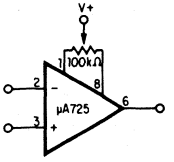
VALUES FOR SUGGESTED COMPENSATION NETWORKS FOR VARIOUS CLOSED LOOP VOLTAGE GAINS



FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS USING RECOMMENDED COMPENSATION NETWORKS



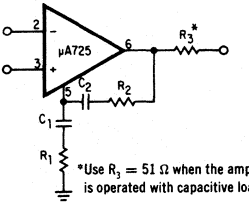
VOLTAGE OFFSET NULL CIRCUIT



COMPENSATION COMPONENT VALUES

A_{VCL}	R_1 (Ω)	C_1 (μF)	R_2 (Ω)	C_2 (μF)
10,000	10 k	50 pF	—	—
1,000	470	.001	—	—
100	47	.01	—	—
10	27	.05	270	.0015
1	10	.05	39	.02

FREQUENCY COMPENSATION CIRCUIT



*Use R_3 = 51 Ω when the amplifier is operated with capacitive load.

DEFINITION OF TERMS

INPUT OFFSET VOLTAGE — That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the output at zero volts.

INPUT BIAS CURRENT — The average of the two input currents.

INPUT NOISE VOLTAGE — The square root of the mean square narrow-band noise voltage at the output divided by the measurement system gain with low source resistance.

INPUT NOISE CURRENT — $\sqrt{\overline{i_n^2}} = \sqrt{\dfrac{\overline{e_{meas}}^2 - 4kTR_S - \overline{e_n}^2}{R_S^2}}$ for $\Delta f = 1$ Hz

INPUT RESISTANCE — The resistance looking into either input terminal with the other grounded.

INPUT VOLTAGE RANGE — The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

LARGE-SIGNAL VOLTAGE GAIN — The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.

SUPPLY VOLTAGE REJECTION RATIO — The ratio of the change in input offset voltage to the change in supply voltage producing it.

OUTPUT VOLTAGE SWING — The peak output swing, referred to zero, that can be obtained without clipping.

OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

POWER CONSUMPTION — The DC power required to operate the amplifier with the output at zero and with no load current.

AVERAGE INPUT OFFSET VOLTAGE DRIFT — The change in input offset voltage divided by the change in ambient temperature producing it.

AVERAGE INPUT OFFSET CURRENT DRIFT — The change in input offset current divided by the change in ambient temperature producing it.

EQUIVALENT INPUT RIPPLE VOLTAGE — The change in input offset voltage due to ripple on the applied supply voltage.

EQUIVALENT INPUT COMMON MODE NOISE VOLTAGE — The change in input offset voltage due to common mode input noise.

SLEW RATE — The maximum rate of change of output voltage for a large signal input.

CLOSED LOOP VOLTAGE GAIN ERROR — Deviation from the theoretical closed loop voltage gain due to finite open loop voltage gain and input resistance, and non-zero output resistance.

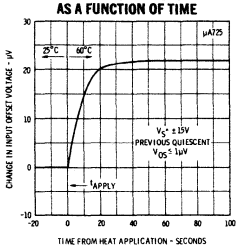
NOTE

FOR OTHER FAIRCHILD OPERATIONAL AMPLIFIERS, SEE THE FOLLOWING DATA SHEETS:

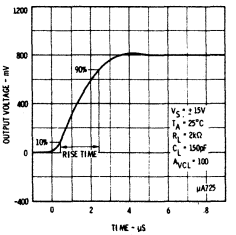
HIGH SPEED — μA715, μA715C
INSTRUMENTATION OPERATIONAL AMPLIFIER — μA725B, μA725C
TEMPERATURE STABLE PREAMPS — μA727, μA727B
MICROPOWER — μA735, μA735B, μA735C
FET INPUT — μA7400C
FREQUENCY COMPENSATED — μA741, μA741C
DUALS — μA739C, μA749, μA749C, μA747, μA747C
HIGH PERFORMANCE — μA748, μA748C
PRECISION — μA777, μA777B, μA777C

TYPICAL PERFORMANCE CURVES

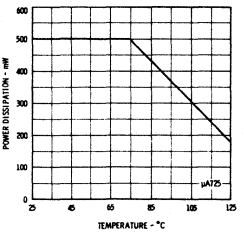
CHANGE IN INPUT OFFSET VOLTAGE DUE TO THERMAL SHOCK AS A FUNCTION OF TIME



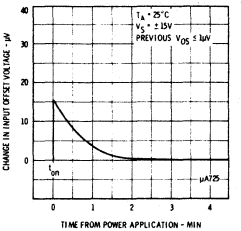
TRANSIENT RESPONSE



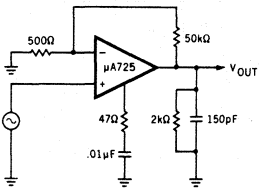
ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



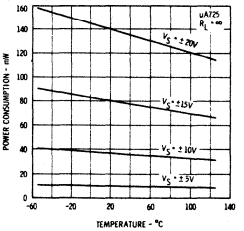
STABILIZATION TIME OF INPUT OFFSET VOLTAGE FROM POWER TURN-ON



TRANSIENT RESPONSE TEST CIRCUIT

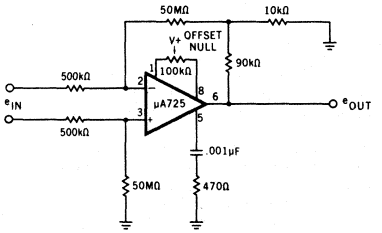


POWER CONSUMPTION AS A FUNCTION OF TEMPERATURE



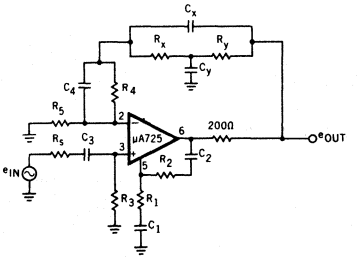
TYPICAL APPLICATIONS

PRECISION AMPLIFIER — $A_{VCL} = 1000$

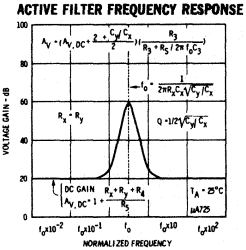


CHARACTERISTICS:
A_{VCL} = 1000 = 60 dB
DC Gain Error = 0.05%
Bandwidth = 1 kHz for −0.05% error
Diff. Input Res. = 1 MΩ
Typical amplifying capability
e_{IN} = 10 μV on V_{CMI} = 1.0 V
Caution: Minimize Stray Capacitance

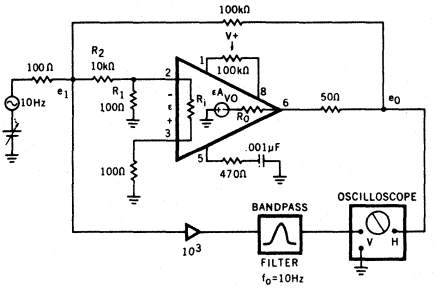
ACTIVE FILTER — BANDPASS WITH 60 dB GAIN



ACTIVE FILTER FREQUENCY RESPONSE



OPEN LOOP VOLTAGE GAIN TEST CIRCUIT



$$A_{VO} \simeq \frac{e_0}{e_1}\left(\frac{R_2 R_i + R_1 R_i + R_1 R_2}{R_1 R_i}\right) = \frac{e_0}{e_1}\,101$$

μA725B

INSTRUMENTATION OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

- **LOW INPUT NOISE CURRENT . . . . . 0.15 pA/$\sqrt{\text{Hz}}$**
- **HIGH OPEN LOOP GAIN 3,000,000**
- **LOW INPUT OFFSET CURRENT . . . . . 2 nA**
- **LOW INPUT VOLTAGE DRIFT . . . . . 0.6 μV/°C**
- **HIGH COMMON MODE REJECTION . . . 120 dB**
- **HIGH INPUT VOLTAGE RANGE . . . . . ±14 V**
- **WIDE POWER SUPPLY RANGE . . . . . ±3 V TO ±22 V**
- **OFFSET NULL CAPABILITY**

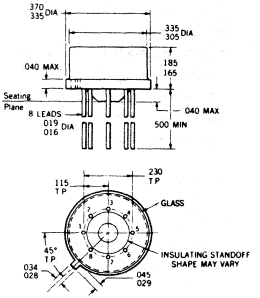
GENERAL DESCRIPTION — The μA725B is an instrumentation operational amplifier constructed on a single silicon chip using the Fairchild Planar* epitaxial process. It is intended for precise, low level signal amplification applications where low noise, low drift, and accurate closed loop gain are required. The offset null capability, low power consumption, very high voltage gain as well as wide power supply voltage range provide superior performance for a wide range of instrumentation applications. The μA725B is pin compatible with the popular μA741 operational amplifier. For full temperature operation (−55°C to +125°C), see μA725 data sheet. (For other Fairchild Operational Amplifiers, see Page 5.)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22 V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage (Note 2)	±22 V
Input Voltage (Note 3)	±22 V
Voltage between Offset Null and V⁺	±0.5 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−20°C to +85°C
Lead Temperature (Soldering, 60 seconds)	300°C

PHYSICAL DIMENSIONS

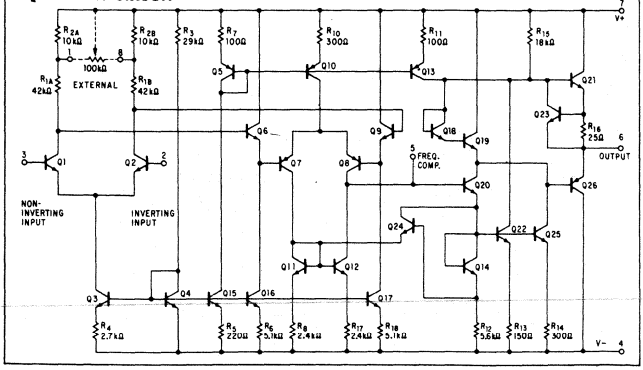
Similar to JEDEC (TO-100) outline



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.22 grams

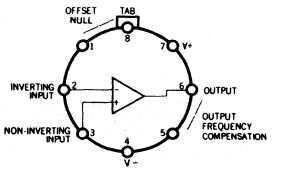
ORDER PART NO. U5T7725333

EQUIVALENT CIRCUIT



CONNECTION DIAGRAM

(TOP VIEW)



NOTE: Pin 4 connected to case

NOTES:

(1) Rating applies for case temperatures to +85°C; derate linearly at 6.5 mW/°C for ambient temperatures above 75°C.
(2) Rating applies for 5 ms pulses with 10% duty cycle, derate to ±5 V for continuous operation.
(3) For supply voltages less than ±22 V, the absolute maximum input voltage is equal to the supply voltage.

*Planar is a patented Fairchild process.

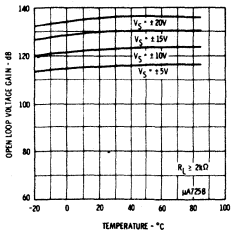
FAIRCHILD SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified)

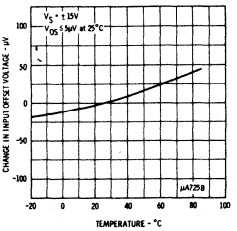
PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage (Without external trim)	$R_S \leq 10$ kΩ		0.5	1.5	mV
Input Offset Current			2.0	20	nA
Input Bias Current			42	100	nA
Input Noise Voltage	$f_o = 10$ Hz		15		nV/$\sqrt{\text{Hz}}$
	$f_o = 100$ Hz		9.0		nV/$\sqrt{\text{Hz}}$
	$f_o = 1$ kHz		8.0		nV/$\sqrt{\text{Hz}}$
Input Noise Current	$f_o = 10$ Hz		1.0		pA/$\sqrt{\text{Hz}}$
	$f_o = 100$ Hz		0.3		pA/$\sqrt{\text{Hz}}$
	$f_o = 1$ kHz		0.15		pA/$\sqrt{\text{Hz}}$
Input Resistance			1.5		MΩ
Input Voltage Range		±13.5	±14		V
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	500,000	3,000,000		
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	100	120		dB
Power Supply Rejection Ratio	$R_S \leq 10$ kΩ		2.0	10	μV/V
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±13.5		V
	$R_L \geq 2$ kΩ	±10	±13.5		V
Output Resistance			150		Ω
Power Consumption			80	120	mW
The following specifications apply for $-20°C \leq T_A \leq +85°C$ unless otherwise specified:					
Input Offset Voltage (Without external trim)	$R_S \leq 10$ kΩ			2.5	mV
Average Input Offset Voltage Drift (Without external trim)	$R_S = 50$ Ω		2.0	10	μV/°C
Average Input Offset Voltage Drift (With external trim)	$R_S = 50$ Ω		0.6		μV/°C
Input Offset Current	$T_A = +85°C$		1.2	20	nA
	$T_A = -20°C$		4.0	40	nA
Average Input Offset Current Drift				300	pA/°C
Input Bias Current	$T_A = +85°C$			100	nA
	$T_A = -20°C$			200	nA
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, $T_A = +85°C$	500,000			
	$R_L \geq 2$ kΩ, $T_A = -20°C$	250,000			
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	100			dB
Power Supply Rejection Ratio	$R_S \leq 10$ kΩ			20	μV/V
Output Voltage Swing	$R_L \geq 2$ kΩ	±10			V

TYPICAL PERFORMANCE CURVES

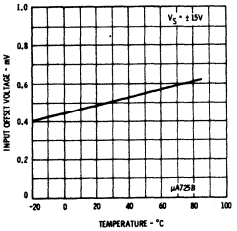
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE FOR VARIOUS SUPPLY VOLTAGES



NULLED INPUT OFFSET VOLTAGE AS A FUNCTION OF TEMPERATURE

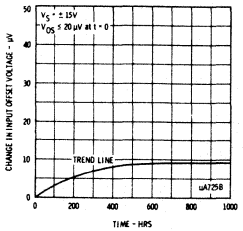


UNNULLED INPUT OFFSET VOLTAGE AS A FUNCTION OF TEMPERATURE

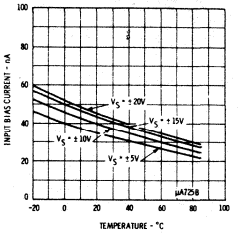


TYPICAL PERFORMANCE CURVES

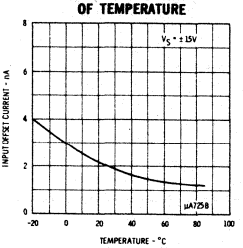
INPUT OFFSET VOLTAGE DRIFT AS A FUNCTION OF TIME



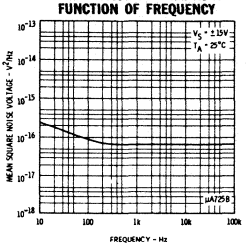
INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE



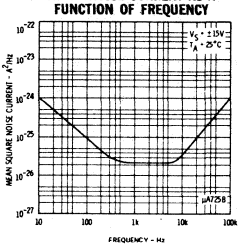
INPUT OFFSET CURRENT AS A FUNCTION OF TEMPERATURE



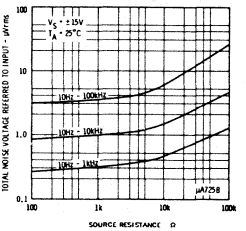
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



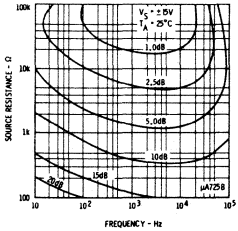
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



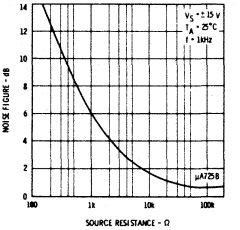
BROADBAND NOISE FOR VARIOUS BANDWIDTHS



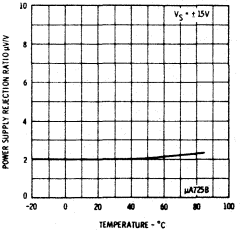
NARROW BAND SPOT NOISE FIGURE CONTOURS



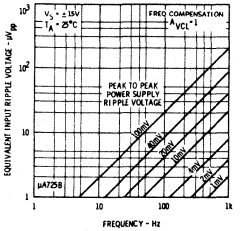
NOISE FIGURE AS A FUNCTION OF SOURCE RESISTANCE



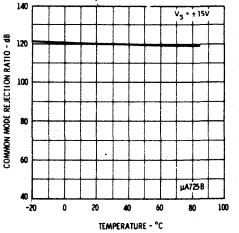
SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF TEMPERATURE



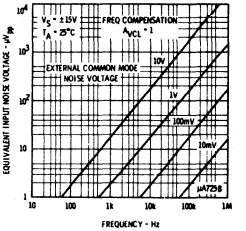
EQUIVALENT INPUT RIPPLE VOLTAGE DUE TO POWER SUPPLY RIPPLE AS A FUNCTION OF FREQUENCY



COMMON MODE REJECTION RATIO AS A FUNCTION OF TEMPERATURE

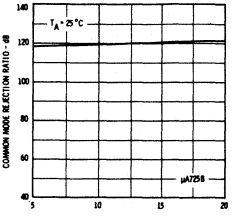


EQUIVALENT INPUT NOISE VOLTAGE DUE TO EXTERNAL COMMON MODE NOISE AS A FUNCTION OF FREQUENCY

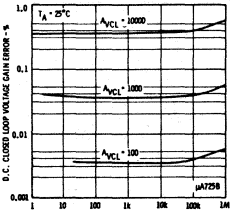


TYPICAL PERFORMANCE CURVES

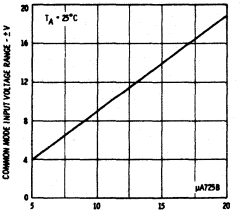
COMMON MODE REJECTION RATIO AS A FUNCTION OF SUPPLY VOLTAGE



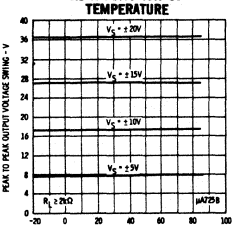
D.C. CLOSED LOOP VOLTAGE GAIN ERROR AS A FUNCTION OF SOURCE RESISTANCE



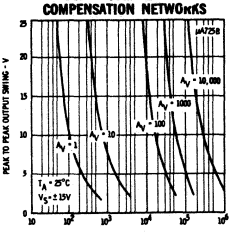
COMMON MODE INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



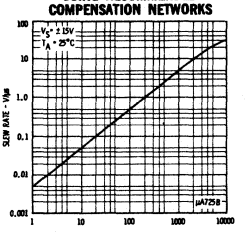
OUTPUT VOLTAGE SWING AS A FUNCTION OF TEMPERATURE



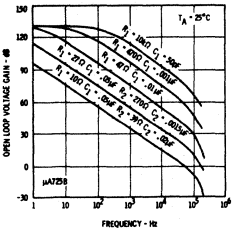
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR RECOMMENDED COMPENSATION NETWORKS



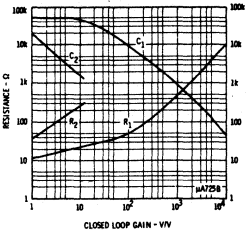
SLEW RATE AS A FUNCTION OF CLOSED-LOOP GAIN USING RECOMMENDED COMPENSATION NETWORKS



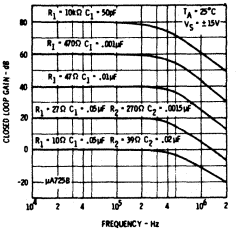
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY USING RECOMMENDED COMPENSATION NETWORKS



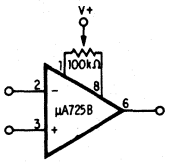
VALUES FOR SUGGESTED COMPENSATION NETWORKS FOR VARIOUS CLOSED LOOP VOLTAGE GAINS



FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS USING RECOMMENDED COMPENSATION NETWORKS



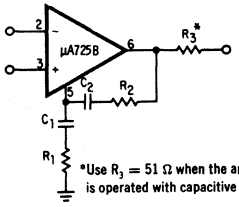
VOLTAGE OFFSET NULL CIRCUIT



COMPENSATION COMPONENT VALUES

A_{VCL}	R_1 (Ω)	C_1 (μF)	R_2 (Ω)	C_2 (μF)
10,000	10 k	50 pF	—	—
1,000	470	.001	—	—
100	47	.01	—	—
10	27	.05	270	.0015
1	10	.05	39	.02

FREQUENCY COMPENSATION CIRCUIT



*Use $R_3 = 51\ \Omega$ when the amplifier is operated with capacitive load.

DEFINITION OF TERMS

INPUT OFFSET VOLTAGE — That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the output at zero volts.

INPUT BIAS CURRENT — The average of the two input currents.

INPUT NOISE VOLTAGE — The square root of the mean square narrow-band noise voltage at the output divided by the measurement system gain with low source resistance.

INPUT NOISE CURRENT — $\sqrt{\overline{i_n}^2} = \sqrt{\dfrac{\overline{e_{meas}}^2 - 4kTR_S - \overline{e_n}^2}{R_S^2}}$ for $\Delta f = 1$ Hz

INPUT RESISTANCE — The resistance looking into either input terminal with the other grounded.

INPUT VOLTAGE RANGE — The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

LARGE-SIGNAL VOLTAGE GAIN — The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.

SUPPLY VOLTAGE REJECTION RATIO — The ratio of the change in input offset voltage to the change in supply voltage producing it.

OUTPUT VOLTAGE SWING — The peak output swing, referred to zero, that can be obtained without clipping.

OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

POWER CONSUMPTION — The DC power required to operate the amplifier with the output at zero and with no load current.

AVERAGE INPUT OFFSET VOLTAGE DRIFT — The change in input offset voltage divided by the change in ambient temperature producing it.

AVERAGE INPUT OFFSET CURRENT DRIFT — The change in input offset current divided by the change in ambient temperature producing it.

EQUIVALENT INPUT RIPPLE VOLTAGE — The change in input offset voltage due to ripple on the applied supply voltage.

EQUIVALENT INPUT COMMON MODE NOISE VOLTAGE — The change in input offset voltage due to common mode input noise.

SLEW RATE — The maximum rate of change of output voltage for a large signal input.

CLOSED LOOP VOLTAGE GAIN ERROR — Deviation from the theoretical closed loop voltage gain due to finite open loop voltage gain and input resistance, and non-zero output resistance.

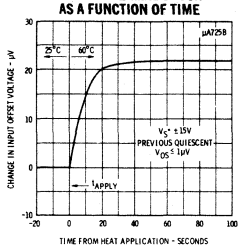
NOTE

FOR OTHER FAIRCHILD OPERATIONAL AMPLIFIERS, SEE THE FOLLOWING DATA SHEETS:

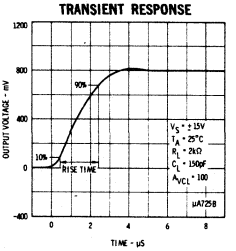
HIGH SPEED — μA715, μA715C
INSTRUMENTATION OPERATIONAL AMPLIFIER — μA725 μA725C
TEMPERATURE STABLE PREAMPS — μA727, μA727B
MICROPOWER — μA735, μA735B, μA735C
FET INPUT — μA740, μA740C
FREQUENCY COMPENSATED — μA741, μA741C
DUALS — μA739C, μA749, μA749C, μA747, μA747C
HIGH PERFORMANCE — μA748, μA748C
PRECISION — μA777, μA777B, μA777C

TYPICAL PERFORMANCE CURVES

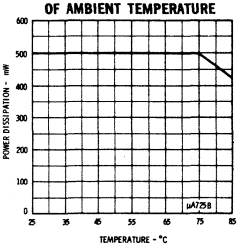
CHANGE IN INPUT OFFSET VOLTAGE DUE TO THERMAL SHOCK AS A FUNCTION OF TIME



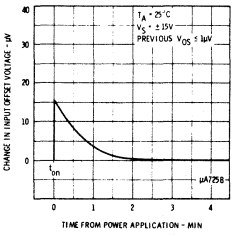
TRANSIENT RESPONSE



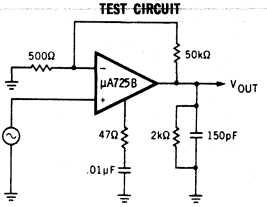
ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



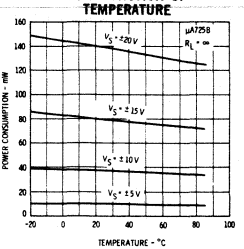
STABILIZATION TIME OF INPUT OFFSET VOLTAGE FROM POWER TURN-ON



TRANSIENT RESPONSE TEST CIRCUIT

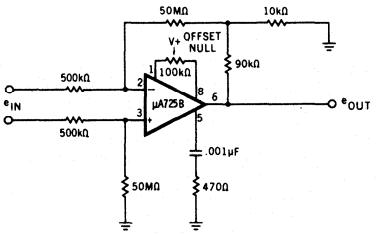


POWER CONSUMPTION AS A FUNCTION OF TEMPERATURE



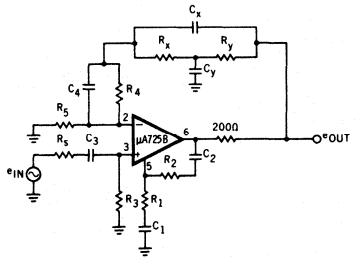
TYPICAL APPLICATIONS

PRECISION AMPLIFIER — A_{VCL} = 1000

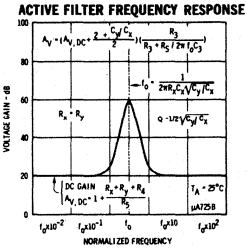


CHARACTERISTICS:
- A_{VCL} = 1000 = 60 dB
- DC Gain Error = 0.05%
- Bandwidth = 1 kHz for −0.05% error
- Diff. Input Res. = 1 MΩ
- Typical amplifying capability
  - e_{IN} = 10 μV on V_{CMI} = 1.0 V
- Caution: Minimize Stray Capacitance

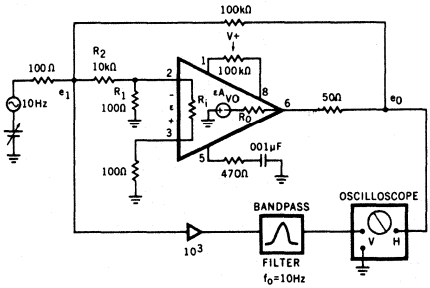
ACTIVE FILTER — BANDPASS WITH 60 dB GAIN



ACTIVE FILTER FREQUENCY RESPONSE



OPEN LOOP VOLTAGE GAIN TEST CIRCUIT



$$A_{VO} \simeq \frac{e_O}{e_1}\left(\frac{R_2 R_i + R_1 R_i + R_1 R_2}{R_1 R_i}\right) = \frac{e_O}{e_1}\,101$$

μA725C
INSTRUMENTATION OPERATIONAL AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

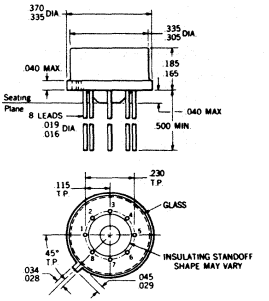
- **LOW INPUT NOISE CURRENT . . . . . 0.15 pA/$\sqrt{\text{Hz}}$**
- **HIGH OPEN LOOP GAIN 3,000,000**
- **LOW INPUT OFFSET CURRENT . . . . . 2 nA**
- **LOW INPUT VOLTAGE DRIFT . . . . . 0.6 μV/°C**
- **HIGH COMMON MODE REJECTION . . . 120 dB**
- **HIGH INPUT VOLTAGE RANGE . . . . . ±14 V**
- **WIDE POWER SUPPLY RANGE . . . . . ±3 V TO ±22 V**
- **OFFSET NULL CAPABILITY**

GENERAL DESCRIPTION — The μA725C is an instrumentation operational amplifier constructed on a single silicon chip using the Fairchild Planar* epitaxial process. It is intended for precise, low level signal amplification applications where low noise, low drift, and accurate closed loop gain are required. The offset null capability, low power consumption, very high voltage gain as well as wide power supply voltage range provide superior performance for a wide range of instrumentation applications. The μA725C is pin compatible with the popular μA741 operational amplifier. For full temperature operation (−55°C to +125°C), see μA725 data sheet. (For other Fairchild Operational Amplifiers, see Page 5.)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22 V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage (Note 2)	±22 V
Input Voltage (Note 3)	±22 V
Voltage between Offset Null and V^+	±0.5 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 60 seconds)	300°C

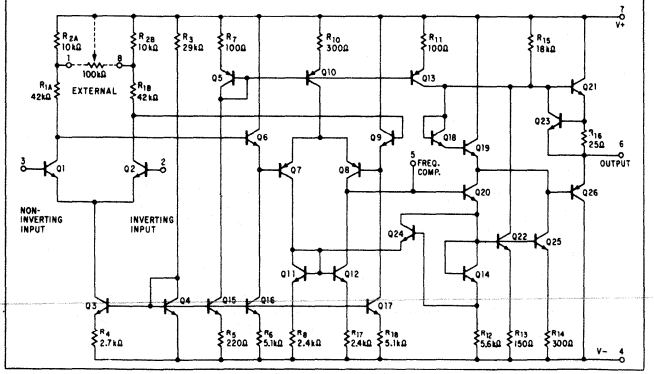
PHYSICAL DIMENSIONS
Similar to JEDEC (TO-100) outline



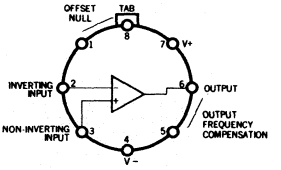
NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.22 grams

ORDER PART NO. U5T7725393

EQUIVALENT CIRCUIT



CONNECTION DIAGRAM
(TOP VIEW)



NOTE: Pin 4 connected to case

NOTES:
(1) Rating applies for case temperatures to +70°C.
(2) Rating applies for 5 ms pulses with 10% duty cycle, derate to ±5 V for continuous operation.
(3) For supply voltages less than ±22 V, the absolute maximum input voltage is equal to the supply voltage.

*Planar is a patented Fairchild process.

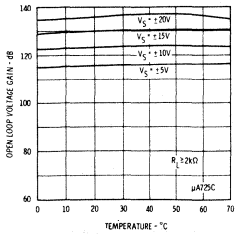
FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified)

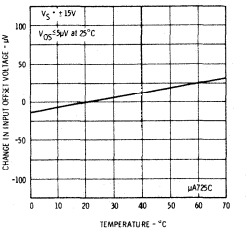
PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage (Without external trim)	$R_S \leq 10$ kΩ		0.5	2.5	mV
Input Offset Current			2.0	35	nA
Input Bias Current			42	125	nA
Input Noise Voltage	$f_o = 10$ Hz		15		nV/$\sqrt{\text{Hz}}$
	$f_o = 100$ Hz		9.0		nV/$\sqrt{\text{Hz}}$
	$f_o = 1$ kHz		8.0		nV/$\sqrt{\text{Hz}}$
Input Noise Current	$f_o = 10$ Hz		1.0		pA/$\sqrt{\text{Hz}}$
	$f_o = 100$ Hz		0.3		pA/$\sqrt{\text{Hz}}$
	$f_o = 1$ kHz		0.15		pA/$\sqrt{\text{Hz}}$
Input Resistance			1.5		MΩ
Input Voltage Range		±13.5	±14		V
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	250,000	3,000,000		
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	94	120		dB
Power Supply Rejection Ratio	$R_S \leq 10$ kΩ		2.0	35	μV/V
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±13.5		V
	$R_L \geq 2$ kΩ	±10	±13.5		V
Output Resistance			150		Ω
Power Consumption			80	150	mW
The following specifications apply for $0°C \leq T_A \leq +70°C$ unless otherwise specified:					
Input Offset Voltage (Without external trim)	$R_S \leq 10$ kΩ			3.5	mV
Average Input Offset Voltage Drift (Without external trim)	$R_S = 50$ Ω		2.0		μV/°C
Average Input Offset Voltage Drift (With external trim)	$R_S = 50$ Ω		0.6		μV/°C
Input Offset Current	$T_A = +70°C$		1.2	35	nA
	$T_A = 0°C$		4.0	50	nA
Average Input Offset Current Drift			10		pA/°C
Input Bias Current	$T_A = +70°C$			125	nA
	$T_A = 0°C$			250	nA
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, $T_A = +70°C$	125,000			
	$R_L \geq 2$ kΩ, $T_A = 0°C$	125,000			
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ		115		dB
Power Supply Rejection Ratio	$R_S \leq 10$ kΩ		20		μV/V
Output Voltage Swing	$R_L \geq 2$ kΩ	±10			V

TYPICAL PERFORMANCE CURVES

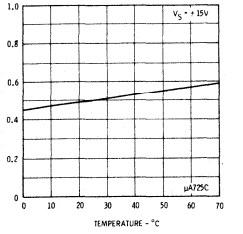
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE FOR VARIOUS SUPPLY VOLTAGES



NULLED INPUT OFFSET VOLTAGE AS A FUNCTION OF TEMPERATURE

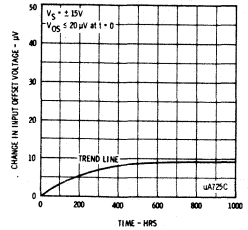


UNNULLED INPUT OFFSET VOLTAGE AS A FUNCTION OF TEMPERATURE

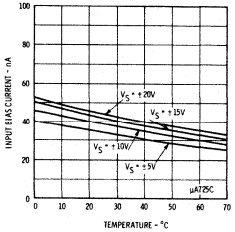


TYPICAL PERFORMANCE CURVES

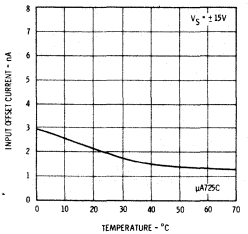
INPUT OFFSET VOLTAGE DRIFT AS A FUNCTION OF TIME



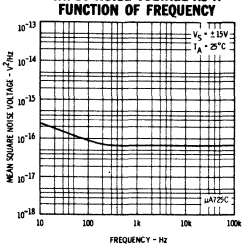
INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE



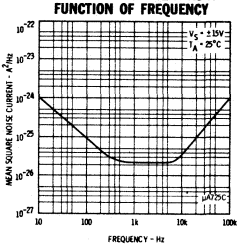
INPUT OFFSET CURRENT AS A FUNCTION OF TEMPERATURE



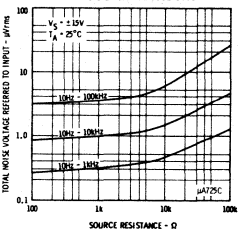
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



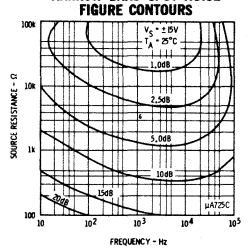
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



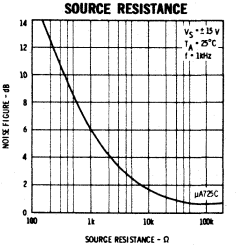
BROADBAND NOISE FOR VARIOUS BANDWIDTHS



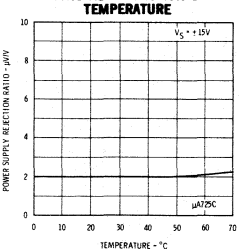
NARROW BAND SPOT NOISE FIGURE CONTOURS



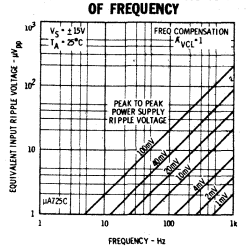
NOISE FIGURE AS A FUNCTION OF SOURCE RESISTANCE



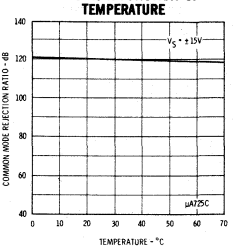
SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF TEMPERATURE



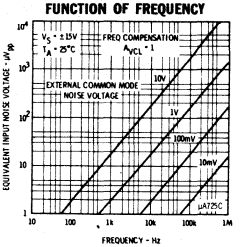
EQUIVALENT INPUT RIPPLE VOLTAGE DUE TO POWER SUPPLY RIPPLE AS A FUNCTION OF FREQUENCY



COMMON MODE REJECTION RATIO AS A FUNCTION OF TEMPERATURE

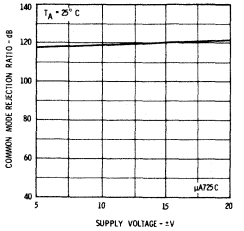


EQUIVALENT INPUT NOISE VOLTAGE DUE TO EXTERNAL COMMON MODE NOISE AS A FUNCTION OF FREQUENCY

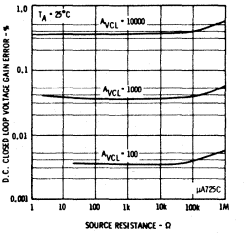


TYPICAL PERFORMANCE CURVES

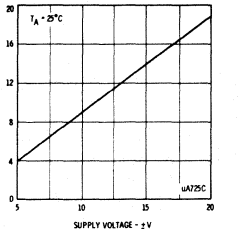
COMMON MODE REJECTION RATIO AS A FUNCTION OF SUPPLY VOLTAGE



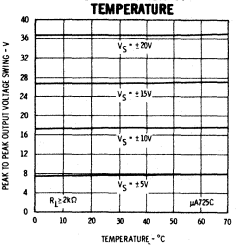
D.C. CLOSED LOOP VOLTAGE GAIN ERROR AS A FUNCTION OF SOURCE RESISTANCE



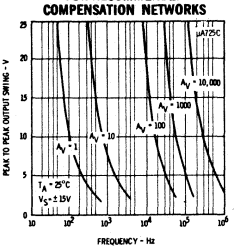
COMMON MODE INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



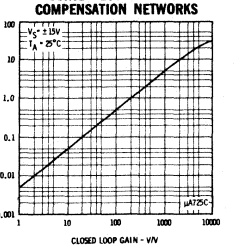
OUTPUT VOLTAGE SWING AS A FUNCTION OF TEMPERATURE



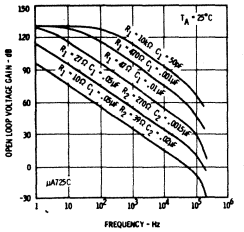
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR RECOMMENDED COMPENSATION NETWORKS



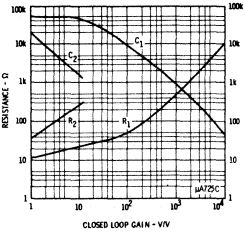
SLEW RATE AS A FUNCTION OF CLOSED-LOOP GAIN USING RECOMMENDED COMPENSATION NETWORKS



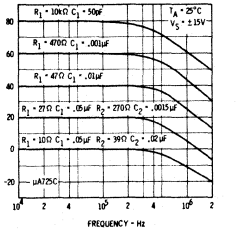
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY USING RECOMMENDED COMPENSATION NETWORKS



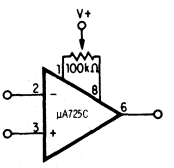
VALUES FOR SUGGESTED COMPENSATION NETWORKS FOR VARIOUS CLOSED LOOP VOLTAGE GAINS



FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS USING RECOMMENDED COMPENSATION NETWORKS



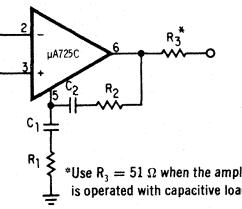
VOLTAGE OFFSET NULL CIRCUIT



COMPENSATION COMPONENT VALUES

A_{VCL}	R_1 (Ω)	C_1 (μF)	R_2 (Ω)	C_2 (μF)
10,000	10 k	50 pF	—	—
1,000	470	.001	—	—
100	47	.01	—	—
10	27	.05	270	.0015
1	10	.05	39	.02

FREQUENCY COMPENSATION CIRCUIT



*Use $R_3 = 51\ \Omega$ when the amplifier is operated with capacitive load.

DEFINITION OF TERMS

INPUT OFFSET VOLTAGE — That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the output at zero volts.

INPUT BIAS CURRENT — The average of the two input currents.

INPUT NOISE VOLTAGE — The square root of the mean square narrow-band noise voltage at the output divided by the measurement system gain with low source resistance.

INPUT NOISE CURRENT — $\sqrt{\overline{I_n}^2} = \sqrt{\dfrac{\overline{e_{meas}}^2 - 4kTR_S - \overline{e_n}^2}{R_S^2}}$ for $\Delta f = 1$ Hz

INPUT RESISTANCE — The resistance looking into either input terminal with the other grounded.

INPUT VOLTAGE RANGE — The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

LARGE-SIGNAL VOLTAGE GAIN — The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.

SUPPLY VOLTAGE REJECTION RATIO — The ratio of the change in input offset voltage to the change in supply voltage producing it.

OUTPUT VOLTAGE SWING — The peak output swing, referred to zero, that can be obtained without clipping.

OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

POWER CONSUMPTION — The DC power required to operate the amplifier with the output at zero and with no load current.

AVERAGE INPUT OFFSET VOLTAGE DRIFT — The change in input offset voltage divided by the change in ambient temperature producing it.

AVERAGE INPUT OFFSET CURRENT DRIFT — The change in input offset current divided by the change in ambient temperature producing it.

EQUIVALENT INPUT RIPPLE VOLTAGE — The change in input offset voltage due to ripple on the applied supply voltage.

EQUIVALENT INPUT COMMON MODE NOISE VOLTAGE — The change in input offset voltage due to common mode input noise.

SLEW RATE — The maximum rate of change of output voltage for a large signal input.

CLOSED LOOP VOLTAGE GAIN ERROR — Deviation from the theoretical closed loop voltage gain due to finite open loop voltage gain and input resistance, and non-zero output resistance.

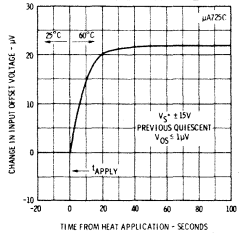
NOTE:

FOR OTHER FAIRCHILD OPERATIONAL AMPLIFIERS, SEE THE FOLLOWING DATA SHEETS:

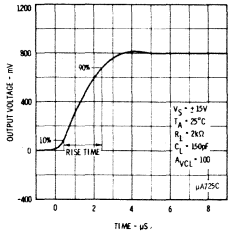
HIGH SPEED — μA715, μA715C
INSTRUMENTATION OPERATIONAL AMPLIFIER — μA725, μA725B
TEMPERATURE STABLE PREAMPS — μA727, μA727B
MICROPOWER — μA735, μA735B, μA735C
FET INPUT — μA740, μA740C
FREQUENCY COMPENSATED — μA741, μA741C
DUALS — μA739C, μA749, μA749C, μA747, μA747C
HIGH PERFORMANCE — μA748, μA748C
PRECISION — μA777, μA777B, μA777C

TYPICAL PERFORMANCE CURVES

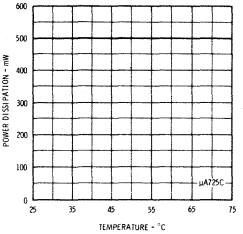
CHANGE IN INPUT OFFSET VOLTAGE DUE TO THERMAL SHOCK AS A FUNCTION OF TIME



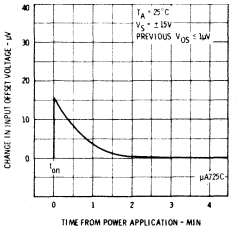
TRANSIENT RESPONSE



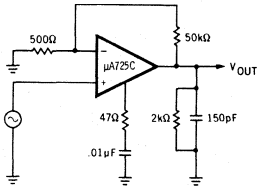
ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



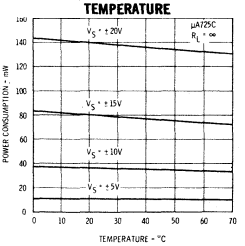
STABILIZATION TIME OF INPUT OFFSET VOLTAGE FROM POWER TURN-ON



TRANSIENT RESPONSE TEST CIRCUIT

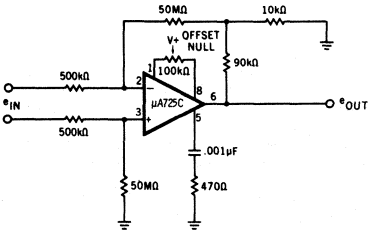


POWER CONSUMPTION AS A FUNCTION OF TEMPERATURE



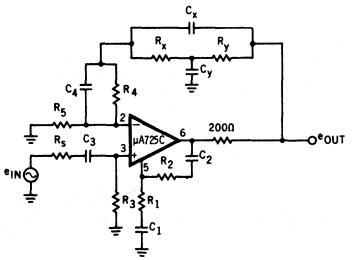
TYPICAL APPLICATIONS

PRECISION AMPLIFIER — A_{VCL} = 1000

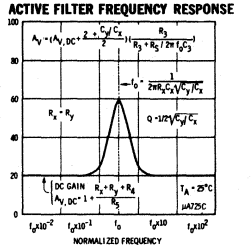


CHARACTERISTICS:
- A_{VCL} = 1000 = 60 dB
- DC Gain Error = 0.05%
- Bandwidth = 1 kHz for −0.05% error
- Diff. Input Res. = 1 MΩ
- Typical amplifying capability
  - e_{IN} = 10 μV on V_{CM} = 1.0 V
- Caution: Minimize Stray Capacitance

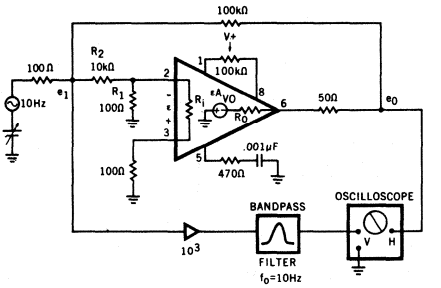
ACTIVE FILTER — BANDPASS WITH 60 dB GAIN



ACTIVE FILTER FREQUENCY RESPONSE



OPEN LOOP VOLTAGE GAIN TEST CIRCUIT



$$A_{VO} \simeq \frac{e_0}{e_1}\left(\frac{R_2 R_i + R_1 R_i + R_1 R_2}{R_1 R_i}\right) = \frac{e_0}{e_1} 101$$

μA726
TEMPERATURE-CONTROLLED DIFFERENTIAL PAIR
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA726 is a monolithic transistor pair in a high thermal-resistance package, held at a constant temperature by active temperature regulator circuitry. The transistor pair displays the excellent matching, close thermal coupling, and fast thermal response inherent in monolithic construction. The high gain and low standby dissipation of the regulator circuit permits tight temperature control over a wide range of ambient temperatures. It is intended for use as an input stage in very-low-drift dc amplifiers, replacing complex chopper-stabilized amplifiers; it is also useful as the nonlinear element in logarithmic amplifiers and multipliers where the highly predictable exponential relation between emitter-base voltage and collector current is employed. The device is constructed on a single silicon chip using the Fairchild Planar° process.

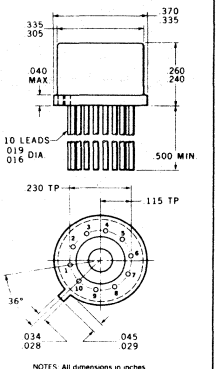
ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 60 seconds)	300°C
Supply Voltage	±18 V

MAXIMUM RATINGS FOR EACH TRANSISTOR

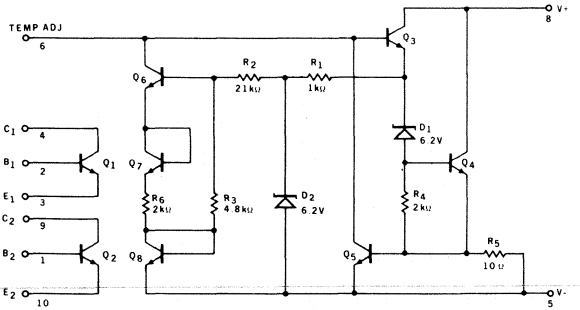
Maximum collector-to-substrate voltage	40 V
BV_{CBO}	40 V
LV_{CEO} [Note 1]	30 V
BV_{EBO}	5 V
Collector Current	5 mA

PHYSICAL DIMENSIONS

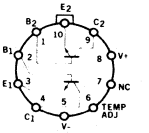


ORDER PART NO. U5U7726312

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



TOP VIEW

Note 1: Measured at 1 mA collector current.

° Planar is a patented Fairchild process.

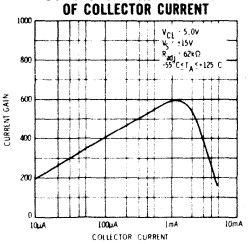
FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS ($-55°C \leq T_A \leq +125°C$, $V_S = \pm 15$ V, $R_{adj} = 62$ kΩ unless otherwise specified)

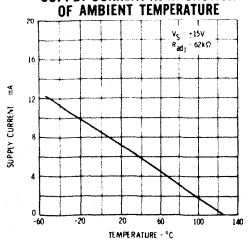
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$10\ \mu A \leq I_C \leq 100\ \mu A$ $V_{CE} = 5$ V, $R_S \leq 50\Omega$		1.0	2.5	mV
Input Offset Current	$I_C = 10\ \mu A$, $V_{CE} = 5$ V		10	50	nA
Input Offset Current	$I_C = 100\ \mu A$, $V_{CE} = 5$ V		50	200	nA
Average Input Bias Current	$I_C = 10\ \mu A$, $V_{CE} = 5$ V		50	150	nA
Average Input Bias Current	$I_C = 100\ \mu A$, $V_{CE} = 5$ V		250	500	nA
Offset Voltage Change	$I_C = 10\ \mu A$, $5\text{ V} \leq V_{CE} \leq 25$ V, $R_S \leq 100$ kΩ		0.3	6.0	mV
Offset Voltage Change	$I_C = 100\ \mu A$, $5\text{ V} \leq V_{CE} \leq 25$ V, $R_S \leq 10$ kΩ		0.3	6.0	mV
Input Offset Voltage Drift	$10\ \mu A \leq I_C \leq 100\ \mu A$, $V_{CE} = 5$ V, $R_S \leq 50\Omega$, $+25°C \leq T_A \leq +125°C$		0.2	1.0	μV/°C
Input Offset Voltage Drift	$10\mu A \leq I_C \leq 100\ \mu A$, $V_{CE} = 5$ V, $R_S \leq 50\Omega$, $-55°C \leq T_A \leq +25°C$		0.2	1.0	μV/°C
Input Offset Current Drift	$I_C = 10\ \mu A$, $V_{CE} = 5$ V		10		pA/°C
Input Offset Current Drift	$I_C = 100\ \mu A$, $V_{CE} = 5$ V		30		pA/°C
Supply Voltage Rejection Ratio	$10\mu A \leq I_C \leq 100\ \mu A$, $R_S \leq 50\Omega$,		25		μV/V
Low-Frequency Noise	$I_C = 10\ \mu A$, $V_{CE} = 5$ V, $R_S \leq 50\Omega$ BW = .001 Hz to 0.1 Hz		4.0		μV pp
Broadband Noise	$I_C = 10\ \mu A$, $V_{CE} = 5$ V, $R_S \leq 50\Omega$ BW = 0.1 Hz to 10 kHz		10		μV pp
Long-term Drift	$10\ \mu A \leq I_C \leq 100\ \mu A$, $V_{CE} = 5$ V, $R_S \leq 50\Omega$, $T_A = 25°C$		5.0		μV/week
High Frequency Current Gain	f = 20 MHz, $I_C = 100\ \mu A$, $V_{CE} = 5$ V	1.5	3.5		
Output Capacitance	$I_E = 0$, $V_{CB} = 5$ V		1.0		pF
Emitter Transition Capacitance	$I_E = 100\ \mu A$		1.0		pF
Collector Saturation Voltage	$I_B = 100\ \mu A$, $I_C = 1$ mA		0.5	1.0	V

TYPICAL PERFORMANCE CURVES

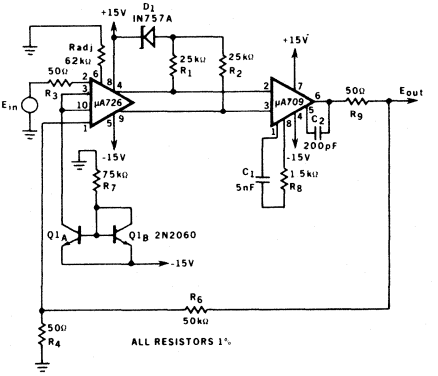
CURRENT GAIN AS A FUNCTION OF COLLECTOR CURRENT



SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



TYPICAL X1000 CIRCUIT



μA726C
TEMPERATURE-CONTROLLED DIFFERENTIAL PAIR
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION—The μA726C is a monolithic transistor pair in a high thermal-resistance package, held at a constant temperature by active temperature regulator circuitry. The transistor pair displays the excellent matching, close thermal coupling, and fast thermal response inherent in monolithic construction. The high gain and low standby dissipation of the regulator circuit permits tight temperature control over a wide range of ambient temperatures. It is intended for use as an input stage in very-low-drift dc amplifiers, replacing complex chopper-stabilized amplifiers; it is also useful as the nonlinear element in logarithmic amplifiers and multipliers where the highly predictable exponential relation between emitter-base voltage and collector current is employed. The device is constructed on a single silicon chip using the Fairchild Planar* process. For full temperature range (−55°C to +125°C) see μA726 data sheet.

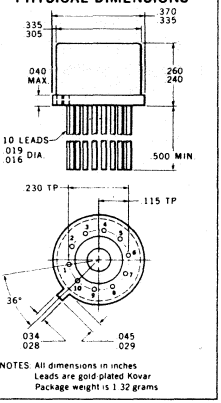
ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	0°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	300°C
Supply Voltage	±18V

MAXIMUM RATINGS FOR EACH TRANSISTOR

Maximum collector-to-substrate voltage	40V
BV_{CBO}	40V
LV_{CEO} (Note 1)	30V
BV_{EBO}	5V
Collector Current	5 mA

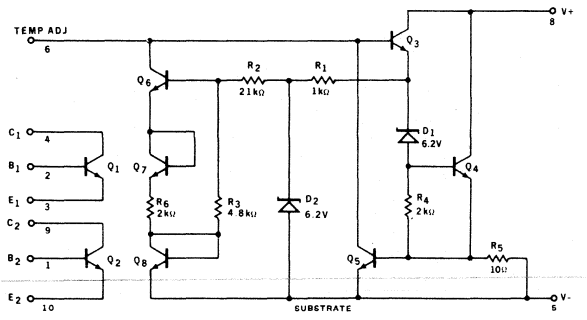
PHYSICAL DIMENSIONS



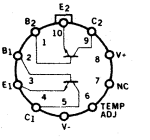
NOTES: All dimensions in inches
Leads are gold plated Kovar
Package weight is 1.32 grams

ORDER PART NO. U5U7726323

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



TOP VIEW

NOTE: (1) Measured at 1 mA collector current.

*Planar is a patented Fairchild process.

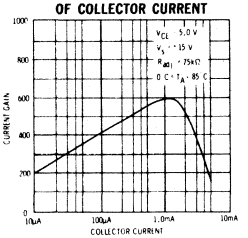
FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +85°C$, $V_S = \pm 15V$, $R_{adj} = 75\ k\Omega$ unless otherwise specified)

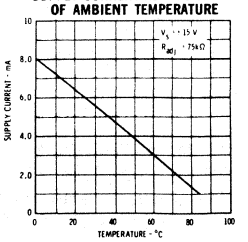
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$10\ \mu A \leq I_C \leq 100\ \mu A$ $V_{CE} = 5V$, $R_S \leq 50\Omega$		1.0	3.0	mV
Input Offset Current	$I_C = 10\ \mu A$, $V_{CE} = 5V$		10	100	nA
Input Offset Current	$I_C = 100\ \mu A$, $V_{CE} = 5V$		50	400	nA
Average Input Bias Current	$I_C = 10\ \mu A$, $V_{CE} = 5V$		50	300	nA
Average Input Bias Current	$I_C = 100\ \mu A$, $V_{CE} = 5V$		250	1000	nA
Offset Voltage Change	$I_C = 10\ \mu A$, $5V \leq V_{CE} \leq 25V$, $R_S \leq 100\ k\Omega$		0.3	6.0	mV
Offset Voltage Change	$I_C = 100\ \mu A$, $5V \leq V_{CE} \leq 25V$, $R_S \leq 10\ k\Omega$		0.3	6.0	mV
Input Offset Voltage Drift	$I_C = 100\ \mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$		0.2	2.0	μV/°C
Input Offset Current Drift	$I_C = 10\ \mu A$, $V_{CE} = 5V$		10		pA/°C
Input Offset Current Drift	$I_C = 100\ \mu A$, $V_{CE} = 5V$		30		pA/°C
Supply Voltage Rejection Ratio	$I_C = 100\ \mu A$, $R_S = 50\Omega$		25		μV/V
Low-Frequency Noise	$I_C = 10\ \mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$, BW = 0.001 Hz to 0.1 Hz		4.0		μV pp
Broadband Noise	$I_C = 10\ \mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$, BW = 0.1 Hz to 10 kHz		10		μV pp
Long-Term Drift	$I_C = 100\ \mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$, $T_A = 25°C$		5.0		μV/week
High-Frequency Current Gain	f = 20 MHz, $I_C = 100\ \mu A$, $V_{CE} = 5V$	1.5	3.5		
Output Capacitance	$I_E = 0$, $V_{CB} = 5V$		1.0		pF
Emitter Transition Capacitance	$I_E = 100\ \mu A$		1.0		pF
Collector Saturation Voltage	$I_B = 100\ \mu A$, $I_C = 1\ mA$		0.5	1.0	V

TYPICAL PERFORMANCE CURVES

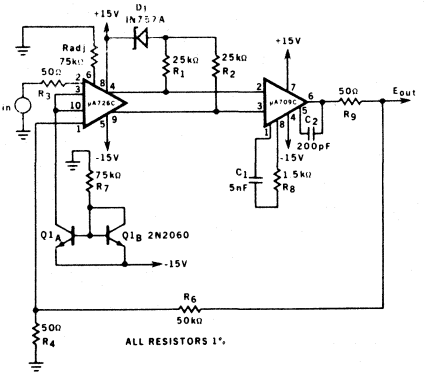
CURRENT GAIN AS A FUNCTION OF COLLECTOR CURRENT



SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



TYPICAL X1000 CIRCUIT



μA727
TEMPERATURE-CONTROLLED DIFFERENTIAL PREAMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

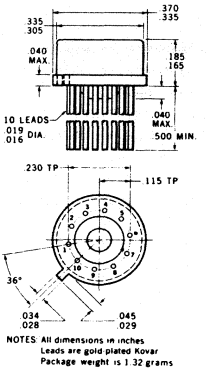
FEATURES
- **VERY LOW OFFSET DRIFTS**
- **HIGH INPUT IMPEDANCE**
- **WIDE COMMON MODE RANGE**

GENERAL DESCRIPTION — The μA727 is a monolithic, fixed gain, differential-input differential-output amplifier, constructed with the Fairchild Planar* epitaxial process, mounted in a high thermal-resistance package, and held at constant temperature by active regulator circuitry. The high gain and low standby dissipation of the regulator circuit give tight temperature control over a wide ambient temperature range. The device is intended for use as a self-contained input stage in very low-drift DC amplifiers, replacing complex chopper-stabilized amplifiers in such applications as thermo-couple bridges, strain gage transducers, and A to D converters.

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 second time limit)	300°C
Supply Voltage (Amplifier and Heater)	±18 V
Differential Input Voltage	±10 V
Common Mode Input Voltage	±15 V

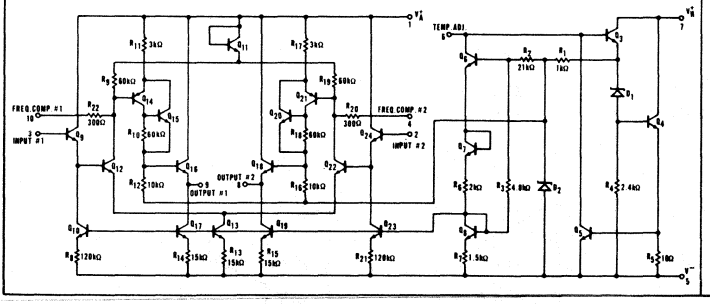
PHYSICAL DIMENSIONS
(In accordance with JEDEC TO-100)



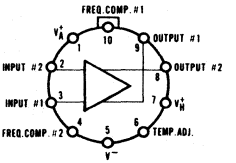
NOTES: All dimensions in inches
Leads are gold plated Kovar
Package weight is 1.32 grams

ORDER PART NO. U5U7726312

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(Top View)



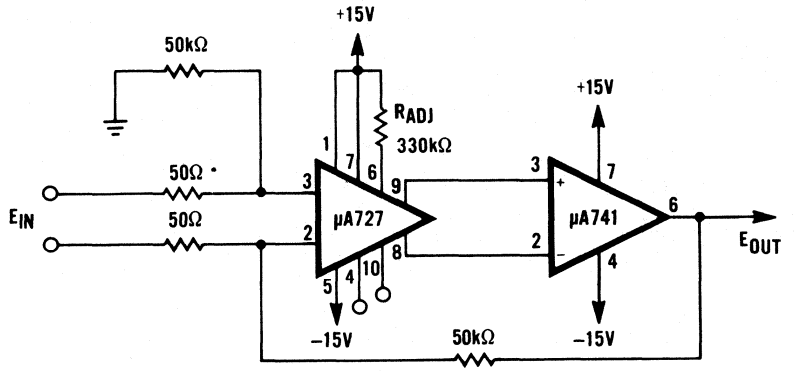
*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS ($-55°C \leq T_A \leq +125°C$, $V_{H^+} = V_A{}^+ = +15\ V$, $V^- = -15\ V$, $R_{ADJ} = 330\ k\Omega$, unless otherwise specified)

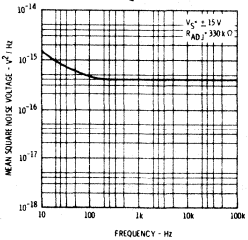
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 50\ \Omega$		2.0	10	mV
Input Offset Current			2.5	15	nA
Input Bias Current			12	40	nA
Input Offset Voltage Drift	$R_S \leq 50\ \Omega$, $+25°C \leq T_A \leq +125°C$		0.6	1.5	μV/°C
	$R_S \leq 50\ \Omega$, $-55°C \leq T_A \leq +25°C$		0.6	1.5	μV/°C
Input Offset Current Drift	$+25°C \leq T_A \leq +125°C$		2.0		pA/°C
	$-55°C \leq T_A \leq +25°C$		2.0		pA/°C
Input Bias Current Drift	$-55°C \leq T_A \leq +125°C$		15		pA/°C
Differential Input Resistance			300		MΩ
Common Mode Input Resistance			1000		MΩ
Input Voltage Range		±12	±13		V
Supply Voltage Rejection Ratio	$R_S \leq 100\ k\Omega$		80		μV/V
Common Mode Rejection Ratio	$R_S \leq 100\ k\Omega$	80	100		dB
Output Resistance			1.0	4.0	kΩ
Output Common Mode Voltage		−6.0	−5.0	−4.0	V
Differential Output Voltage Swing		±5.0	±7.0	±10	V
Output Sink Current		10	30	80	μA
Differential Load Rejection			5.0	10	μV/μA
Differential Voltage Gain		60	100	250	
Low Frequency Noise	BW = 10 Hz to 500 Hz, $R_S \leq 50\ \Omega$		3.0		μVrms
Long Term Drift	$R_S \leq 50\ \Omega$		5.0		μV/week
Amplifier Supply Current	$T_A = +25°C$		1.0	2.0	mA
Heater Supply Current	$T_A = +25°C$		10	15	mA

TYPICAL X1000 CIRCUIT

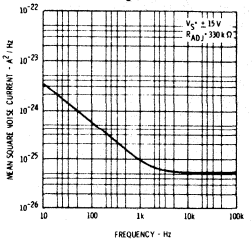


TYPICAL PERFORMANCE CURVES

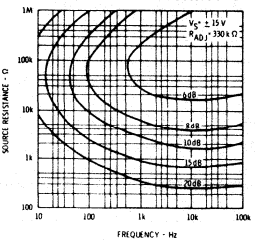
NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



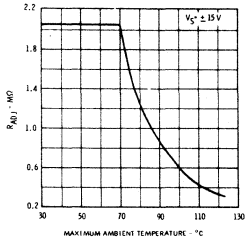
NOISE CURRENT AS A FUNCTION OF FREQUENCY



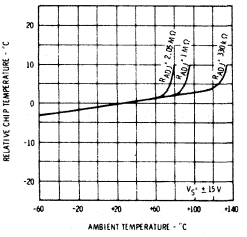
SPOT NOISE FIGURE CONTOURS



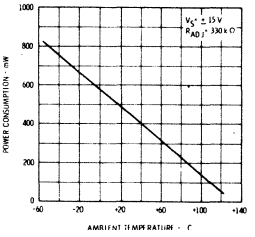
RECOMMENDED R_{ADJ} AS A FUNCTION OF MAXIMUM AMBIENT TEMPERATURE



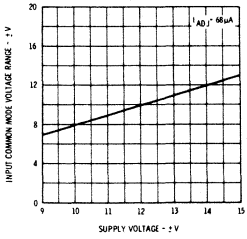
RELATIVE CHIP TEMPERATURE AS A FUNCTION OF AMBIENT TEMPERATURE



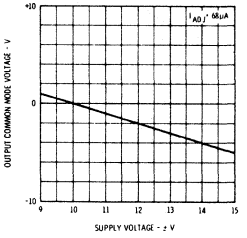
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



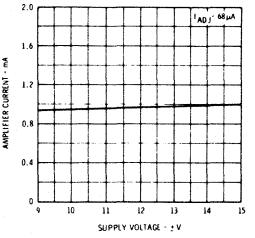
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



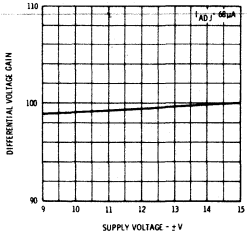
OUTPUT COMMON MODE VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



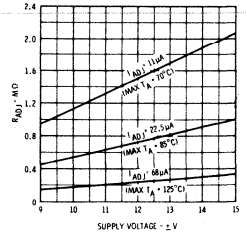
AMPLIFIER CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



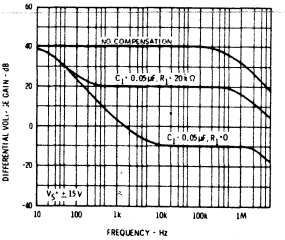
DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



REQUIRED R_{ADJ} FOR CONSTANT I_{ADJ} AS A FUNCTION OF SUPPLY VOLTAGE



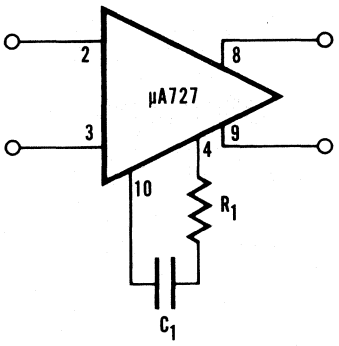
OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF COMPENSATION



DEFINITION OF TERMS

INPUT OFFSET VOLTAGE — That voltage which must be applied between the input terminals to obtain zero differential output voltage.
INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the differential output at zero.
DIFFERENTIAL INPUT RESISTANCE — The resistance looking into either input terminal with the other grounded.
COMMON MODE INPUT RESISTANCE — The resistance looking into both inputs tied together.
INPUT BIAS CURRENT — The average of the two input currents.
INPUT VOLTAGE RANGE — A range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.
INPUT COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.
DIFFERENTIAL VOLTAGE GAIN — The ratio of the change in differential output voltage to the change in differential input voltage producing it.
DIFFERENTIAL OUTPUT VOLTAGE SWING — The peak differential output swing that can be obtained without clipping.
OUTPUT RESISTANCE — The resistance seen looking into either output terminal with the differential output at zero.
SUPPLY VOLTAGE REJECTION RATIO — The ratio of the change in input offset voltage to the change in supply voltage producing it.
OUTPUT COMMON MODE VOLTAGE — The average voltage at the two output terminals referred to ground.
OUTPUT SINK CURRENT — The maximum negative current that can be supplied by each output.
DIFFERENTIAL LOAD REJECTION — The ratio of the change in input offset voltage to the change in differential load current producing it.
I_{AO} — The current into terminal 6.

FREQUENCY COMPENSATION CIRCUIT



μA727B
TEMPERATURE-CONTROLLED DIFFERENTIAL PREAMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

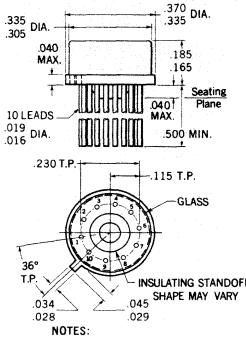
- **VERY LOW OFFSET DRIFTS**
- **HIGH INPUT IMPEDANCE**
- **WIDE COMMON MODE RANGE**

GENERAL DESCRIPTION — The μA727B is a monolithic, fixed gain, differential-input differential-output amplifier, constructed with the Fairchild Planar* epitaxial process, mounted in a high thermal-resistance package, and held at constant temperature by active regulator circuitry. The high gain and low standby dissipation of the regulator circuit give tight temperature control over a wide ambient temperature range. The device is intended for use as a self-contained input stage in very low-drift DC amplifiers, replacing complex chopper-stabilized amplifiers in such applications as thermo-couple bridges, strain gage transducers, and A to D converters. For full temperature range operation (−55°C to +125°C) see μA727 data sheet.
(For other Fairchild Operational Amplifiers, see listing on back page.)

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−20°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 second time limit)	300°C
Supply Voltage (Amplifier and Heater)	±18 V
Differential Input Voltage	±10 V
Common Mode Input Voltage	±15 V

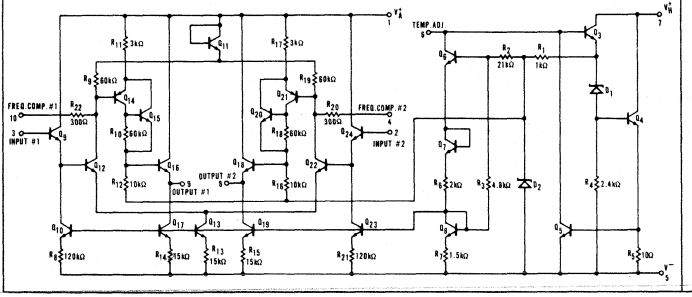
PHYSICAL DIMENSIONS
(in accordance with JEDEC (TO-100) outline)



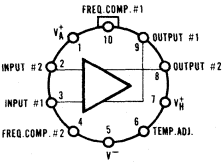
NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.32 grams

ORDER PART NO. U5U7727333

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(top view)



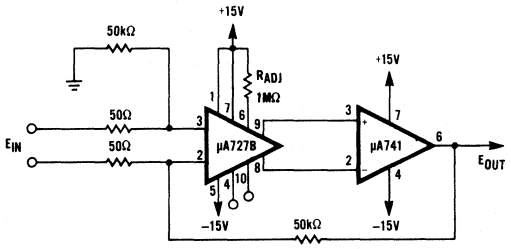
*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS ($-20°C \leq T_A \leq +85°C$, $V_H^+ = V_A^+ = +15\,V$, $V^- = -15\,V$, $R_{ADJ} = 1M\Omega$, unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 50\,\Omega$		2.0	10	mV
Input Offset Current			2.5	25	nA
Input Bias Current			12	75	nA
Input Offset Voltage Drift	$R_S \leq 50\,\Omega$		0.6	3.0	μV/°C
Input Offset Current Drift			2.0		pA/°C
Input Bias Current Drift			15		pA/°C
Differential Input Resistance			300		MΩ
Common Mode Input Resistance			1000		MΩ
Input Voltage Range		±12	±13		V
Supply Voltage Rejection Ratio	$R_S \leq 100\,k\Omega$		80		μV/V
Common Mode Rejection Ratio	$R_S \leq 100\,k\Omega$	70	100		dB
Output Resistance			1.0	4.0	kΩ
Output Common Mode Voltage		−7.0	−5.0	−4.0	V
Differential Output Voltage Swing		±3.0	±7.0	±10	V
Output Sink Current		10	30	80	μA
Differential Load Rejection			5.0	15	μV/μA
Differential Voltage Gain		50	100	250	
Low Frequency Noise	BW = 10 Hz to 500 Hz, $R_S \leq 50\,\Omega$		3.0		μV_{rms}
Long Term Drift	$R_S \leq 50\,\Omega$		5.0		μV/week
Amplifier Supply Current	$T_A = +25°C$		1.0	2.0	mA
Heater Supply Current	$T_A = +25°C$		10	15	mA

TYPICAL X1000 CIRCUIT



NOTES:

1. FOR OTHER FAIRCHILD OPERATIONAL AMPLIFIERS, SEE THE FOLLOWING DATA SHEETS:
   - HIGH SPEED — μA715, μA715C
   - TEMPERATURE STABLE PREAMPS — μA727,
   - MICROPOWER — μA735, μA735B, μA735C
   - FET INPUT — μA740, μA740B, μA740C
   - FREQUENCY COMPENSATED — μA741, μA741C
   - DUALS — μA739C, μA749, μA749C, μA747, μA747C
   - HIGH PERFORMANCE — μA748, μA748C
   - PRECISION — μA777, μA777B, μA777C

μA729
FM STEREO MULTIPLEX DECODER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

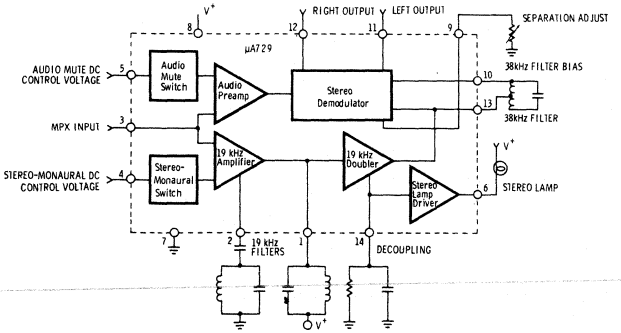
- **55 dB CHANNEL SEPARATION, EXTERNALLY ADJUSTABLE**
- **55 dB STORECAST REJECTION WITHOUT SCA FILTERS**
- **HIGH-CURRENT STEREO INDICATOR LAMP DRIVER**
- **OPERATION WITH 8 V TO 14 V SUPPLIES**
- **INTERNAL STEREO SWITCHING AND AUDIO MUTING FUNCTIONS**

GENERAL DESCRIPTION — The μA729 is a monolithic FM Stereo Multiplex Decoder System constructed on a single silicon chip using the Fairchild Planar* Epitaxial Process. This integrated circuit accomplishes the demodulation of a Stereo Multiplex Signal into the Right and Left audio channels while inherently suppressing SCA frequency components. Internal provision is made for interstation audio muting, stereo/mono mode switching and driving an external stereo mode indicator lamp. The excellent performance, wide supply range and low external parts requirement makes the μA729 suitable for all line-operated and automotive FM Stereo Multiplex applications. For Stereo Decoding with internal separation adjustment, see the μA732 Data Sheet. For stereo decoding without automatic muting and stereo switching, see the μA767 Data Sheet. See Note 1.

ABSOLUTE MAXIMUM RATINGS

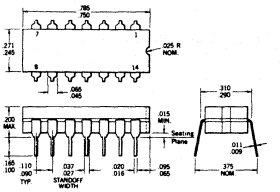
Supply Voltage (Note 2)	+15 V
Voltage at Stereo Lamp Driver Terminal	+22 V
Current into Stereo Lamp Driver Terminal (Note 3)	100 mA
Internal Power Dissipation	400 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 10 Sec.)	+260°C

BLOCK DIAGRAM



PHYSICAL DIMENSIONS

In accordance with JEDEC (TO-116) outline

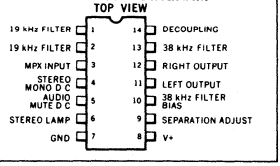


NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams

ORDER PART NO. U6A7729394

CONNECTION DIAGRAM

TOP VIEW



Notes on Page 2.

*Planar is a patented Fairchild process.

FAIRCHILD SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V^+ = +12$ V, 200 mV RMS Standard Stereo Multiplex signal applied to Input, unless otherwise specified (Note 4). Refer to Test Circuit of Figure 1.)

PARAMETER	MIN.	TYP.	MAX.	UNITS
Supply Current		10	18	mA
Input Resistance	12	20		kΩ
Stereo Separation (Adjusted)				
f = 100 Hz		45		dB
f = 1 kHz	30	55		dB
f = 10 kHz	20	50		dB
Channel Balance (Monaural Input)		0.2		dB
Total Harmonic Distortion		0.5	1.0	%
Voltage Gain		1.0		V/V
67 kHz Storecast Rejection (Note 5)		55		dB
19 kHz Pilot Level Required at Input for:				
Stereo Indicator Lamp on		12	22	mV RMS
Stereo Indicator Lamp off	4.0	8.0		mV RMS
DC Voltage Required at Pin 4 for Stereo-Monaural Switching				
Stereo on	1.0	1.25	1.5	V DC
Stereo off	0.6	0.85	1.0	V DC
DC Voltage Required at Pin 5 for Audio Mute Switching				
Audio on	1.0	1.20	1.5	V DC
Audio off	0.6	0.85	1.0	V DC
Mute Attenuation of Audio	45	55		dB
High Frequency Audio Components in Left and Right Outputs (dB below 1 kHz output)				
19 kHz		30		dB
38 kHz		25		dB

NOTES:

(1) The μA729 is a plug-in replacement for the MC1305. For μA729 applications information, and other Fairchild Communications Integrated circuits see listing on last page.

(2) Power supply transients up to 22V are permissible for periods of 15 seconds. However, extended operation at voltages greater than 15V should be avoided as the maximum allowable internal power dissipation for this device may be exceeded.

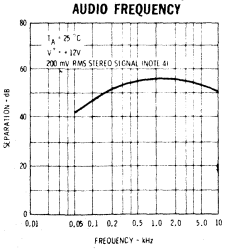
(3) Rating applies to steady state current. Maximum permissible surge current during turn-on of the Stereo Indicator Lamp is 500 mA.

(4) "Standard Stereo Multiplex Signal" here refers to a 200mV RMS (0.56V p-p) composite stereo signal including 10% pilot with L = 1 and R = 1 as described in the FCC Rules on FM Broadcasting.

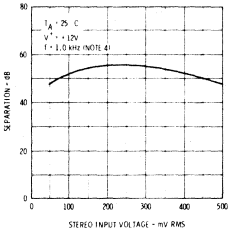
(5) Measured with a stereo composite signal consisting of 80% stereo, 10% pilot and 10% SCA as defined in the FCC Rules on FM Broadcasting.

TYPICAL PERFORMANCE CURVES

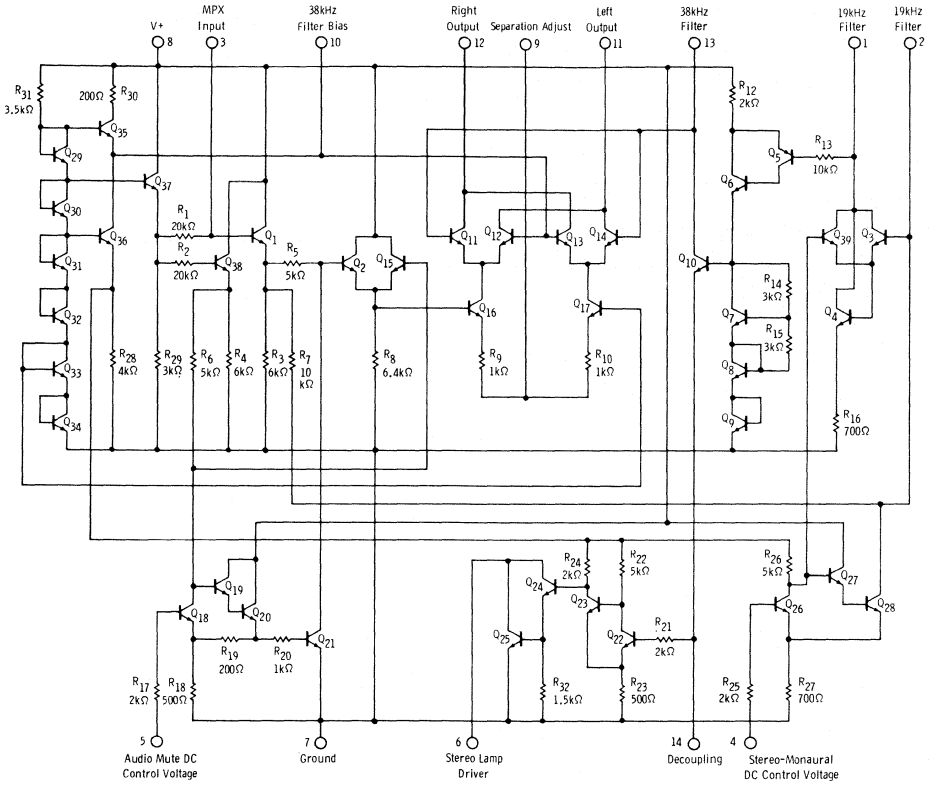
SEPARATION VERSUS AUDIO FREQUENCY



1 kHz SEPARATION VERSUS COMPOSITE INPUT VOLTAGE

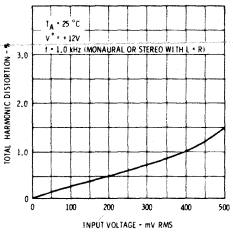


μA729 FM STEREO MULTIPLEX DECODER EQUIVALENT CIRCUIT

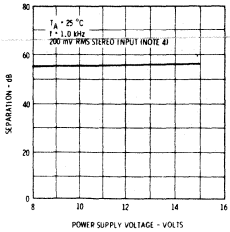


TYPICAL PERFORMANCE CURVES

1 kHz DISTORTION VERSUS INPUT VOLTAGE



1 kHz SEPARATION VERSUS POWER SUPPLY VOLTAGE



μA729 FM STEREO MULTIPLEX DECODER TEST CIRCUIT AND TYPICAL APPLICATION

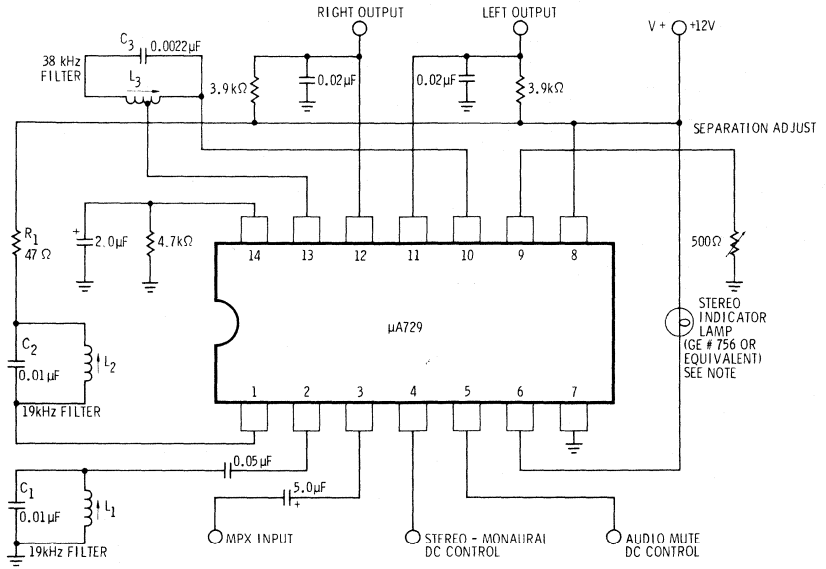


Fig. 1

NOTES:
(1) Capacitors C_1, C_2 and C_3 should be polystyrene or mylar.
(2) Coils L_1 and L_2 are 7.0 mH nominal with $Q_{@1} = 60$ (Miller #1361 or equivalent).
(3) Coil L_3 is 8.0 mH nominal with $Q_{@1} = 80$, tapped at 10:1 turns ratio. (Miller #1362 or equivalent).
(4) Resistor R_1 can be increased (or decreased) in value to increase (or decrease) the 19kHz sensitivity.

μA729 APPLICATIONS INFORMATION:

APP BRIEF 150 — The μA729 and μA732 Integrated Circuit Stereo Multiplex Decoders.
APP BRIEF 151 — A High Quality AM/FM Stereo Receiver.

FOR INFORMATION ON OTHER FAIRCHILD COMMUNICATIONS INTEGRATED CIRCUITS, SEE THE FOLLOWING DATA SHEETS:

RF/IF LIMITING AMP — μA703C
RF/IF LIMITING AMP — μA703D
FIXED GAIN, LOW DISTORTION AMP — μA716C
HIGH FREQUENCY COMMUNICATIONS SYSTEM μA719C
FM STEREO MULTIPLEX DECODER μA732
DUAL LOW NOISE HIGH GAIN OP-AMP μA739C
DUAL AC AMP μA745
COLOR TV CHROMA DEMODULATOR μA746
DUAL A.C. AMPLIFIER μA749D
TV/FM SOUND SYSTEM μA754C
GAIN CONTROLLED IF AMP μA757C
FM STEREO MULTIPLEX DECODER μA767
BALANCED MODULATOR-DEMODULATOR μA796C

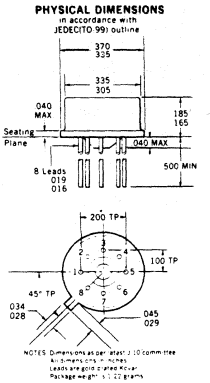
μA730
DIFFERENTIAL AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA730 is a differential amplifier constructed on a single silicon-chip using the Fairchild Planar* epitaxial process. This device has a wide range of applications since it has both a differential input and output; any combination of single-ended or differential configurations can be employed at its input and output. The emitter follower output stage gives this device a low output impedance making it useful as a preamplifier.

ABSOLUTE MAXIMUM RATINGS

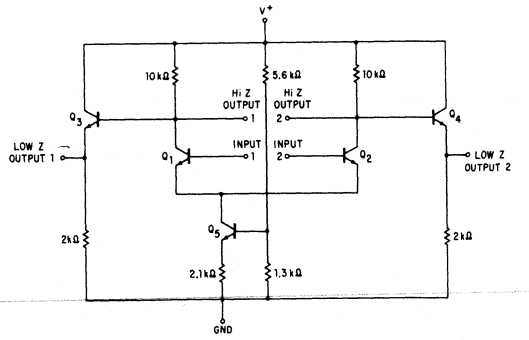
Supply Voltage	15 V
Differential Input Voltage	±5 V
Common Mode Input Voltage	2.5 to 5.5 V
Internal Power Dissipation (Note 1)	300 mW
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	+300°C

PHYSICAL DIMENSIONS
in accordance with JEDEC(TO-99) outline

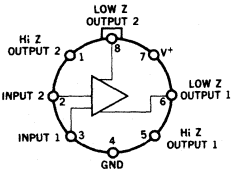


ORDER PART NO. U5B7730312

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(Top View)



Note: Pin 4 connected to case

NOTES:
(1) Rating applies for case temperature to +125°C; derate linearly at 5.6 mW/°C for ambient temperatures above +105°C.

*Planar is a patented Fairchild process.

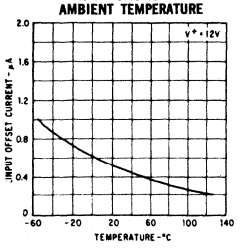
FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, V+ = 12.0 V, and $V_{CM} = 3.5$ V unless otherwise specified)

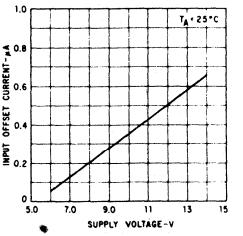
PARAMETER (See Definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 50\Omega$		1.0	2.5	mV
Input Offset Current			0.5	1.5	μA
Input Bias Current			3.5	7.5	μA
Input Resistance		5.0	20		kΩ
Differential Voltage Gain	$R_L \geq 100$ kΩ	100	145	160	
Differential Distortion	$R_L \geq 100$ kΩ		80	300	mVpp
Bandwidth		1.0	1.5		MHz
Single-Ended Output Resistance			70	500	Ω
Output Voltage Swing	$R_L \geq 100$ kΩ	5.0	8.0		Vpp
Supply Current	$R_L \geq 100$ kΩ		9.5	13	mA
Power Consumption	$R_L \geq 100$ kΩ		114	156	mW
The following specifications apply for $-55°C \leq T_A \leq 125°C$:					
Input Offset Voltage	$R_S \leq 50\Omega$			3.5	mV
Input Offset Current	$T_A = +125°C$		0.2	1.5	μA
	$T_A = -55°C$		1.0	3.0	μA
Input Bias Current	$T_A = -55°C$		6.5	15	μA
Input Resistance		0.9			kΩ
Input Voltage Range		3.5		5.2	V
Common Mode Rejection Ratio	$R_S \leq 50\Omega$ f ≤ 1.0 kHz, $+3.5\text{ V} \leq V_{CM} \leq +5.2\text{ V}$	70	85		dB
Differential Voltage Gain	$R_L \geq 100$ kΩ	90		175	
Common Mode Output Voltage		5.5	7.0	7.75	V
Output Resistance				600	Ω
Output Voltage Swing		4.5	6.8		Vpp
Supply Current	$T_A = -55°C$		10	15	mA
	$T_A = 125°C$		8.0	11	mA
Power Consumption	$T_A = -55°C$		120	180	mW
	$T_A = 125°C$		96	121	mW

TYPICAL PERFORMANCE CURVES

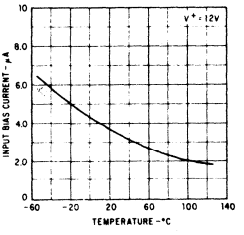
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

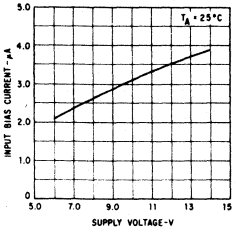


INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

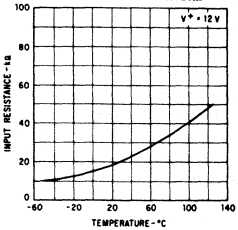


TYPICAL PERFORMANCE CURVES

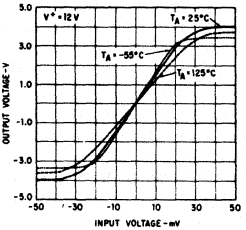
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



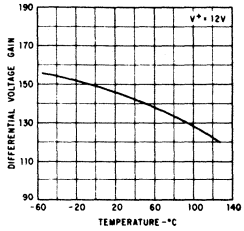
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



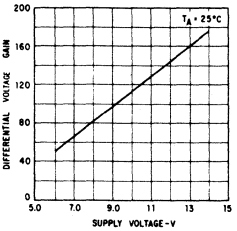
VOLTAGE TRANSFER CHARACTERISTICS



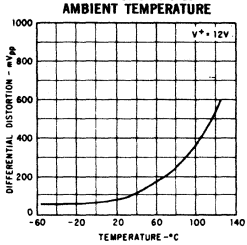
DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



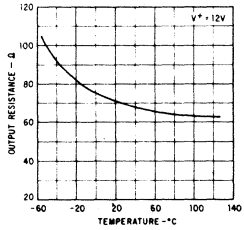
DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



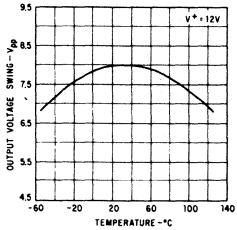
DIFFERENTIAL DISTORTION AS A FUNCTION OF AMBIENT TEMPERATURE



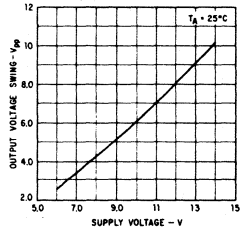
OUTPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



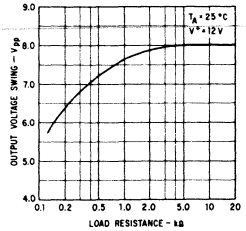
OUTPUT VOLTAGE SWING AS A FUNCTION OF AMBIENT TEMPERATURE



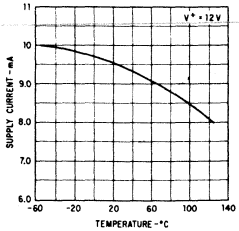
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



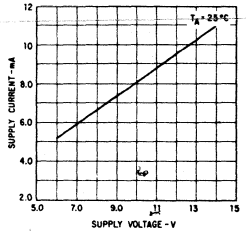
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

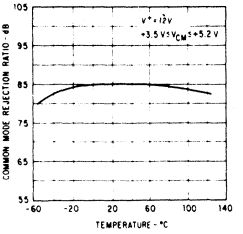


DEFINITION OF TERMS

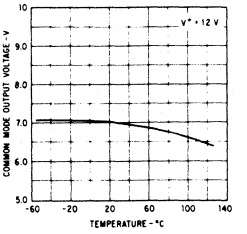
INPUT OFFSET VOLTAGE—That voltage which must be applied between the input terminals to obtain zero differential output voltage.
INPUT OFFSET CURRENT—The difference in the currents into the two input terminals with the output at zero differential volts.
INPUT BIAS CURRENT—The average of the two input currents.
INPUT BIAS RESISTANCE—The resistance looking into either input terminal with the other grounded.
INPUT VOLTAGE RANGE—The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.
COMMON MODE REJECTION RATIO—The ratio of the input voltage range to the maximum change in input offset voltage over this range.
DIFFERENTIAL VOLTAGE GAIN—The ratio of the change in the differential output voltage to the change in voltage between the input terminals producing it.
DIFFERENTIAL DISTORTION—The A.C. unbalance in the output common mode voltage produced by unsymmetrical output voltage swings.
BANDWIDTH—The frequency at which the differential voltage gain is 3 dB below its low frequency value.
OUTPUT RESISTANCE—The resistance seen looking into either output terminal with the output at differential null.
COMMON MODE OUTPUT VOLTAGE—The average voltage at the two output terminals referred to ground.
OUTPUT VOLTAGE SWING—The peak-to-peak output swing that can be obtained without clipping.
SUPPLY CURRENT—The current required from the power supply to operate the device with no load.
POWER CONSUMPTION—The DC power required to operate the amplifier with no load current.

TYPICAL PERFORMANCE CURVES

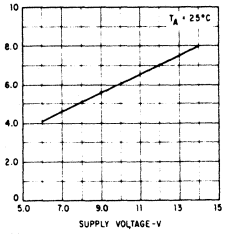
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



COMMON MODE OUTPUT VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



COMMON MODE OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



μA730C
DIFFERENTIAL AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

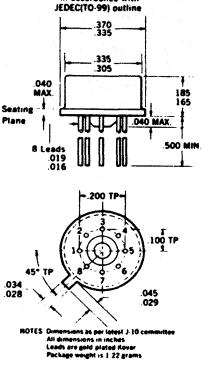
GENERAL DESCRIPTION – The μA730C is a differential amplifier constructed on a single silicon-chip using the Fairchild Planar* epitaxial process. This device has a wide range of applications since it has both a differential input and output; any combination of single-ended or differential configurations can be employed at its input and output. The emitter follower output stage gives this device a low output impedance making it useful as a preamplifier.

For full temperature range operation (−55°C to +125°C), see μA730 data sheet.

ABSOLUTE MAXIMUM RATINGS

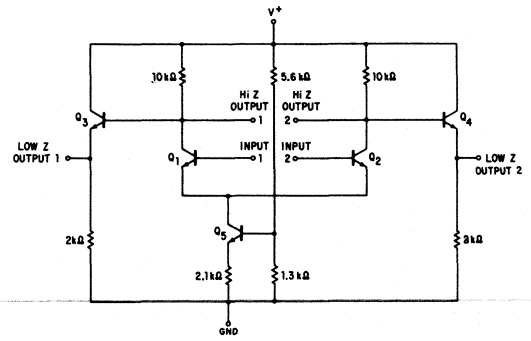
Supply Voltage	15 V
Differential Input Voltage	±5 V
Common Mode Input Voltage	2.5 to 5.5 V
Internal Power Dissipation (Note 1)	300 mW
Operating Temperature Range	0°C to + 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	+300°C

PHYSICAL DIMENSIONS
in accordance with JEDEC(TO-99) outline

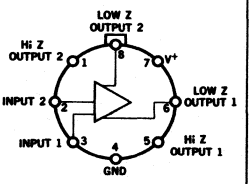


Order Part No. USB7730393

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(Top View)



Note: Pin 4 connected to case

NOTES:
(1) Rating applies for ambient temperatures to + 70°C.

*Planar is a patented Fairchild process.

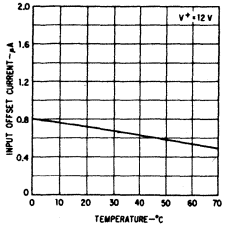
FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, V+ = 12.0 V, and $V_{CM} = 3.5$ V unless otherwise specified)

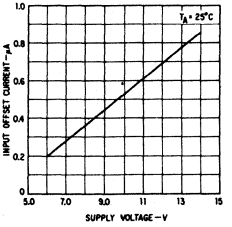
PARAMETER (See Definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 50\Omega$		2.0	5.0	mV
Input Offset Current			0.7	3.0	μA
Input Bias Current			4.5	16.0	μA
Input Resistance		2.5	15		kΩ
Differential Voltage Gain	$R_L \geq 100$ kΩ	100	135	160	
Differential Distortion	$R_L \geq 100$ kΩ		85	300	mVpp
Bandwidth		1.0	1.5		MHz
Single-Ended Output Resistance			70	500	Ω
Output Voltage Swing	$R_L \geq 100$ kΩ	5.0	8.0		Vpp
Supply Current	$R_L \geq 100$ kΩ		9.5	13	mA
Power Consumption	$R_L \geq 100$ kΩ		114	156	mW
The following specifications apply for $0°C \leq T_A \leq +70°C$					
Input Offset Voltage	$R_S \leq 50\Omega$			7.5	mV
Input Offset Current	$T_A = +70°C$		0.5	3.0	μA
	$T_A = 0°C$		0.8	5.0	μA
Input Bias Current	$T_A = 0°C$		5.0	20	μA
Input Resistance		1.8			kΩ
Input Voltage Range		+3.5		+5.2	
Common Mode Rejection Ratio	$R_S \leq 50\Omega$, $f \leq 1.0$ kHz, $+3.5\,V \leq V_{CM} \leq +5.2\,V$	60	80		dB
Differential Voltage Gain	$R_L \geq 100$ kΩ	80		190	
Common Mode Output Voltage		5.0	7.0	8.0	V
Output Resistance				600	Ω
Output Voltage Swing		4.5	7.5		Vpp
Supply Current	$T_A = 0°C$		10	15	mA
	$T_A = +70°C$		8.8	13	mA
Power Consumption	$T_A = 0°C$		120	180	mW
	$T_A = +70°C$		106	156	mW

TYPICAL PERFORMANCE CURVES

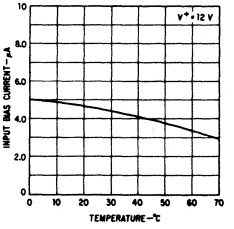
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

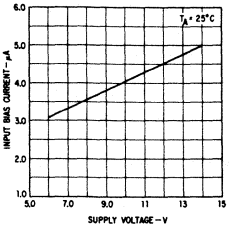


INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

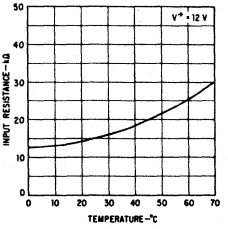


TYPICAL PERFORMANCE CURVES

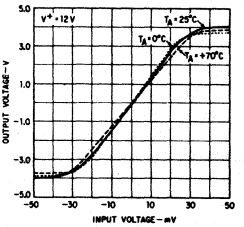
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



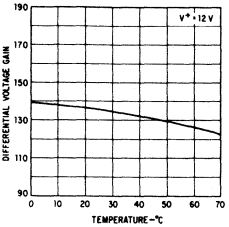
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



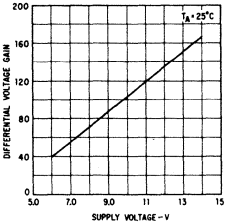
VOLTAGE TRANSFER CHARACTERISTICS



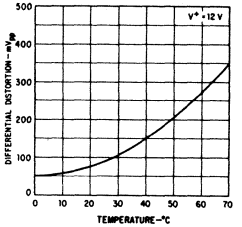
DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



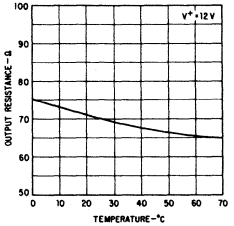
DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



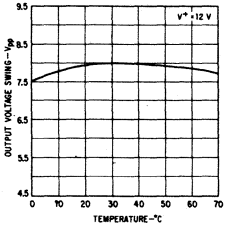
DIFFERENTIAL DISTORTION AS A FUNCTION OF AMBIENT TEMPERATURE



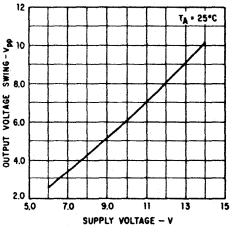
OUTPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



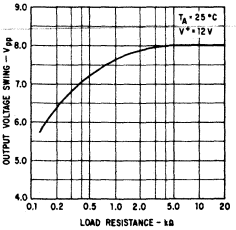
OUTPUT VOLTAGE SWING AS A FUNCTION OF AMBIENT TEMPERATURE



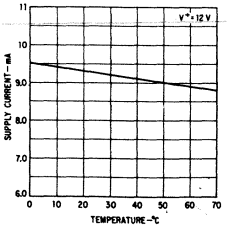
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



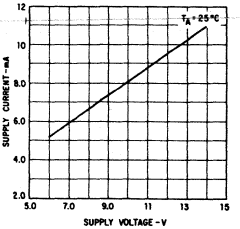
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



DEFINITION OF TERMS

INPUT OFFSET VOLTAGE—That voltage which must be applied between the input terminals to obtain zero differential output voltage.

INPUT OFFSET CURRENT—The difference in the currents into the two input terminals with the output at zero differential volts.

INPUT BIAS CURRENT—The average of the two input currents.

INPUT BIAS RESISTANCE—The resistance looking into either input terminal with the other grounded.

INPUT VOLTAGE RANGE—The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

COMMON MODE REJECTION RATIO—The ratio of the input voltage range to the maximum change in input offset voltage over this range.

DIFFERENTIAL VOLTAGE GAIN—The ratio of the change in the differential output voltage to the change in voltage between the input terminals producing it.

DIFFERENTIAL DISTORTION—The A.C. unbalance in the output common mode voltage produced by unsymmetrical output voltage swings.

BANDWIDTH—The frequency at which the differential voltage gain is 3 dB below its low frequency value.

OUTPUT RESISTANCE—The resistance seen looking into either output terminal with the output at differential null.

COMMON MODE OUTPUT VOLTAGE—The average voltage at the two output terminals referred to ground.

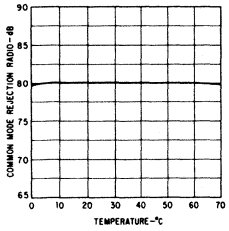
OUTPUT VOLTAGE SWING—The peak-to-peak output swing that can be obtained without clipping.

SUPPLY CURRENT—The current required from the power supply to operate the device with no load.

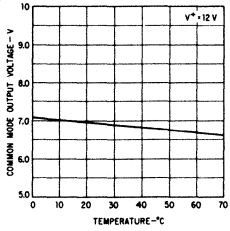
POWER CONSUMPTION—The DC power required to operate the amplifier with no load current.

TYPICAL PERFORMANCE CURVES

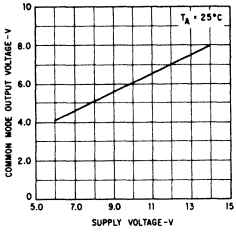
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



COMMON MODE OUTPUT VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



COMMON MODE OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



μA732
FM STEREO MULTIPLEX DECODER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

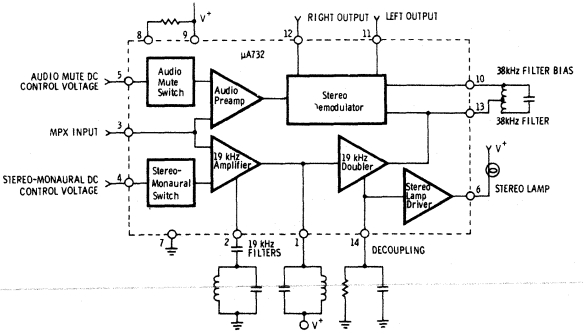
- **45 dB CHANNEL SEPARATION**
- **55 dB STORECAST REJECTION WITHOUT SCA FILTERS**
- **HIGH-CURRENT STEREO INDICATOR LAMP DRIVER**
- **OPERATION WITH 8 V TO 14 V SUPPLIES**
- **INTERNAL STEREO SWITCHING AND AUDIO MUTING FUNCTIONS**

GENERAL DESCRIPTION — The μA732 is a monolithic FM Stereo Multiplex Decoder System constructed on a single silicon chip using the Fairchild Planar* Epitaxial Process. This integrated circuit accomplishes the demodulation of a Stereo Multiplex Signal into the Right and Left audio channels while inherently suppressing SCA frequency components. Internal provision is made for interstation audio muting, stereo/mono mode switching and driving an external stereo mode indicator lamp. The excellent performance, wide supply range and low external parts requirement makes the μA732 suitable for all line-operated and automotive FM Stereo Multiplex applications. For Stereo Decoding with external separation adjustment, see the μA729 Data Sheet. See Note 1.

ABSOLUTE MAXIMUM RATINGS

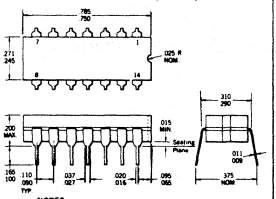
Supply Voltage (Note 2)	+15 V
Voltage at Stereo Lamp Driver Terminal	+22 V
Current into Stereo Lamp Driver Terminal (Note 3)	100 mA
Internal Power Dissipation	400 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 10 Sec.)	+260°C

BLOCK DIAGRAM



PHYSICAL DIMENSIONS

In accordance with JEDEC (TO-116) outline

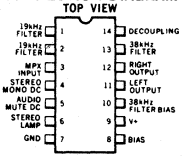


NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams

ORDER PART NO. U6A7732394

CONNECTION DIAGRAM

TOP VIEW



Notes on Page 2.

*Planar is a patented Fairchild process.

FAIRCHILD SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V^+ = +12$ V, 200 mV RMS Standard Stereo Multiplex signal applied to Input, unless otherwise specified (Note 4). Refer to Test Circuit of Figure 1.)

PARAMETER	MIN.	TYP.	MAX.	UNITS
Supply Current		10		mA
Input Resistance		20		kΩ
Stereo Separation				
f = 100 Hz		40		dB
f = 1 kHz		45		dB
f = 10 kHz		40		dB
Channel Balance (Monaural Input)		0.5		dB
Total Harmonic Distortion		0.5		%
Voltage Gain		1.0		V/V
67 kHz Storecast Rejection (Note 5)		55		dB
19 kHz Pilot Level Required at Input for:				
Stereo Indicator Lamp on		12		mV RMS
Stereo Indicator Lamp off		8.0		mV RMS
DC Voltage Required at Pin 4 for Stereo-Monaural Switching				
Stereo on		1.25		V DC
Stereo off		0.85		V DC
DC Voltage Required at Pin 5 for Audio Mute Switching				
Audio on		1.20		V DC
Audio off		0.85		V DC
Mute Attenuation of Audio		55		dB
High Frequency Audio Components in Left and Right Outputs (dB below 1 kHz output)				
19 kHz		30		dB
38 kHz		25		dB

NOTES:

(1) The μA732 is a plug-in replacement for the MC1304. For μA732 applications information, and other Fairchild Communications Integrated circuits see listing on last page.

(2) Power supply transients up to 22V are permissible for periods of 15 seconds. However, extended operation at voltages greater than 15V should be avoided as the maximum allowable internal power dissipation for this device may be exceeded.

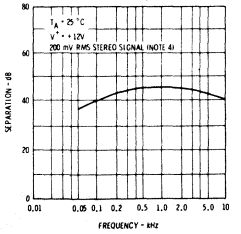
(3) Rating applies to steady state current. Maximum permissible surge current during turn-on of the Stereo Indicator Lamp is 500 mA.

(4) "Standard Stereo Multiplex Signal" here refers to a 200mV RMS (0.56V p-p) composite stereo signal including 10% pilot with L = 1 and R = 1 as described in the FCC Rules on FM Broadcasting.

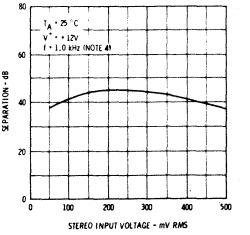
(5) Measured with a stereo composite signal consisting of 80% stereo, 10% pilot and 10% SCA as defined in the FCC Rules on FM Broadcasting.

TYPICAL PERFORMANCE CURVES

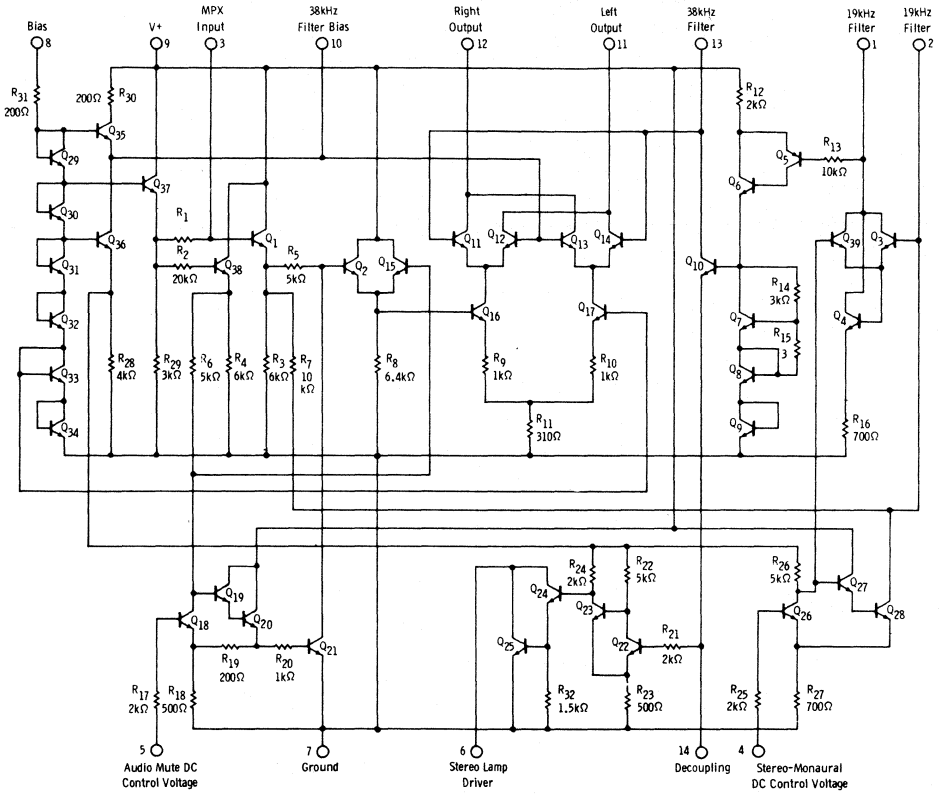
SEPARATION VERSUS AUDIO FREQUENCY



1 kHz SEPARATION VERSUS COMPOSITE INPUT VOLTAGE

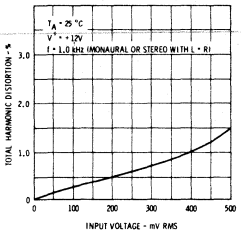


μA732 FM STEREO MULTIPLEX DECODER EQUIVALENT CIRCUIT

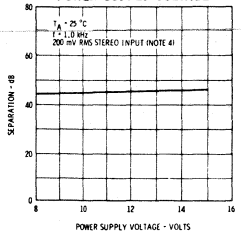


TYPICAL PERFORMANCE CURVES

1 kHz DISTORTION VERSUS INPUT VOLTAGE



1 kHz SEPARATION VERSUS POWER SUPPLY VOLTAGE



μA732 FM STEREO MULTIPLEX DECODER TEST CIRCUIT AND TYPICAL APPLICATION

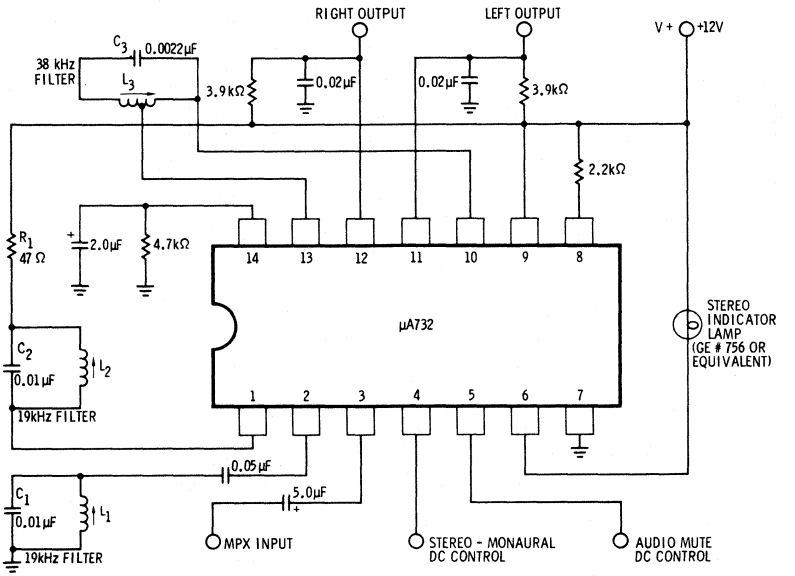


Fig. 1

NOTES:
(1) Capacitors C_1, C_2 and C_3 should be polystyrene or mylar.
(2) Coils L_1 and L_2 are 7.0 mH nominal with Q_{u1} = 60 (Miller #1361 or equivalent).
(3) Coil L_3 is 8 mH nominal with Q_{u1} = 80, tapped at 10:1 turns ratio. (Miller #1362 or equivalent).
(4) Resistor R_1 can be increased (or decreased) in value to increase (or decrease) the 19kHz sensitivity.

μA732 APPLICATIONS INFORMATION:

APP BRIEF 150 — The μA729 and μA732 Integrated Circuit Stereo Multiplex Decoders.
APP BRIEF 151 — A High Quality AM/FM Stereo Receiver.

FOR INFORMATION ON OTHER FAIRCHILD COMMUNICATIONS INTEGRATED CIRCUITS, SEE THE FOLLOWING DATA SHEETS:

RF/IF LIMITING AMP — μA703C
RF/IF LIMITING AMP — μA703D
FIXED GAIN, LOW DISTORTION AMP — μA716C
HIGH FREQUENCY COMMUNICATIONS SYSTEM μA719C
FM STEREO MULTIPLEX DECODER μA729
DUAL LOW NOISE HIGH GAIN OP-AMP μA739C
DUAL AC AMP μA745
COLOR TV CHROMA DEMODULATOR μA746
DUAL OPERATIONAL AMPLIFIER μA749D
TV/FM SOUND SYSTEM μA754C
GAIN CONTROLLED IF AMP μA757C
BALANCED MODULATOR-DEMODULATOR μA796C

μA733
DIFFERENTIAL VIDEO AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

- **120 MHz BANDWIDTH**
- **250 kΩ INPUT RESISTANCE**
- **SELECTABLE GAINS OF 10, 100, AND 400**
- **NO FREQUENCY COMPENSATION REQUIRED**

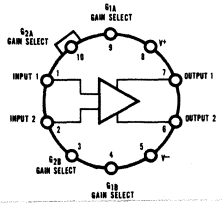
GENERAL DESCRIPTION — The μA733 is a monolithic two-stage differential input, differential output video amplifier constructed on a single silicon chip using the Fairchild Planar* epitaxial process. Internal series-shunt feedback is used to obtain wide bandwidth, low phase distortion, and excellent gain stability. Emitter follower outputs enable the device to drive capacitive loads and all stages are current-source biased to obtain high power supply and common mode rejection ratios. It offers fixed gains of 10, 100, or 400 without external components, and adjustable gains from 10 to 400 by the use of a single external resistor. No external frequency compensation components are required for any gain option. The device is particularly useful in magnetic tape or disc file systems using phase or NRZ encoding and in high-speed thin film or plated wire memories. Other applications include general-purpose video and pulse amplifiers where wide bandwidth, low phase shift, and excellent gain stability are required.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage		±8 V
Differential Input Voltage		±5 V
Common Mode Input Voltage		±6 V
Output Current		10 mA
Internal Power Dissipation (Note 1)	3F (Flat Pak)	280 mW
	5F (Metal Can)	500 mW
	6A (DIP)	720 mW
Operating Temperature Range		−55°C to +125°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 60 second time limit)		300°C

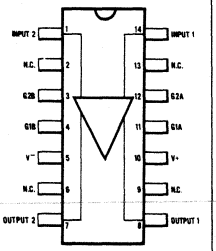
CONNECTION DIAGRAM (Top Views)

TO-100 METAL CAN

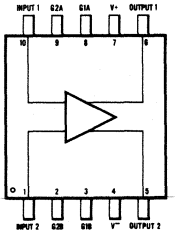


Note: Pin 5 connected to case.

TO-116 DUAL IN-LINE



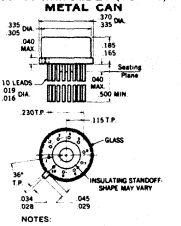
TO-91 FLAT PACKAGE



PHYSICAL DIMENSIONS

In accordance with JEDEC (TO-100) outline

METAL CAN

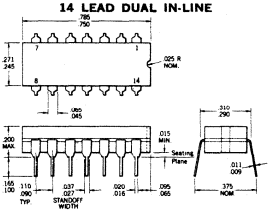


NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.32 grams
Lead 5 is connected to case

ORDER PART NO. U5F773312

In accordance with JEDEC (TO-116) outline

14 LEAD DUAL IN-LINE

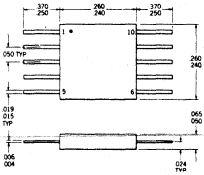


NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for a .020 inch diameter lead
Leads are tin plated kovar
Package weight is 2.0 grams

ORDER PART NO. U6A7733312

In accordance with JEDEC (TO-91) outline

10 LEAD CERPAK



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.26 gram

ORDER PART NO. U3F7733312

Notes on Page 4

*Planar is a patented Fairchild process.

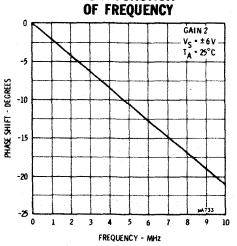
FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V_S = \pm 6.0$ V unless otherwise specified)

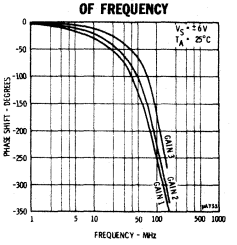
PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Voltage Gain					
Gain 1 (Note 2)		300	400	500	
Gain 2 (Note 3)		90	100	110	
Gain 3 (Note 4)		9.0	10	11	
Bandwidth	$R_S = 50\ \Omega$				
Gain 1			40		MHz
Gain 2			90		MHz
Gain 3			120		MHz
Risetime	$R_S = 50\ \Omega$, $V_{out} = 1$ Vpp				
Gain 1			10.5		ns
Gain 2			4.5	10	ns
Gain 3			2.5		ns
Propagation Delay	$R_S = 50\ \Omega$, $V_{out} = 1$ Vpp				
Gain 1			7.5		ns
Gain 2			6.0	10	ns
Gain 3			3.6		ns
Input Resistance					
Gain 1			4.0		kΩ
Gain 2		20	30		kΩ
Gain 3			250		kΩ
Input Capacitance	Gain 2		2.0		pF
Input Offset Current			0.4	3.0	μA
Input Bias Current			9.0	20	μA
Input Noise Voltage	$R_S = 50\ \Omega$, BW = 1 kHz to 10 MHz		12		μVrms
Input Voltage Range		±1.0			V
Common Mode Rejection Ratio					
Gain 2	$V_{cm} = \pm 1$ V, f ≤ 100 kHz	60	86		dB
Gain 2	$V_{cm} = \pm 1$ V, f = 5 MHz		60		dB
Supply Voltage Rejection Ratio					
Gain 2	$\Delta V_S = \pm 0.5$ V	50	70		dB
Output Offset Voltage					
Gain 1			0.6	1.5	V
Gain 2 and Gain 3			0.35	1.0	V
Output Common Mode Voltage		2.4	2.9	3.4	V
Output Voltage Swing		3.0	4.0		Vpp
Output Sink Current		2.5	3.6		mA
Output Resistance			20		Ω
Power Supply Current			18	24	mA
The following specifications apply for $-55°C \leq T_A \leq +125°C$					
Differential Voltage Gain					
Gain 1 (Note 2)		200		600	
Gain 2 (Note 3)		80		120	
Gain 3 (Note 4)		8.0		12	
Input Resistance—Gain 2		8.0			kΩ
Input Offset Current				5.0	μA
Input Bias Current				40	μA
Input Voltage Range		±1.0			V
Common Mode Rejection Ratio		50			dB
Supply Voltage Rejection Ratio		50			dB
Output Offset Voltage—Gain 1				1.5	V
Output Offset Voltage—Gain 2 & 3				1.2	V
Output Swing		2.5			Vpp
Output Sink Current		2.2			mA
Positive Supply Current				27	mA

TYPICAL PERFORMANCE CURVES

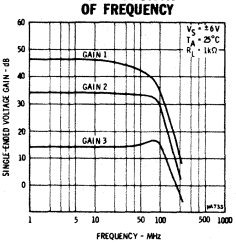
PHASE SHIFT AS A FUNCTION OF FREQUENCY



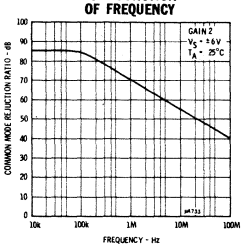
PHASE SHIFT AS A FUNCTION OF FREQUENCY



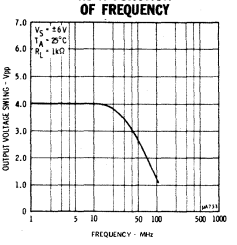
VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



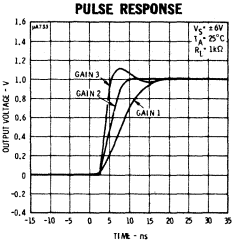
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



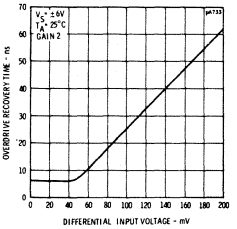
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



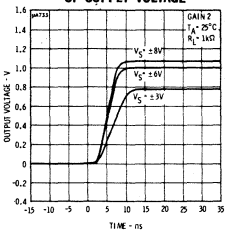
PULSE RESPONSE



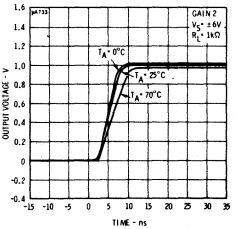
DIFFERENTIAL OVERDRIVE RECOVERY TIME



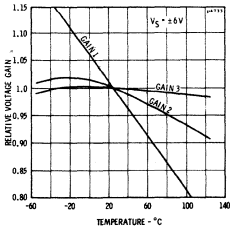
PULSE RESPONSE AS A FUNCTION OF SUPPLY VOLTAGE



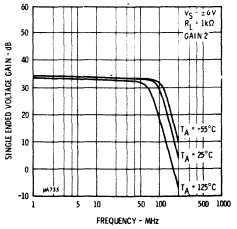
PULSE RESPONSE AS A FUNCTION OF TEMPERATURE



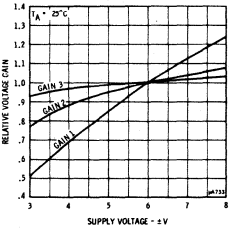
VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



GAIN VERSUS FREQUENCY AS A FUNCTION OF TEMPERATURE

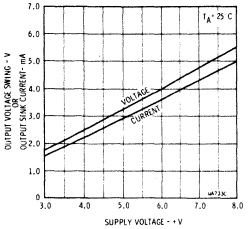


VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE

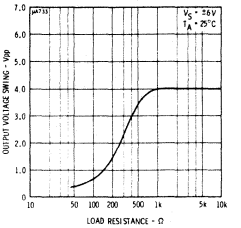


TYPICAL PERFORMANCE CURVES

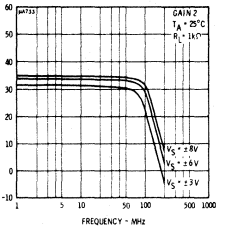
OUTPUT VOLTAGE AND CURRENT SWING AS A FUNCTION OF SUPPLY VOLTAGE



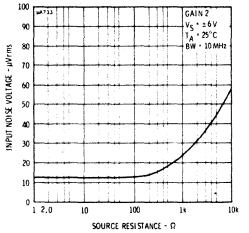
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



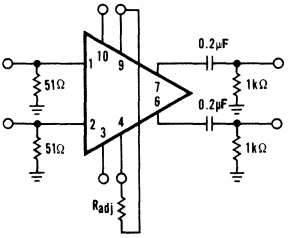
GAIN VERSUS FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



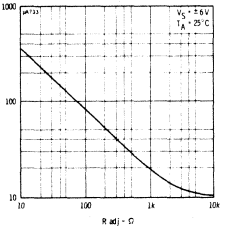
INPUT NOISE VOLTAGE AS A FUNCTION OF SOURCE RESISTANCE



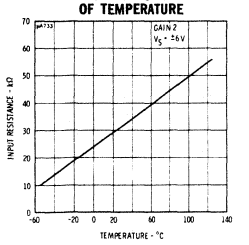
VOLTAGE GAIN ADJUST CIRCUIT



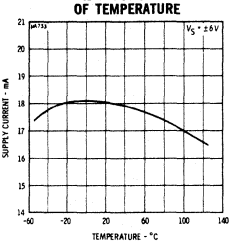
VOLTAGE GAIN AS A FUNCTION OF R_{ADJ}



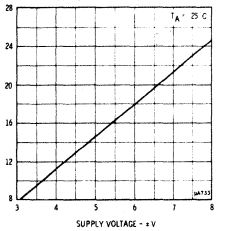
INPUT RESISTANCE AS A FUNCTION OF TEMPERATURE



SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



NOTES:

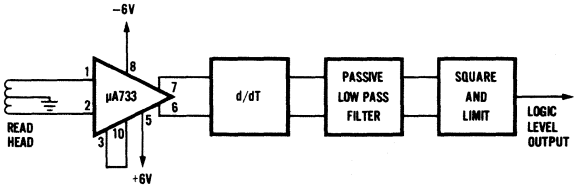
(1) Rating applies for case temperature to 125°C; derate linearly at 4.4 mW/°C for ambient temperature above 95°C (Flat Pak); derate linearly at 6.5 mW/°C for ambient temperature above 75°C (Metal Can); derate linearly at 8.0 mW/°C for ambient temperature above 70°C (DIP).
(2) Gain Select pins G_{1A} and G_{1B} connected together.
(3) Gain Select pins G_{2A} and G_{2B} connected together.
(4) All Gain Select pins open.

DEFINITION OF TERMS

DIFFERENTIAL VOLTAGE GAIN — The ratio of the change in the differential output voltage to the change in voltage between the input terminals producing it.
BANDWIDTH — The frequency at which the differential gain is 3 dB below its low frequency value.
RISE TIME — The time required for an output voltage step to change from 10% to 90% of its final value.
PROPAGATION DELAY — The interval between the application of an input voltage step and its arrival at either output, measured at 50% of the final value.
INPUT RESISTANCE — The resistance seen looking into either input terminal with the other grounded.
INPUT OFFSET CURRENT — The difference between the currents into the two input terminals.
INPUT BIAS CURRENT — The average of the two input currents.
INPUT VOLTAGE RANGE — The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.
COMMON MODE REJECTION RATIO — The ratio of a change in input common mode voltage to the resulting change in output offset voltage referred to the input.
SUPPLY VOLTAGE REJECTION RATIO — The ratio of a change in supply voltage to the resulting change in output offset voltage referred to the input.
OUTPUT OFFSET VOLTAGE — The difference between the voltages at the two output terminals with the inputs grounded.
OUTPUT COMMON MODE VOLTAGE — The average of the voltages at the two output terminals.
OUTPUT VOLTAGE SWING — The peak-to-peak output swing that can be obtained without clipping. This includes the unbalance caused by output offset voltage.
OUTPUT SINK CURRENT — The peak negative current available at either output of the amplifier.
OUTPUT RESISTANCE — The resistance seen looking into either output terminal.
POWER SUPPLY CURRENT — The current required from the power supplies to operate the device with no load.

TYPICAL APPLICATIONS

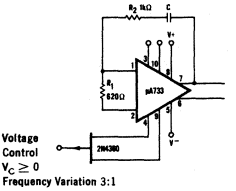
PHASE ENCODING PLAYBACK SYSTEM



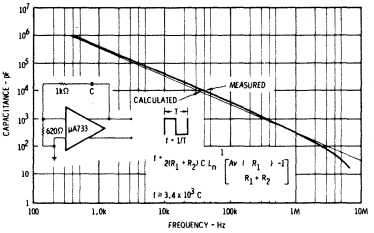
Phase Linearity:	$\pm 2^{\circ}$ from 2 to 5 MHz
Input Resistance:	25 kΩ
Input Capacity:	2 pF
Fixed Gain:	100

TYPICAL APPLICATIONS

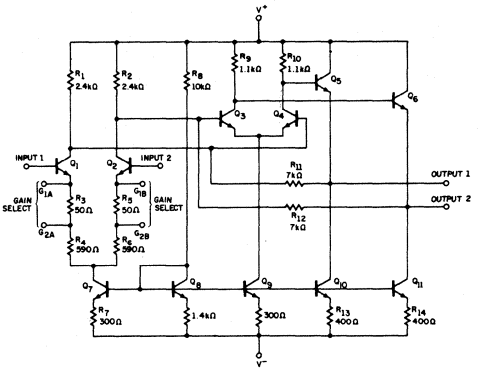
VOLTAGE CONTROLLED OSCILLATOR



OSCILLATOR FREQUENCY FOR VARIOUS CAPACITOR VALUES



EQUIVALENT CIRCUIT



μA733C
DIFFERENTIAL VIDEO AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

- **120 MHz BANDWIDTH**
- **250 kΩ INPUT RESISTANCE**
- **SELECTABLE GAINS OF 10, 100, AND 400**
- **NO FREQUENCY COMPENSATION REQUIRED**

GENERAL DESCRIPTION — The μA733C is a monolithic two-stage differential input, differential output video amplifier constructed on a single silicon chip using the Fairchild Planar* epitaxial process. Internal series-shunt feedback is used to obtain wide bandwidth, low phase distortion, and excellent gain stability. Emitter follower outputs enable the device to drive capacitive loads and all stages are current-source biased to obtain high power supply and common mode rejection ratios. It offers fixed gains of 10, 100, or 400 without external components, and adjustable gains from 10 to 400 by the use of a single external resistor. No external frequency compensation components are required for any gain option. The device is particularly useful in magnetic tape or disc file systems using phase or NRZ encoding and in high-speed thin film or plated wire memories. Other applications include general-purpose video and pulse amplifiers where wide bandwidth, low phase shift, and excellent gain stability are required.

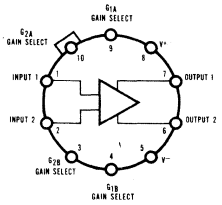
For full temperature range performance (−55°C to 125°C), see μA733 data sheet.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage		±8 V
Differential Input Voltage		±5 V
Common Mode Input Voltage		±6 V
Output Current		10 mA
Internal Power Dissipation (Note 1)	3F (Flat Pak)	280 mW
	5F (Metal Can)	500 mW
	6A (DIP)	720 mW
Operating Temperature Range 5F (Metal Can) and 6A (DIP)		0°C to +70°C
Operating Temperature Range 3F (Flat Pak)		−55°C to +125°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 60 second time limit)		300°C

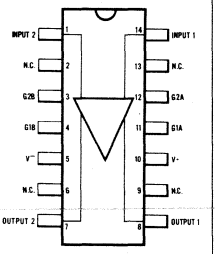
CONNECTION DIAGRAM (Top Views)

TO-100 METAL CAN

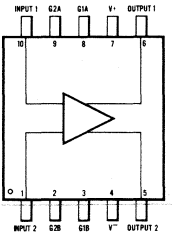


Note: Pin 5 connected to case.

TO-116 DUAL IN-LINE

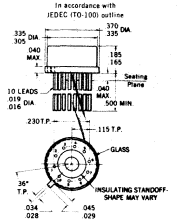


TO-91 FLAT PACKAGE



PHYSICAL DIMENSIONS

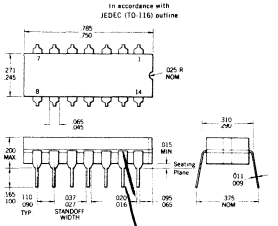
In accordance with JEDEC (TO-100) outline



NOTES:
All dimensions in inches
Leads are gold plated kovar
Package weight is 1.32 grams
Lead 5 is connected to case

ORDER PART NO. U5F773393

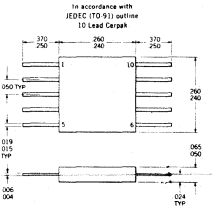
In accordance with JEDEC (TO-116) outline



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for a .020 inch diameter lead
Leads are tin plated kovar
Package weight is 2.0 grams

ORDER PART NO. U6A7733393

In accordance with JEDEC (TO-91) outline
10 Lead Cerpak



NOTES:
All dimensions in inches
Leads are gold plated kovar
Package weight is 0.26 gram

ORDER PART NO. U3F7733313

Notes on Page 4

*Planar is a patented Fairchild process.

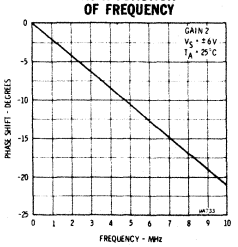
FAIRCHILD SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V_S = \pm 6.0$ V unless otherwise specified)

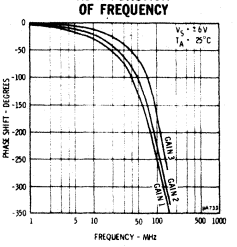
PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Voltage Gain					
Gain 1 (Note 2)		250	400	600	
Gain 2 (Note 3)		80	100	120	
Gain 3 (Note 4)		8.0	10	12	
Bandwidth	$R_S = 50\ \Omega$				
Gain 1			40		MHz
Gain 2			90		MHz
Gain 3			120		MHz
Risetime	$R_S = 50\ \Omega$, $V_{out} = 1$ Vpp				
Gain 1			10.5		ns
Gain 2			4.5	12	ns
Gain 3			2.5		ns
Propagation Delay	$R_S = 50\ \Omega$, $V_{out} = 1$ Vpp				
Gain 1			7.5		ns
Gain 2			6.0	10	ns
Gain 3			3.6		ns
Input Resistance					
Gain 1			4.0		kΩ
Gain 2		10	30		kΩ
Gain 3			250		kΩ
Input Capacitance	Gain 2		2.0		pF
Input Offset Current			0.4	5.0	μA
Input Bias Current			9.0	30	μA
Input Noise Voltage	$R_S = 50\ \Omega$, BW = 1 kHz to 10 MHz		12		μVrms
Input Voltage Range		±1.0			V
Common Mode Rejection Ratio					
Gain 2	$V_{cm} = \pm 1$ V, f ≤ 100 kHz	60	86		dB
Gain 2	$V_{cm} = \pm 1$ V, f = 5 MHz		60		dB
Supply Voltage Rejection Ratio					
Gain 2	$\Delta V_S = \pm 0.5$ V	50	70		dB
Output Offset Voltage					
Gain 1			0.6	1.5	V
Gain 2 and Gain 3			0.35	1.5	V
Output Common Mode Voltage		2.4	2.9	3.4	V
Output Voltage Swing		3.0	4.0		Vpp
Output Sink Current		2.5	3.6		mA
Output Resistance			20		Ω
Power Supply Current			18	24	mA
The following specifications apply for $0°C \leq T_A \leq +70°C$					
Differential Voltage Gain					
Gain 1 (Note 2)		250		600	
Gain 2 (Note 3)		80		120	
Gain 3 (Note 4)		8.0		12	
Input Resistance—Gain 2		8.0			kΩ
Input Offset Current				6.0	μA
Input Bias Current				40	μA
Input Voltage Range		±1.0			V
Common Mode Rejection Ratio					
Gain 2	$V_{cm} = \pm 1$ V, f ≤ 100 kHz	50			dB
Supply Voltage Rejection Ratio					
Gain 2	$\Delta V_S = \pm 0.5$ V	50			dB
Output Offset Voltage (All Gain)				1.5	V
Output Voltage Swing		2.8			Vpp
Output Sink Current		2.5			mA
Power Supply Current				27	mA

TYPICAL PERFORMANCE CURVES

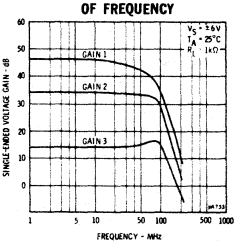
PHASE SHIFT AS A FUNCTION OF FREQUENCY



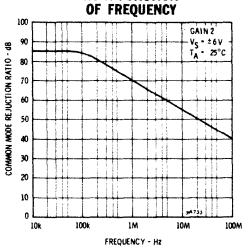
PHASE SHIFT AS A FUNCTION OF FREQUENCY



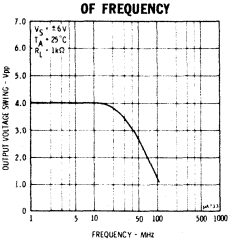
VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



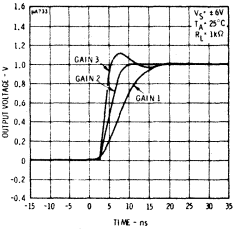
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



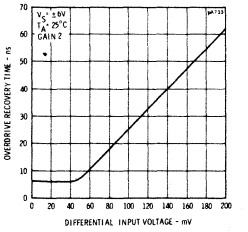
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



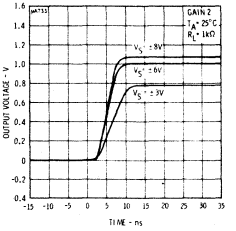
PULSE RESPONSE



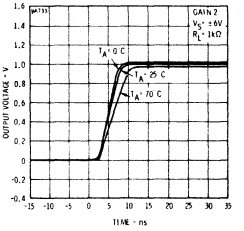
DIFFERENTIAL OVERDRIVE RECOVERY TIME



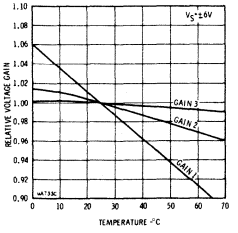
PULSE RESPONSE AS A FUNCTION OF SUPPLY VOLTAGE



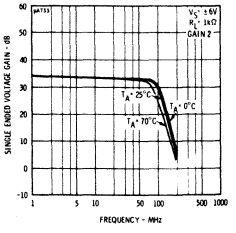
PULSE RESPONSE AS A FUNCTION OF TEMPERATURE



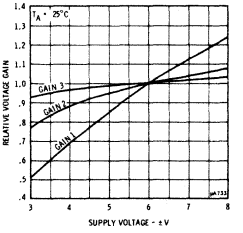
VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



GAIN VERSUS FREQUENCY AS A FUNCTION OF TEMPERATURE

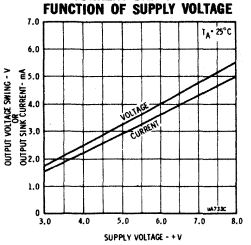


VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE

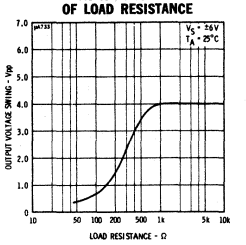


TYPICAL PERFORMANCE CURVES

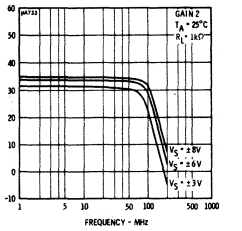
OUTPUT VOLTAGE AND CURRENT SWING AS A FUNCTION OF SUPPLY VOLTAGE



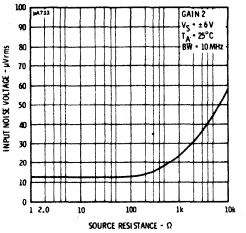
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



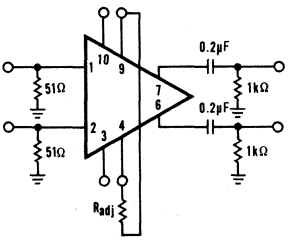
GAIN VERSUS FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



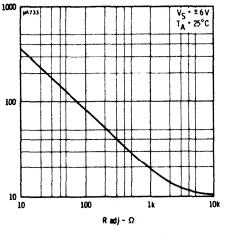
INPUT NOISE VOLTAGE AS A FUNCTION OF SOURCE RESISTANCE



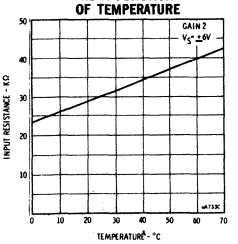
VOLTAGE GAIN ADJUST CIRCUIT



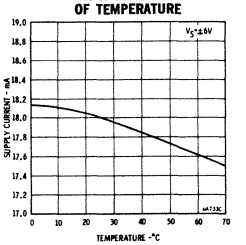
VOLTAGE GAIN AS A FUNCTION OF R_{ADJ}



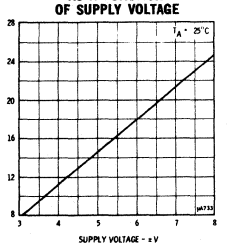
INPUT RESISTANCE AS A FUNCTION OF TEMPERATURE



SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



NOTES:

(1) Rating applies for ambient temperature to 70°C for metal can and DIP, case temperature to 125°C for Flat Pak; derate linearly at 4.4 mW/°C for ambient temperature above 95°C.

(2) Gain Select pins G_{1A} and G_{1B} connected together.

(3) Gain Select pins G_{2A} and G_{2B} connected together.

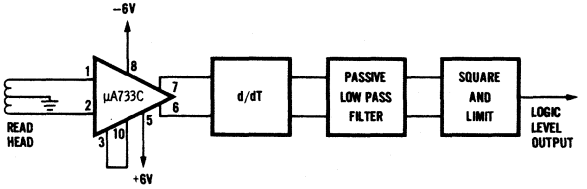
(4) All Gain Select pins open.

DEFINITION OF TERMS

DIFFERENTIAL VOLTAGE GAIN — The ratio of the change in the differential output voltage to the change in voltage between the input terminals producing it.
BANDWIDTH — The frequency at which the differential gain is 3 dB below its low frequency value.
RISE TIME — The time required for an output voltage step to change from 10% to 90% of its final value.
PROPAGATION DELAY — The interval between the application of an input voltage step and its arrival at either output, measured at 50% of the final value.
INPUT RESISTANCE — The resistance seen looking into either input terminal with the other grounded.
INPUT OFFSET CURRENT — The difference between the currents into the two input terminals.
INPUT BIAS CURRENT — The average of the two input currents.
INPUT VOLTAGE RANGE — The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.
COMMON MODE REJECTION RATIO — The ratio of a change in input common mode voltage to the resulting change in output offset voltage referred to the input.
SUPPLY VOLTAGE REJECTION RATIO — The ratio of a change in supply voltage to the resulting change in output offset voltage referred to the input.
OUTPUT OFFSET VOLTAGE — The difference between the voltages at the two output terminals with the inputs grounded.
OUTPUT COMMON MODE VOLTAGE — The average of the voltages at the two output terminals.
OUTPUT VOLTAGE SWING — The peak-to-peak output swing that can be obtained without clipping. This includes the unbalance caused by output offset voltage.
OUTPUT SINK CURRENT — The peak negative current available at either output of the amplifier.
OUTPUT RESISTANCE — The resistance seen looking into either output terminal.
POWER SUPPLY CURRENT — The current required from the power supplies to operate the device with no load.

TYPICAL APPLICATIONS

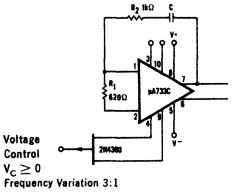
PHASE ENCODING PLAYBACK SYSTEM



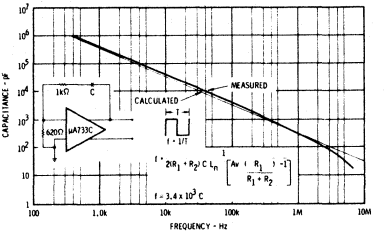
Phase Linearity:	±2° from 2 to 5 MHz
Input Resistance:	25 kΩ
Input Capacity:	2 pF
Fixed Gain:	100

TYPICAL APPLICATIONS

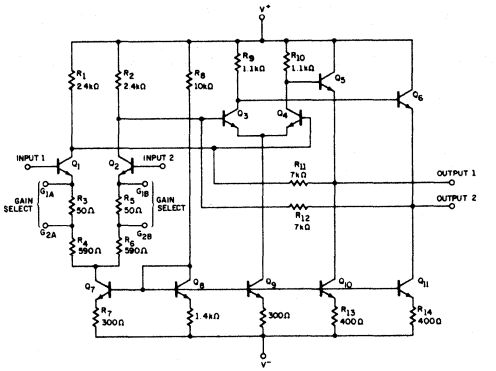
VOLTAGE CONTROLLED OSCILLATOR



OSCILLATOR FREQUENCY FOR VARIOUS CAPACITOR VALUES



EQUIVALENT CIRCUIT



μA734
PRECISION VOLTAGE COMPARATOR
FAIRCHILD LINEAR INTEGRATED CIRCUITS

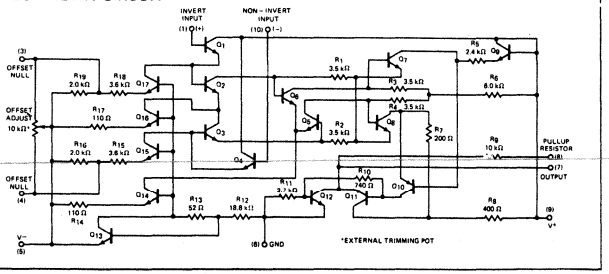
- **CONSTANT INPUT IMPEDANCE OVER DIFFERENTIAL INPUT RANGE**
- **HIGH INPUT IMPEDANCE**
- **LOW DRIFT**
- **HIGH GAIN**
- **BALANCED OFFSET NULL CAPABILITY**
- **WIDE SUPPLY VOLTAGE RANGE**
- **TTL COMPATIBLE**

GENERAL DESCRIPTION – The μA734 is a precision voltage comparator constructed on a single silicon chip using the Fairchild Planar* epitaxial process. It is specifically designed for high accuracy level sensing and measuring applications. The μA734 is extremely useful for analog-to-digital converters with twelve bit accuracies and one mega-bit conversion rates. Maximum resolution is obtained by high gain, low input offset current, and low input offset voltage. Its superior temperature stability can be improved by offset nulling which further reduces offset voltage drift. Balanced or unbalanced supply operation and standard TTL logic compatibility enhance the μA734's versatility. (For other Fairchild comparators and power control circuits, see last page.)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18 V
Peak Output Current	10 mA
Differential Input Voltage	±10 V
Input Voltage Range	$\pm V_S$ -2.0 V
Voltage Between Offset Null and V^-	±0.5 V
Internal Power Dissipation (Note 1)	500 mW
Operating Temperature Range	
Military (312 Grade)	-55°C to +125°C
Commercial (393 Grade)	0°C to +70°C
Storage Temperature Range	
Metal Can, Ceramic Dip	-65°C to +150°C
Silicone Dip and Mini Dip	-55°C to +125°C
Lead Temperature	
Metal Can, Ceramic Dip (Soldering, 60 Seconds Max.)	300°C
Silicone Dip and Mini Dip (Soldering, 10 Seconds Max.)	260°C

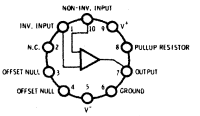
EQUIVALENT CIRCUIT



Notes on Page 3.

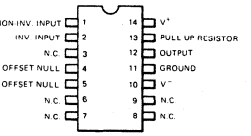
CONNECTION DIAGRAMS

10 LEAD METAL CAN
(TOP VIEW)



ORDER PART NOS: U5F7734312
U5F7734393

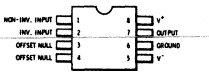
14 LEAD DIP
(TOP VIEW)



FOR CERAMIC DIP
ORDER PART NOS: U6A7734312
U6A7734393

FOR SILICONE DIP
ORDER PART NO: U9A7734393

MINI DIP
(TOP VIEW)



ORDER PART NO: U9T7734393

*Planar is a patented Fairchild process.

FAIRCHILD SEMICONDUCTOR

±15 VOLT OPERATION FOR 312 GRADE

ELECTRICAL CHARACTERISTICS [T_A = 25°C, Pin 8 (Note 2) tied to +15 V, unless otherwise specified]

PARAMETERS (see definitions)	CONDITIONS	MIN	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 50\ k\Omega$		0.9	3.0	mV
Input Offset Current			1.5	10	nA
Input Bias Current			28	50	nA
Input Resistance		20	60		MΩ
Input Capacitance			3.0		pF
Offset Voltage Adjustment Range			8.5		mV
Large Signal Voltage Gains	R_L = 1.5 kΩ to +5.0V	35k	70k		V/V
Positive Supply Current – Output Low			4.0	5.0	mA
Negative Supply Current – Output Low			1.5	2.0	mA
Power Consumption – Output Low			82	105	mW
Transient Response	R_L = 1.5 kΩ to +5.0V		0.2		μs
	5mV overdrive, 100mV pulse				
The following specifications apply for $-55^\circ C \leq T_A \leq +125^\circ C$					
Input Offset Voltage	$R_S \leq 50\ k\Omega$		1.1	4.0	mV
Input Offset Current			3.0	20	nA
Average Input Offset Voltage Drift	$R_S \leq 50\ k\Omega$				
Without External Trim			2.5	15	μV/°C
Average Input Offset Current Drift					
	+25°C to +125°C		0.01	0.1	nA/°C
	+25°C to -55°C		0.05	0.4	nA/°C
Input Bias Current				150	nA
Large Signal Voltage Gain	R_L = 1.5 kΩ to +5.0V	25k			V/V
Input Common Mode Voltage Range		±10			V
Differential Input Voltage Range		±10			V
Common Mode Rejection Ratio	$R_S \leq 50\ k\Omega$	70	100		dB
Supply Voltage Rejection Ratio	$R_S \leq 50\ k\Omega$		5.0	100	μV/V
(V_S = ±5V to ±18V)					
Positive Output Voltage Level	I_O = .080 mA	7.0			V
	I_O = .080 mA, V_8 = +5V	2.4		5.0	V
Negative Output Voltage Level	I_{SINK} = 3.2 mA			0.4	V
Positive Supply Current – Output Low				7.0	mA
Negative Supply Current – Output Low				2.5	mA
Power Dissipation – Output Low				145	mW

±15 VOLT OPERATION FOR 393 GRADE

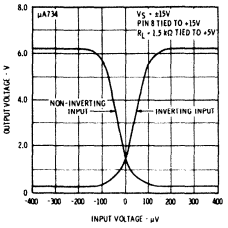
ELECTRICAL CHARACTERISTICS [T_A = 25°C, Pin 8 (Note 2) tied to +15 V, unless otherwise specified]

PARAMETERS (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 50\ k\Omega$		1.1	5.0	mV
Input Offset Current			3.5	25	nA
Input Bias Current			30	100	nA
Input Resistance		7.0	55		MΩ
Input Capacitance			3.0		pF
Offset Voltage Adjustment Range			8.5		mV
Large Signal Voltage Gains	R_L = 1.5 kΩ to +5.0V	35k	60k		V/V
Positive Supply Current – Output Low			4.0	5.0	mA
Negative Supply Current – Output Low			1.5	2.0	mA
Power Consumption – Output Low			82	105	mW
Transient Response	R_L = 1.5 kΩ to +5.0V		0.2		μs
	5 mV overdrive, 100 mV Pulse				
The following specifications apply for $0°C \leq T_A \leq +70°C$					
Input Offset Voltage	$R_S \leq 50\ k\Omega$		1.2	7.5	mV
Input Offset Current			4.0	45	nA
Average Input Offset Voltage Drift	$R_S \leq 50\Omega$				
Without External Trim			3.5	20	μV/°C
Average Input Offset Current Drift					
	+25°C to +70°C		0.02	0.3	nA/°C
	+25°C to 0°C		0.05	0.75	nA/°C
Input Bias Current				150	nA
Large Signal Voltage Gain	R_L = 1.5 kΩ to +5.0V	25k			V/V
Input Common Mode Voltage Range		±10			V
Differential Input Voltage Range		±10			V
Common Mode Rejection Ratio	$R_S \leq 50\ k\Omega$	70	100		dB
Supply Voltage Rejection Ratio	$R_S \leq 50\ k\Omega$		6.0	100	μV/V
(V_S = ±15V to ±18V)					
Positive Output Voltage Level	I_O = .080 mA	7.0			V
	I_O = .080 mA, V_8 = +5V	2.4		5.0	V
Negative Output Voltage Level	I_{SINK} = 3.2 mA			0.4	V
Positive Supply Current – Output Low				7.0	mA
Negative Supply Current – Output Low				2.5	mA
Power Dissipation – Output Low				145	mW

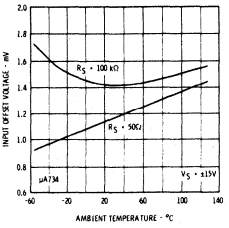
NOTES:
(1) Military ratings (312 grade) apply for case temperatures to 125°C; Derate linearly at 6.5 mW/°C for ambient temperatures above +75°C. Commercial ratings (393 grade) apply for case temperatures to +70°C.
(2) Pin numbers refer to metal can package.

TYPICAL PERFORMANCE CURVES (NOTE 2)

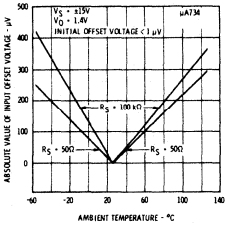
TRANSFER CHARACTERISTICS



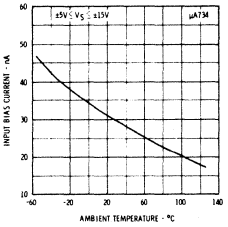
UN-NULLED INPUT OFFSET VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



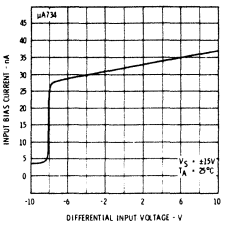
INPUT OFFSET VOLTAGE CHANGE AS A FUNCTION OF AMBIENT TEMPERATURE - NULLED TO ZERO AT 25°C



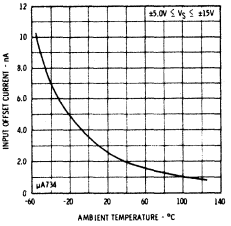
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



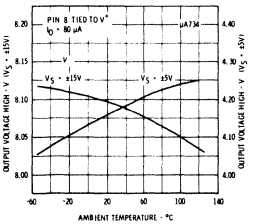
INPUT BIAS CURRENT AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE



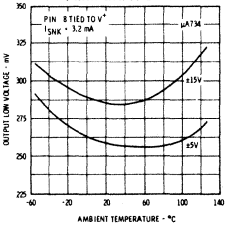
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



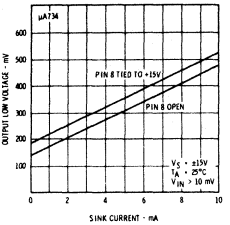
OUTPUT HIGH VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE AND AMBIENT TEMPERATURE



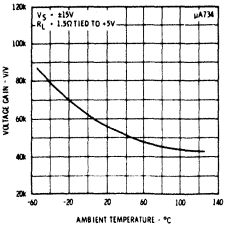
OUTPUT LOW VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE AND AMBIENT TEMPERATURE



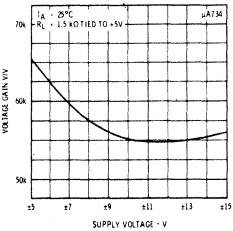
OUTPUT VOLTAGE LOW VS SINK CURRENT



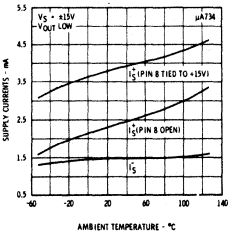
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE

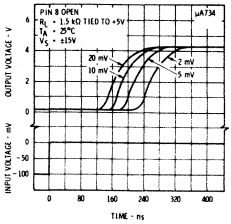


POSITIVE AND NEGATIVE SUPPLY CURRENTS AS A FUNCTION OF AMBIENT TEMPERATURE

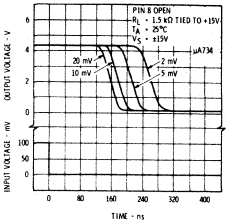


TYPICAL PERFORMANCE CURVES (CONT'D)

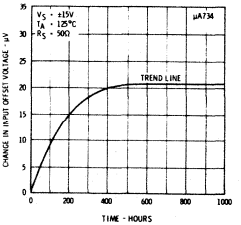
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



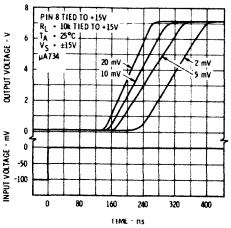
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



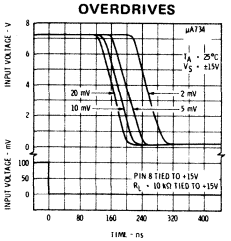
INPUT OFFSET VOLTAGE DRIFT AS A FUNCTION OF TIME



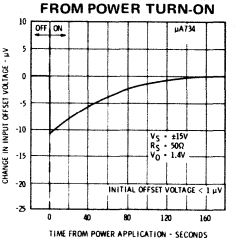
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



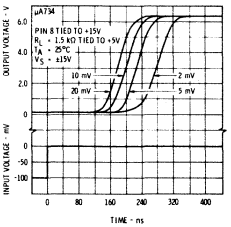
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



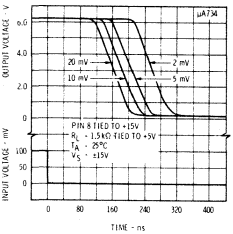
STABILIZATION TIME OF INPUT OFFSET VOLTAGE FROM POWER TURN-ON



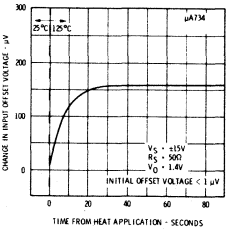
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



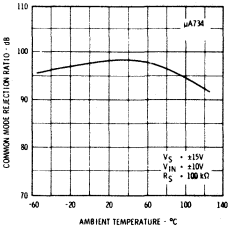
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



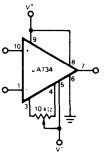
THERMAL RESPONSE OF INPUT OFFSET VOLTAGE TO STEP CHANGE OF CASE TEMPERATURE



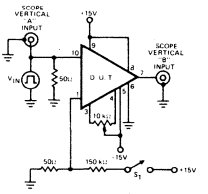
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



OFFSET NULL CIRCUIT TO-100 PIN NUMBERS



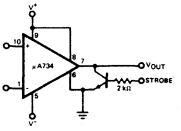
A. C. TEST CIRCUIT



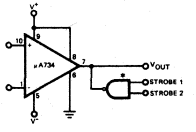
V_{IN} = -100 mV, 100 kHz

TYPICAL APPLICATIONS

STROBE CIRCUITRY

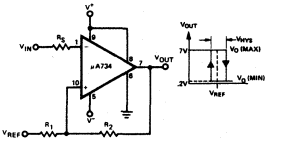


ALTERNATE STROBE CIRCUITRY



* 1/2 9944

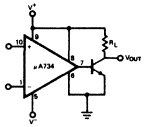
LEVEL DETECTOR WITH HYSTERESIS



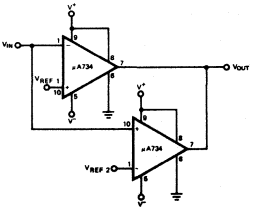
$$R_S = \frac{R_1 R_2}{R_1 + R_2} \text{ FOR MINIMUM OFFSET}$$

$$V_{HYS} = \frac{R_1 [V_{O\,MAX} - V_{O\,MIN}]}{R_1 + R_2}$$

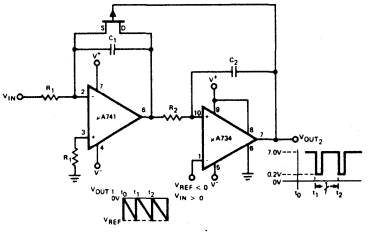
HIGH POWER OUTPUT CIRCUITS



PRECISION DUAL LIMIT GO-NO GO TESTER

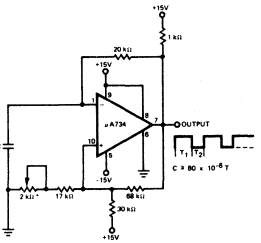


VOLTAGE CONTROLLED OSCILLATOR



$$f = \frac{V_{IN}}{|V_{REF}| R_1 C_1} \qquad R_2 C_2 > \frac{|V_{REF}| C_1}{I_{DSS}}$$

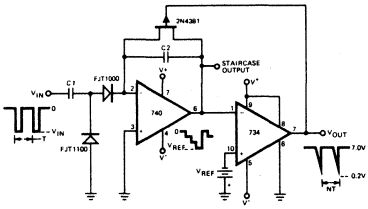
FREE RUNNING OSCILLATOR



$C \approx 80 \times 10^{-6} T$

* Adjusts $\frac{T_1}{T_2}$

FREQUENCY DIVIDER & STAIRCASE GENERATOR

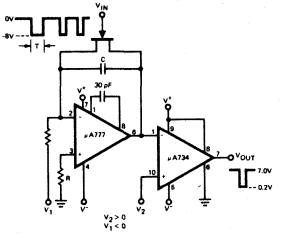


$$|V_{REF}| = 2V_D + N\left[3.5T + 2V_D - \frac{C_1 V_{IN}}{C_2}\right]$$

T In Seconds

V_D for FJT 1000 ≈ 0.31V

PULSE WIDTH DISCRIMINATOR



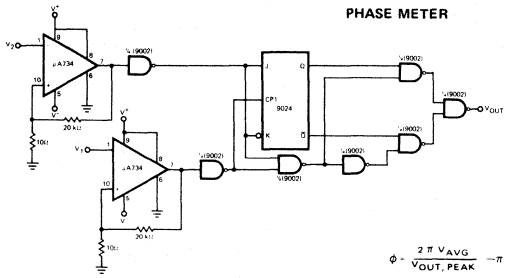
$V_2 > 0$
$V_1 < 0$

V_{OUT} Pulse Appears

Whenever $T > \frac{R C V_2}{|V_1|}$

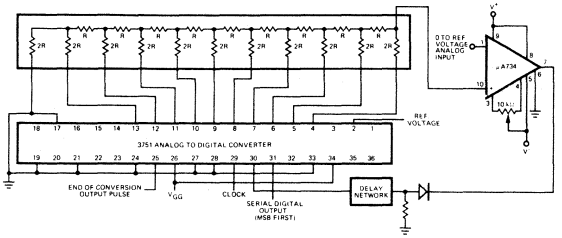
TYPICAL APPLICATIONS (CONT'D)

PHASE METER



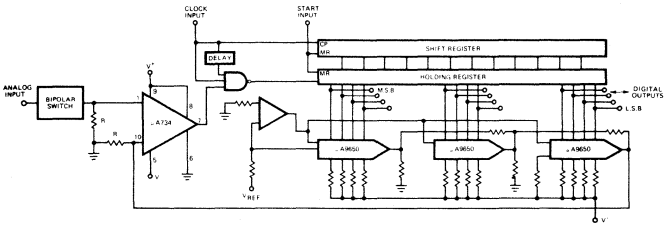
$$\phi = \frac{2\pi V_{AVG}}{V_{OUT,\,PEAK}} - \pi$$

12 BIT A/D CONVERTER



NO. OF BITS	R VALUE
8	12.5kΩ
9	25kΩ
10	50kΩ
12	200kΩ

12 BIT A/D CONVERTER



DEFINITION OF TERMS

LOGIC THRESHOLD VOLTAGE – The approximate voltage at the output of the comparator at which the loading logic circuitry changes its digital state.

INPUT OFFSET VOLTAGE – The voltage between the input terminals when the output is at the logic threshold voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT – The difference in the currents into the two input terminals with the output at the logic threshold voltage.

INPUT BIAS CURRENT – The average of the two input currents.

INPUT COMMON MODE VOLTAGE RANGE – The range of voltage on the input terminals for which the comparator will operate within specifications.

COMMON MODE REJECTION RATIO – The ratio of the input voltage range to the maximum change in input offset voltage over this range.

DIFFERENTIAL INPUT VOLTAGE RANGE – The range of voltage between the input terminals for which operation within specifications is assured.

VOLTAGE GAIN – The ratio of the change in output voltage to the change in voltage between the input terminals producing it with the DC output level in the vicinity of the logic threshold voltage.

RESPONSE TIME – The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

POSITIVE OUTPUT VOLTAGE LEVEL – The DC output voltage in the positive direction with the input voltage equal to or greater than a minimum specified amount.

NEGATIVE OUTPUT VOLTAGE LEVEL – The DC output voltage in the negative direction with the input voltage equal to or greater than a minimum specified amount.

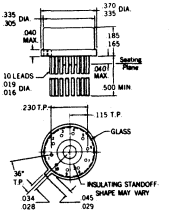
OUTPUT SINK CURRENT – The maximum negative current that can be delivered by the comparator.

PEAK OUTPUT CURRENT – The maximum current that may flow into the output load without causing damage to the comparator.

POWER CONSUMPTION – The DC power into the amplifier with no output load. The DC power will vary with signal level, but is specified as a maximum for the entire range of input-signal conditions.

PHYSICAL DIMENSIONS

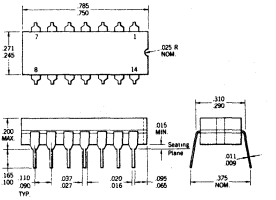
METAL CAN
5F PACKAGE



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.32 grams
Lead 5 is shorted to the can

CERAMIC DIP
6A PACKAGE

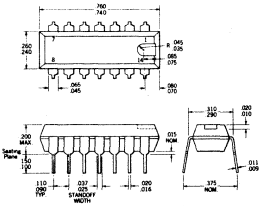
in accordance with JEDEC (TO-116) outline



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams

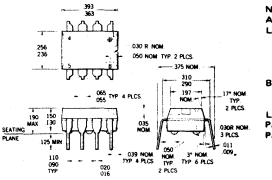
SILICONE DIP
9A PACKAGE

in accordance with JEDEC (TO-116) outline



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for .020 inch diameter lead.
Leads are tin-plated kovar
Package weight is 0.9 gram

MINI DIP
9T PACKAGE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 0.6 gram
Package material is silicone

FOR INFORMATION ON OTHER FAIRCHILD COMPARATORS AND INTERFACE CIRCUITS SEE THE FOLLOWING DATA SHEETS:

COMPARATORS
- HIGH SPEED – μA710
- DUAL HIGH SPEED – μA711
- VERY HIGH SPEED – μA760
- DUAL POWER – μA750

A/D AND D/A CONVERTERS
- 10 BIT CURRENT SOURCE – μA722
- 4 BIT CURRENT SOURCE – μA9650*
- 10 BIT A/D CONVERTER – SH8091
- 10 BIT D/A CONVERTER – SH8090
- 10 BIT LOW COST D/A – SH1500*

* To be announced

SENSE AMPLIFIERS
- DUAL – μA761, μA7524, μA7525

POWER DRIVERS
- DUAL, GENERAL PURPOSE – μA75450, μA75451
- LAMP AND RELAY DRIVERS – SH2001, SH2002, SH2200

LINE DRIVERS AND RECEIVERS
- DUAL DIFFERENTIAL – μA9614, μA9615
- EIA RS232C TRIPLE – μA9616*, μA9617*

INTERFACE
- MOS/TTμL – μA9624, μA9625
- UNIVERSAL MOS CLOCK DRIVER – SH2011*
- SILICON GATE MOS CLOCK DRIVER – SH2010*

μA735
MICROPOWER OPERATIONAL AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

FEATURES

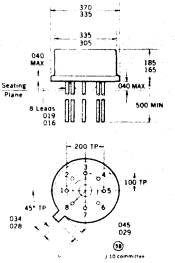
- **LOW POWER CONSUMPTION** . . . . . 100 μW
- **LOW INPUT OFFSET CURRENT** . . . . . 2 nA
- **LOW NOISE** . . . . . 0.4 pA/$\sqrt{Hz}$
- **OPERATION OVER WIDE SUPPLY RANGE** . . . ±3 V TO ±18 V
- **PIN COMPATIBLE WITH POPULAR** μA741

GENERAL DESCRIPTION — The μA735 is a low standby power consumption monolithic operational amplifier constructed on a single silicon chip using compatible thin film resistors and the Fairchild Planar* epitaxial process. It is designed for use in a wide variety of applications where very low system power consumption, low system heating, low battery drain or low input currents are required. The μA735 features very low power consumption, high input impedance, low offset voltage, low input currents, and low noise. The device has excellent common mode and power supply rejection and will operate over a wide range of supplies. In addition, it is pin compatible with the popular μA741 operational amplifier. The μA735 is ideally suited for control or telemetry applications in medical electronics, portable electronic systems, airborne systems, and missile and spacecraft systems.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18 V
Internal Power Dissipation (Note 1)	300 mW
Differential Input Voltage	±5 V
Input Voltage (Note 2)	±15 V
Peak Output Current	10 mA
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 60 seconds)	300°C

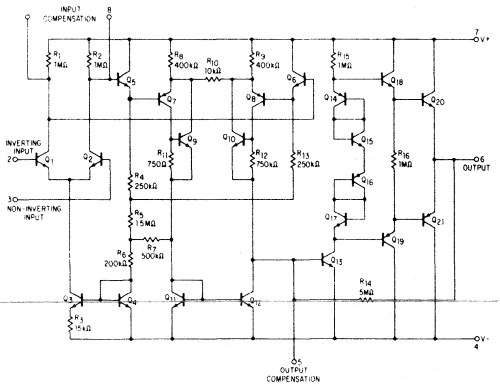
PHYSICAL DIMENSIONS
In accordance with JEDEC (TO-99) outline



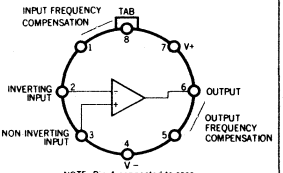
NOTES:
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.22 grams

ORDER PART NO. U5B7735312

EQUIVALENT CIRCUIT



CONNECTION DIAGRAM
(TOP VIEW)



NOTE: Pin 4 connected to case

Notes on Page 2

*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

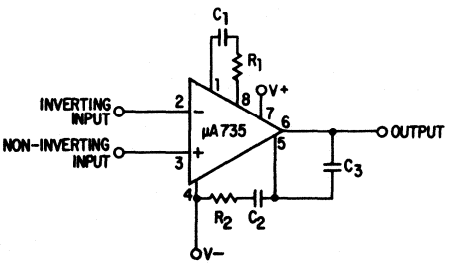
PARAMETER	CONDITIONS	V_S = ±3.0 V MIN.	TYP.	MAX.	V_S = ±15 V MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 100$ kΩ		1.0			1.0		mV
Input Offset Current			2.0			4.0		nA
Input Bias Current			5.0			10		nA
Common Mode Rejection Ratio	$R_S \leq 100$ kΩ		30			30		μV/V
Supply Voltage Rejection Ratio	$R_S \leq 100$ kΩ		25			25		μV/V
Large Signal Voltage Gain	R_L = 5.0 kΩ, V_{OUT} = ±1.0 V		20,000					
	R_L = 10 kΩ, V_{OUT} = ±10 V					40,000		
Output Voltage Swing	R_L = 5.0 kΩ		±1.2					V
	R_L = 10 kΩ					±12		V
Input Resistance			10			5.0		MΩ
Output Resistance			220			10		Ω
Power Consumption			100			6,000		μW
The following specifications apply for −55°C ≤ T_A ≤ +125°C.								
Input Offset Voltage	$R_S \leq 100$ kΩ		3.0			3.0		mV
Input Offset Current	T_A = −55°C		5.0			12		nA
Input Bias Current	T_A = −55°C		15			30		nA
Supply Voltage Rejection Ratio	$R_S \leq 100$ kΩ		50			50		μV/V
Common Mode Rejection Ratio	$R_S \leq 100$ kΩ		60			60		μV/V
Large Signal Voltage Gain	R_L = 5.0 kΩ, V_{OUT} = ±1.0 V		20,000					
	R_L = 10 kΩ, V_{OUT} = ±10 V					40,000		

NOTES:
(1) Ratings apply for case temperatures to +125°C, derate linearly at 5.6 mW/°C for ambient temperatures above 95°C.
(2) For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

FREQUENCY COMPENSATION FOR VARIOUS CLOSED LOOP GAINS

CLOSED LOOP GAIN	V_S (VOLTS)	R_1 (kΩ)	C_1 (μF)	R_2 (kΩ)	C_2 (μF)	C_3 (pF)
1	±3	39	.001	12	.01	
1	±15	39	.02	100	.0047	220
10	±3	39	.002	12	.001	
10	±15	39	.002	1	180 pF	22
100	±3			.390	.04	
100	±15	39	220 pF	1	180 pF	22
1000	±3			5.6	.002	
1000	±15	56	82 pF	SHORT	10 pF	

FREQUENCY COMPENSATION



μA735B
MICROPOWER OPERATIONAL AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

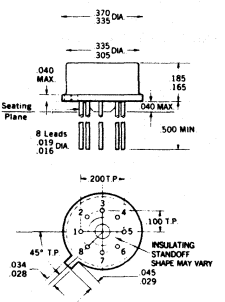
- **LOW POWER CONSUMPTION** . . . . . 100 μW
- **LOW INPUT OFFSET CURRENT** . . . . . 2 nA
- **LOW NOISE** . . . . . 0.4 pA/$\sqrt{Hz}$
- **OPERATION OVER WIDE SUPPLY RANGE** . . . ±3 V TO ±18 V
- **PIN COMPATIBLE WITH POPULAR** μA741

GENERAL DESCRIPTION — The μA735B is a low standby power consumption monolithic operational amplifier constructed on a single silicon chip using compatible thin film resistors and the Fairchild Planar* epitaxial process. It is designed for use in a wide variety of applications where very low system power consumption, low system heating, low battery drain or low input currents are required. The μA735B features very low power consumption, high input impedance, low offset voltage, low input currents, and low noise. The device has excellent common mode and power supply rejection and will operate over a wide range of supplies. In addition, it is pin compatible with the popular μA741 operational amplifier. The μA735B is ideally suited for control or telemetry applications in medical electronics, portable electronic systems, airborne systems, and missile and spacecraft systems. For full temperature range operation (−55°C to +125°C) see μA735 data sheet. (For other Fairchild Operational Amplifiers, see listing on back page.)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18 V
Internal Power Dissipation (Note 1)	300 mW
Differential Input Voltage	±5 V
Input Voltage (Note 2)	±15 V
Peak Output Current	10 mA
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−20°C to +85°C
Lead Temperature (Soldering, 60 seconds)	300°C

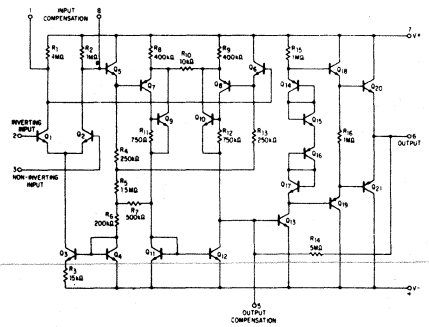
PHYSICAL DIMENSIONS
in accordance with JEDEC (TO-99) outline



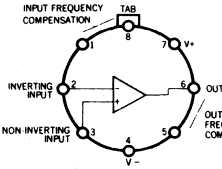
NOTES:
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.22 grams

ORDER PART NO. U5B7735333

EQUIVALENT CIRCUIT



CONNECTION DIAGRAM
(TOP VIEW)



NOTE: Pin 4 connected to case

*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

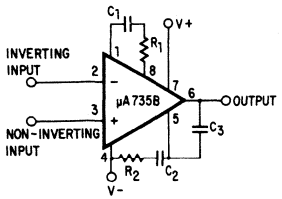
PARAMETER	CONDITIONS	V_S = ±3.0 V MIN.	TYP.	MAX.	V_S = ±15 V MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 100\ k\Omega$		1.0	3.0		1.0	3.0	mV
Input Offset Current			2.0	10		4.0	20	nA
Input Bias Current			5.0	30		10	50	nA
Common Mode Rejection Ratio	$R_S \leq 100\ k\Omega$		30	90		30	90	μV/V
Supply Voltage Rejection Ratio	$R_S \leq 100\ k\Omega$		25	150		25	150	μV/V
Large Signal Voltage Gain	R_L = 5.0 kΩ, V_{OUT} = ±1.0 V	10,000	20,000					
	R_L = 2.0 kΩ, V_{OUT} = ±10 V				25,000	40,000		
Output Voltage Swing	R_L = 5.0 kΩ	±1.2	±1.8					V
	R_L = 2.0 kΩ				±10	±12		V
Input Resistance			10			5.0		MΩ
Output Resistance			220			10		Ω
Power Consumption			150	500		6000		μW
The following specifications apply for −20 °C ≤ T_A ≤ +85 °C								
Input Offset Voltage	$R_S \leq 100\ k\Omega$		3.0	5.0		3.0	5.0	mV
Average Input Offset Voltage Drift	R_S = 50 Ω		3.0			3.0		μV/°C
Input Offset Current	T_A = −20°C		10	60		12	60	nA
Average Input Offset Current Drift			20			20		pA/°C
Input Bias Current	T_A = −20°C		15	75		30	75	nA
Supply Voltage Rejection Ratio	$R_S \leq 100\ k\Omega$		50			50		μV/V
Common Mode Rejection Ratio	$R_S \leq 100\ k\Omega$		60			60		μV/V
Large Signal Voltage Gain	R_L = 5.0 kΩ, V_{OUT} = ±1.0 V	3,000	20,000					
	R_L = 2.0 kΩ, V_{OUT} = ±10 V				16,000	40,000		

NOTES:
(1) Ratings apply for case temperatures to +85°C.
(2) For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

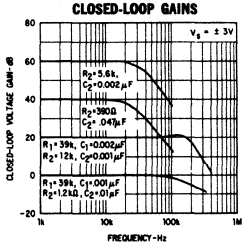
FREQUENCY COMPENSATION FOR VARIOUS CLOSED LOOP GAINS

CLOSED LOOP GAIN	V_S (VOLTS)	R_1 (kΩ)	C_1 (μF)	R_2 (kΩ)	C_2 (μF)	C_3 (pF)
1	±3	39	.001	1.2	.01	
1	±15	39	.02	0.1	.0047	220
10	±3	39	.002	12	.001	
10	±15	39	.002	1.0	180 pF	22
100	±3			.390	.047	
100	±15	39	220 pF	1.0	180 pF	22
1000	±3			5.6	.002	
1000	±15	56	82 pF	SHORT	10 pF	

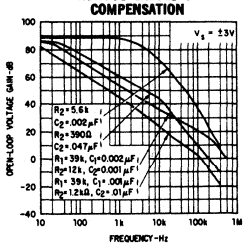
FREQUENCY COMPENSATION



FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS



OPEN-LOOP RESPONSE FOR VARIOUS VALUES OF COMPENSATION



NOTES:
1. FOR OTHER FAIRCHILD OPERATIONAL AMPLIFIERS, SEE THE FOLLOWING DATA SHEETS:

HIGH SPEED — μA715, μA715C
INSTRUMENTATION — μA725, μA725B, μA725C
TEMPERATURE STABLE PREAMPS — μA727, μA727B
FET INPUT — μA740C
FREQUENCY COMPENSATED — μA741, μA741C
DUALS — μA739C, μA749, μA749C, μA747, μA747C
HIGH PERFORMANCE — μA748, μA748C
PRECISION — μA777, μA777B, μA777C

μA735C
MICROPOWER OPERATIONAL AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

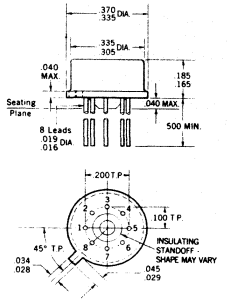
- **LOW POWER CONSUMPTION** . . . . . 100 μW
- **LOW INPUT OFFSET CURRENT** . . . . . 2 nA
- **LOW NOISE** . . . . . 0.4 pA/$\sqrt{Hz}$
- **OPERATION OVER WIDE SUPPLY RANGE** . . . ±3 V TO ±18 V
- **PIN COMPATIBLE WITH POPULAR μA741**

GENERAL DESCRIPTION — The μA735C is a low standby-power consumption monolithic operational amplifier constructed on a single silicon chip using compatible thin film resistors and the Fairchild Planar* epitaxial process. It is designed for use in a wide variety of applications where very low system power consumption, low system heating, low battery drain or low input currents are required. The μA735C features very low power consumption, high input impedance, low offset voltage, low input currents, and low noise. The device has excellent common mode and power supply rejection and will operate over a wide range of supplies. In addition, it is pin compatible with the popular μA741 operational amplifier. The μA735C is ideally suited for control or telemetry applications in medical electronics, portable electronic systems, airborne systems, and missile and spacecraft systems. For full temperature range operation (−55°C to +125°C) see μA735 data sheet. (For other Fairchild Operational Amplifiers, see listing on back page.)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18 V
Internal Power Dissipation (Note 1)	300 mW
Differential Input Voltage	±5 V
Input Voltage (Note 2)	±15 V
Peak Output Current	10 mA
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 60 seconds)	300°C

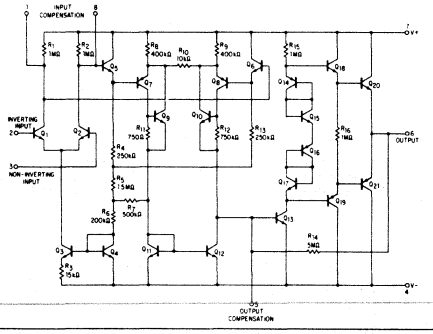
PHYSICAL DIMENSIONS
In accordance with JEDEC (TO-99) outline



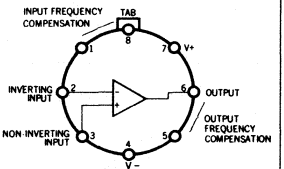
NOTES:
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.22 grams

ORDER PART NO. U5B7735393

EQUIVALENT CIRCUIT



CONNECTION DIAGRAM
(TOP VIEW)



NOTE: Pin 4 connected to case

*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR

FAIRCHILD LINEAR INTEGRATED CIRCUITS μA735C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

PARAMETER	TEST CONDITIONS	V_S = ±3.0 V MIN.	TYP.	MAX.	V_S = ±15 V MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 100$ kΩ		1.0	4.0		1.0	4.0	mV
Input Offset Current			2.0	20		4.0	40	nA
Input Bias Current			5.0	60		10	110	nA
Common Mode Rejection Ratio	$R_S \leq 100$ kΩ		30	90		30	90	μV/V
Supply Voltage Rejection Ratio	$R_S \leq 100$ kΩ		25	250		25	250	μV/V
Large Signal Voltage Gain	R_L = 5.0 kΩ, V_{OUT} = ±1.0 V	5,000	20,000					
	R_L = 2.0 kΩ, V_{OUT} = ±10 V				25,000	40,000		
Output Voltage Swing	R_L = 5.0 kΩ	±1.2	±1.8					V
	R_L = 2.0 kΩ				±10	±12		V
Input Resistance			10			5.0		MΩ
Output Resistance			220			10		Ω
Power Consumption			150	750		6000		μW
The following specifications apply for 0°C ≤ T_A ≤ +70°C:								
Input Offset Voltage	$R_S \leq 100$ kΩ		3.0	7.5		3.0	7.5	mV
Average Input Offset Voltage Drift	R_S = 50 Ω		3.0			3.0		μV/°C
Input Offset Current	T_A = 0°C		10	60		12	60	nA
Average Input Offset Current Drift			20			20		pA/°C
Input Bias Current	T_A = 0°C		15	75		30	110	nA
Supply Voltage Rejection Ratio	$R_S \leq 100$ kΩ		50			50		μV/V
Common Mode Rejection Ratio	$R_S \leq 100$ kΩ		60			60		μV/V
Large Signal Voltage Gain	R_L = 5.0 kΩ, V_{OUT} = ±1.0 V		20,000					
	R_L = 2.0 kΩ, V_{OUT} = ±10 V					40,000		

NOTES:

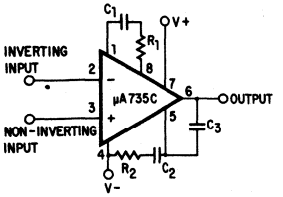
(1) Ratings apply for case temperatures to +70°C.

(2) For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

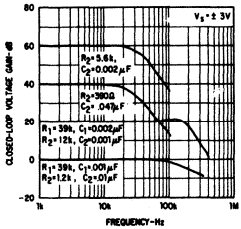
FREQUENCY COMPENSATION FOR VARIOUS CLOSED LOOP GAINS

CLOSED LOOP GAIN	V_S (VOLTS)	R_1 (kΩ)	C_1 (μF)	R_2 (kΩ)	C_2 (μF)	C_3 (pF)
1	±3	39	.001	1.2	.01	
1	±15	39	.02	0.1	.0047	220
10	±3	39	.002	12	.001	
10	±15	39	.002	1.0	180 pF	22
100	±3			.390	.047	
100	±15	39	220 pF	1.0	180 pF	22
1000	±3			5.6	.002	
1000	±15	56	82 pF	SHORT	10 pF	

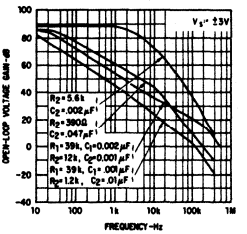
FREQUENCY COMPENSATION



FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS



OPEN-LOOP RESPONSE FOR VARIOUS VALUES OF COMPENSATION



NOTE:

FOR OTHER FAIRCHILD OPERATIONAL AMPLIFIERS, SEE THE FOLLOWING DATA SHEETS:

HIGH SPEED — μA715, μA715C
INSTRUMENTATION — μA725, μA725B, μA725C
TEMPERATURE STABLE PREAMPS — μA727, μA727B
FET INPUT — μA740C
FREQUENCY COMPENSATED — μA741, μA741C
DUALS — μA739C, μA749, μA749C, μA747, μA747C
HIGH PERFORMANCE — μA748, μA748C
PRECISION — μA777, μA777B, μA777C

μA739C

DUAL LOW-NOISE OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA739C consists of two identical operational amplifiers constructed on a single silicon chip using the Fairchild Planar* epitaxial process. These low-noise, high-gain amplifiers exhibit extremely stable operating characteristics over a wide range of supply voltage and temperatures. The device is intended for a variety of applications requiring two high performance operational amplifiers.
(For other Fairchild Operational Amplifiers, see listing on page 2.)

- **SINGLE OR DUAL SUPPLY OPERATION**
- **LOW NOISE FIGURE, 2.0 dB**
- **HIGH GAIN, 20,000 V/V**
- **LARGE COMMON MODE RANGE, ±11 V**
- **EXCELLENT GAIN STABILITY VS. SUPPLY VOLTAGE**
- **NO LATCH-UP**
- **OUTPUT SHORT CIRCUIT PROTECTED**

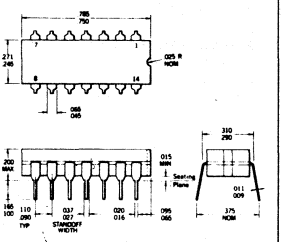
TYPICAL APPLICATIONS

- **DUAL OPERATIONAL AMPLIFIER**
- **PHONO AND TAPE STEREO PREAMPLIFIER**
- **TV REMOTE CONTROL RECEIVER**
- **DUAL COMPARATOR**
- **SENSE AMPLIFIER**
- **OSCILLATOR**
- **ACTIVE FILTER**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18 V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±5 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	−55°C to +125°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 10 seconds)	260°C
Output Short-Circuit Duration, $T_A = 25°C$ (Note 3)	30 seconds

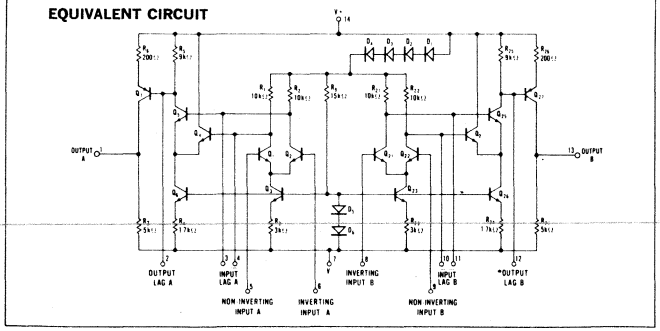
PHYSICAL DIMENSIONS
In accordance with JEDEC (TO-116) outline
14 Lead Dual In-Line



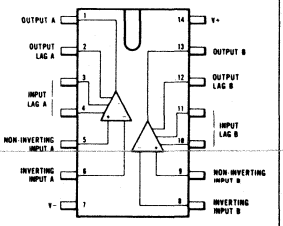
NOTES
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for .020 inch diameter lead.
Leads are tin-plated kovar
Package weight is 2.0 grams

ORDER PART NO. U6A7739393

EQUIVALENT CIRCUIT



CONNECTION DIAGRAM
(TOP VIEW)



Notes on page 2

*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $R_L = 50$ kΩ to Pin 7, $T_A = 25°C$ unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 200\ \Omega$		1.0	6.0	mV
Input Offset Current			50	1000	nA
Input Bias Current			300	2000	nA
Input Resistance		37	150		kΩ
Large-Signal Voltage Gain	$V_{OUT} = \pm 5.0$ V	6500	20,000		V/V
Positive Output Voltage Swing		+12	+13		V
Negative Output Voltage Swing		−14	−15		V
Output Resistance	f = 1.0 kHz		5.0		kΩ
Input Voltage Range		±10	±11		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		50		μV/V
Power Consumption	$V_{OUT} = 0$		270	420	mW
Supply Current	$V_{OUT} = 0$		9.0	14	mA
Broadband Noise Figure	$R_S = 5.0$kΩ, BW = 10 Hz to 10 kHz		2.0		dB
Turn On Delay (See Figure 1)	Open Loop, $V_{IN} = \pm 20$ mV		0.2		μs
Turn Off Delay (See Figure 1)	Open Loop, $V_{IN} = \pm 20$ mV		0.3		μs
Slew Rate (unity gain) (See Figure 2)	$C_1 = 0.1\ \mu F$, $R_1 = 4.7\ \Omega$		1.0		V/μs
Channel Separation (See Figure 3)	$R_S \leq 10$ kΩ, f = 10 kHz		140		dB
The following specifications apply for $V_S = \pm 4.0$ V, $T_A = 25°C$					
Input Offset Voltage	$R_S \leq 200\ \Omega$		1.0	6.0	mV
Input Offset Current			50	1000	nA
Input Bias Current			300		nA
Supply Current	$V_{OUT} = 0$		2.5		mA
Power Consumption	$V_{OUT} = 0$		20		mW
Large-Signal Voltage Gain	$V_{OUT} = \pm 1.0$ V	2500	15,000		V/V
Positive Output Voltage Swing		+2.5	+2.8		V
Negative Output Voltage Swing		−3.6	−4.0		V

NOTES:
(1) Rating applies at ambient temperature below 60°C. Derate at 7.7 mw/°C above 60°C.
(2) For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
(3) Short circuit may be to ground or either supply.

PULSE RESPONSE WAVEFORMS

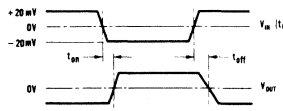


Figure 1

FREQUENCY RESPONSE TEST CIRCUIT

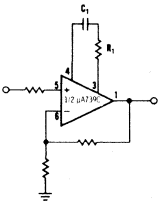


Figure 2

CHANNEL SEPARATION TEST CIRCUIT

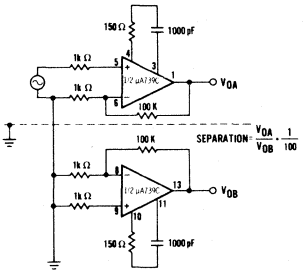


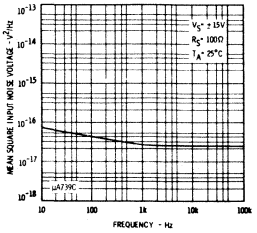
Figure 3

NOTE:
FOR OTHER FAIRCHILD OPERATIONAL AMPLIFIERS, SEE THE FOLLOWING DATA SHEETS:

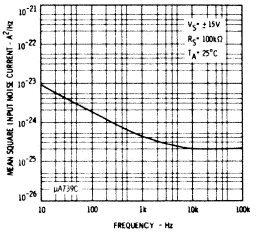
HIGH SPEED — μA715, μA715C
INSTRUMENTATION — μA725, μA725B, μA725C
TEMPERATURE STABLE PREAMPS — μA727, μA727B
MICROPOWER — μA735, μA735B, μA735C
FET INPUT — μA740C
FREQUENCY COMPENSATED — μA741, μA741C
DUALS — μA749, μA749C, μA747, μA747C
HIGH PERFORMANCE — μA748, μA748C
PRECISION — μA777, μA777B, μA777C

TYPICAL PERFORMANCE CURVES

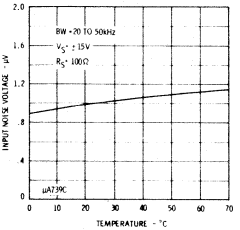
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



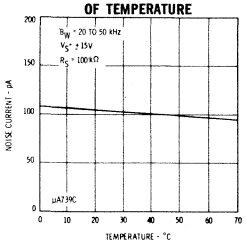
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



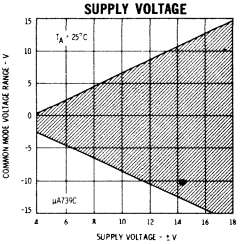
WIDE BAND INPUT NOISE VOLTAGE AS A FUNCTION OF TEMPERATURE



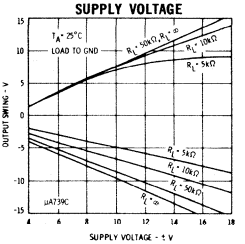
WIDE BAND INPUT NOISE CURRENT AS A FUNCTION OF TEMPERATURE



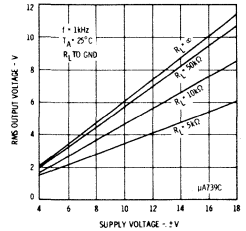
COMMON MODE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



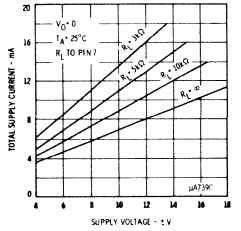
TYPICAL OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



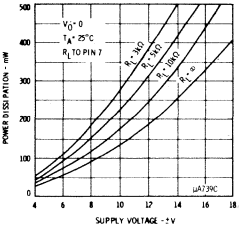
OUTPUT CAPABILITY AS A FUNCTION OF SUPPLY VOLTAGE



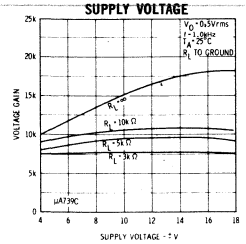
TOTAL SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



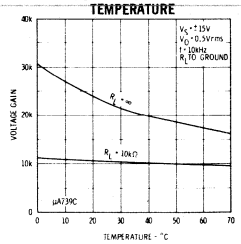
TOTAL POWER DISSIPATION AS A FUNCTION OF SUPPLY VOLTAGE AND LOAD



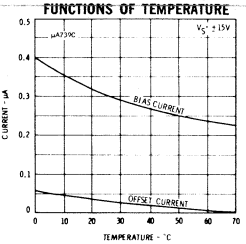
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



OPEN LOOP GAIN AS A FUNCTION OF TEMPERATURE

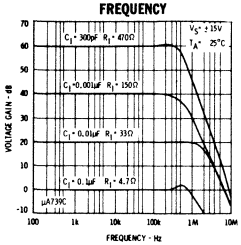


INPUT OFFSET CURRENT AND BIAS CURRENT AS FUNCTIONS OF TEMPERATURE

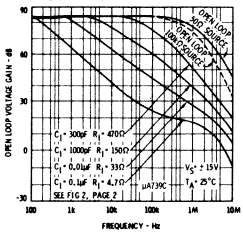


TYPICAL PERFORMANCE CURVES

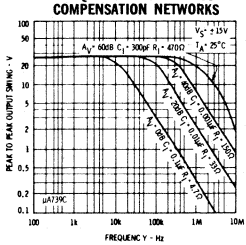
CLOSED LOOP GAIN AS A FUNCTION OF FREQUENCY



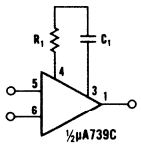
OPEN LOOP FREQUENCY RESPONSE USING RECOMMENDED COMPENSATION NETWORKS



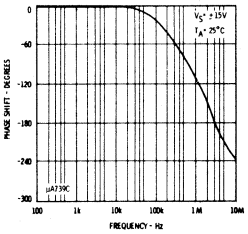
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS COMPENSATION NETWORKS



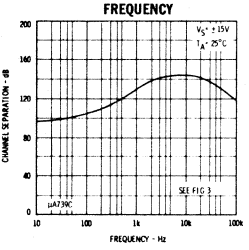
FREQUENCY COMPENSATION NETWORK



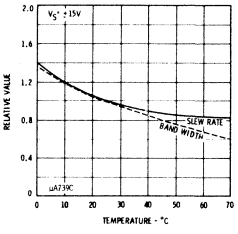
OPEN LOOP PHASE SHIFT WITHOUT COMPENSATION



CHANNEL SEPARATION AS A FUNCTION OF FREQUENCY

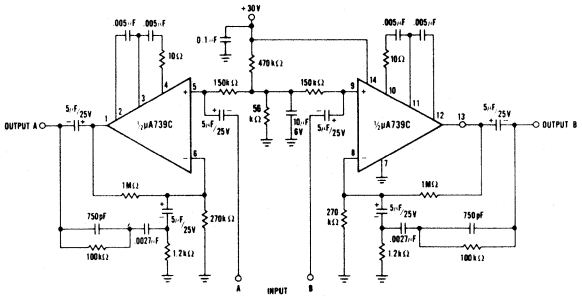


CHANGE OF A.C. CHARACTERISTICS WITH TEMPERATURE



TYPICAL APPLICATION

STEREO PHONO PREAMPLIFIER—RIAA EQUALIZED



TYPICAL PERFORMANCE

Gain 40 dB at 1 kHz, RIAA equalized
Input overload point, 80 mV rms
Noise level, 2μV referred to input
Signal to noise ratio, 74 dB below 10 mV
Channel separation @ 1 kHz, 80 dB

μA740
FET INPUT OPERATIONAL AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

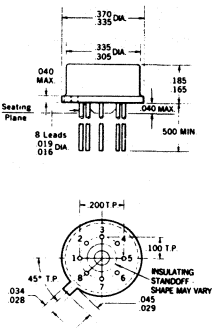
FEATURES
- **HIGH INPUT IMPEDANCE . . . 1,000,000 MΩ**
- **NO FREQUENCY COMPENSATION REQUIRED**
- **SHORT-CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **NO LATCH UP**

GENERAL DESCRIPTION — The μA740 is a high performance FET input operational amplifier constructed on a single silicon chip, using the Fairchild Planar* epitaxial process. It is intended for a wide range of analog applications where very high input impedance is required and features very low input offset current and very low input bias current. High slew rate, high common mode voltage range and absence of "latch up" make the μA740 ideal for use as a voltage follower. The high gain and wide range of operating voltages provide superior performance in active filters, integrators, summing amplifiers, sample and holds, transducer amplifiers, and other general feedback applications. The μA740 is short circuit protected and has the same pin configuration as the popular μA741 operational amplifier. No external components for frequency compensation are required as the internal 6 dB/octave roll-off insures stability in closed loop applications. (For other Fairchild operational amplifiers, see listing on back page.)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22 V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Voltage between Offset Null and V⁺	±0.5 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 60 seconds)	300°C
Output Short-Circuit Duration (Note 3)	Indefinite

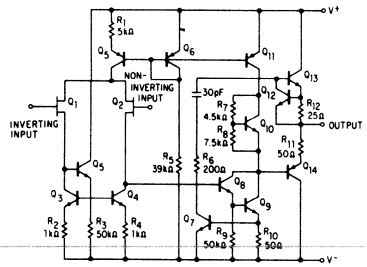
PHYSICAL DIMENSIONS
in accordance with JEDEC (TO-99) outline



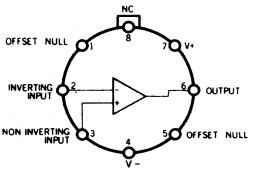
NOTES:
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.22 grams

ORDER PART NO. U5B7740312

EQUIVALENT CIRCUIT



CONNECTION DIAGRAM
(TOP VIEW)



NOTE: PIN 4 CONNECTED TO CASE

NOTES:
(1) Rating applies for case temperatures to 125°C; derate linearly at 6.5 mW/°C for ambient temperatures above +75°C.
(2) For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.
(3) Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

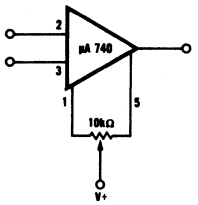
*Planar is a patented Fairchild process.

FAIRCHILD SEMICONDUCTOR

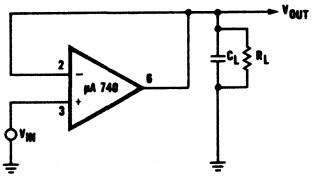
ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_C = 25°C$ unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 100$ kΩ		10	20	mV
Input Offset Current			40		pA
Input Current (either input)			100	200	pA
Input Resistance			1,000,000		MΩ
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	50,000	1,000,000		
Output Resistance			75		Ω
Output Short-Circuit Current			20		mA
Common Mode Rejection Ratio		64	80		dB
Supply Voltage Rejection Ratio			70	300	μV/V
Supply Current			4.2	5.2	mA
Power Consumption			126	156	mW
Slew Rate			6.0		V/μs
Unity Gain Bandwidth			3.0		MHz
Transient Response (Unity Gain)	$C_L \leq 100$ pF, $R_L = 2$ kΩ, $V_{in} = 100$ mV				
Risetime			110		ns
Overshoot			10	20	%
The following specifications apply for $T_C = -55°C$ to $+85°C$:					
Input Voltage Range		±10		±12	V
Large Signal Voltage Gain		25,000			
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		V
Input Offset Voltage	$R_S \leq 100$ kΩ		15	30	mV
Input Offset Current	$T_A = -55°C$		185		pA
	$T_A = +85°C$		30		pA
Input Current (either input)	$T_A = -55°C$			200	pA
	$T_A = +85°C$		2.5	4.0	nA

VOLTAGE OFFSET NULL CIRCUIT



TRANSIENT RESPONSE TEST CIRCUIT



NOTES:

FOR OTHER FAIRCHILD OPERATIONAL AMPLIFIERS, SEE THE FOLLOWING DATA SHEETS:

HIGH SPEED — μA715, μA715C
INSTRUMENTATION — μA725, μA725B, μA725C
TEMPERATURE STABLE PREAMPS — μA727, μA727B
MICROPOWER — μA735, μA735B, μA735C
FREQUENCY COMPENSATED — μA741, μA741C
DUALS — μA739C, μA749, μA749C, μA747, μA747C
HIGH PERFORMANCE — μA748, μA748C
PRECISION — μA777, μA777B, μA777C

μA740C
FET INPUT OPERATIONAL AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

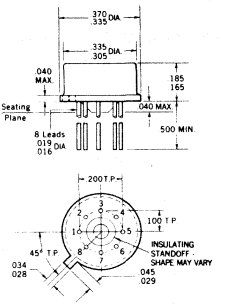
- **HIGH INPUT IMPEDANCE . . . 1,000,000 MΩ**
- **NO FREQUENCY COMPENSATION REQUIRED**
- **SHORT-CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **NO LATCH UP**

GENERAL DESCRIPTION — The μA740C is a high performance FET input operational amplifier constructed on a single silicon chip, using the Fairchild Planar* epitaxial process. It is intended for a wide range of analog applications where very high input impedance is required and features very low input offset current and very low input bias current. High slew rate, high common mode voltage range and absence of "latch up" make the μA740C ideal for use as a voltage follower. The high gain and wide range of operating voltages provide superior performance in active filters, integrators, summing amplifiers, sample and holds, transducer amplifiers, and other general feedback applications. The μA740C is short circuit protected and has the same pin configuration as the popular μA741 operational amplifier. No external components for frequency compensation are required as the internal 6 dB/octave roll-off insures stability in closed loop applications. For full temperature range operation (−55°C to +125°C), see the μA740 data sheet. (For other Fairchild operational amplifiers, see listing on back page.)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22 V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Voltage between Offset Null and V⁺	±0.5 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 60 seconds)	300°C
Output Short-Circuit Duration (Note 3)	Indefinite

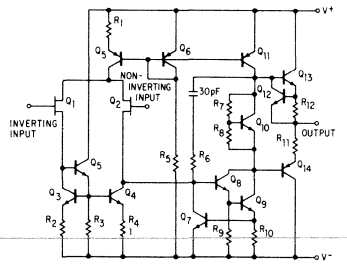
PHYSICAL DIMENSIONS
in accordance with JEDEC (TO-99) outline



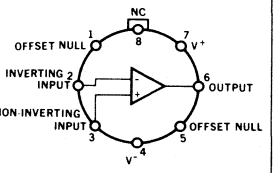
NOTES:
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.22 grams

ORDER PART NO. U5B7740393

EQUIVALENT CIRCUIT



CONNECTION DIAGRAM
(TOP VIEW)



NOTE: PIN 4 CONNECTED TO CASE

NOTES:
(1) Rating applies for ambient temperatures to +70°C.
(2) For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
(3 Short circuit may be to ground or either supply. Rating applies to +70°C ambient temperature.

*Planar is a patented Fairchild process.

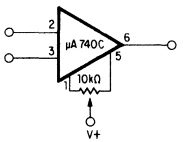
FAIRCHILD
SEMICONDUCTOR

FAIRCHILD LINEAR INTEGRATED CIRCUITS μA740C

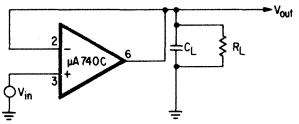
ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_C = 25°C$ unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 100$ kΩ		30		mV
Input Offset Current			60		pA
Input Current (either input)			0.1	2.0	nA
Input Resistance			1,000,000		MΩ
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V		1,000,000		
Output Resistance			75		Ω
Output Short-Circuit Current			20		mA
Supply Current			4.2	8.0	mA
Power Consumption			126	240	mW
Slew Rate			6.0		V/μs
Unity Gain Bandwidth			1.0		MHz
Transient Response (Unity Gain)	$C_L \leq 100$ pF, $R_L = 2$ kΩ, $V_{in} = 100$ mV				
Risetime			300		ns
Overshoot			10		%
The following specifications apply for $0°C \leq T_A \leq +70°C$:					
Input Voltage Range			±12		V
Common Mode Rejection Ratio			80		dB
Supply Voltage Rejection Ratio			70		μV/V
Large Signal Voltage Gain			500,000		
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		V
Input Offset Voltage			30		mV
Input Offset Current			60		pA
Input Current (either input)			1.1	10	nA

VOLTAGE OFFSET NULL CIRCUIT



TRANSIENT RESPONSE TEST CIRCUIT



NOTES:

FOR OTHER FAIRCHILD OPERATIONAL AMPLIFIERS, SEE THE FOLLOWING DATA SHEETS:

HIGH SPEED — μA715, μA715C
INSTRUMENTATION — μA725, μA725B, μA725C
TEMPERATURE STABLE PREAMPS — μA727, μA727B
MICROPOWER — μA735, μA735B, μA735C
FREQUENCY COMPENSATED — μA741, μA741C
DUALS — μA739C, μA749, μA749C, μA747, μA747C
HIGH PERFORMANCE — μA748, μA748C
PRECISION — μA777, μA777B, μA777C

μA741

FREQUENCY-COMPENSATED OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

FEATURES:

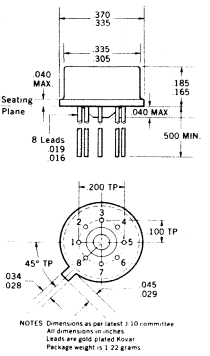
- **NO FREQUENCY COMPENSATION REQUIRED**
- **SHORT-CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **LOW POWER CONSUMPTION**
- **NO LATCH UP**

GENERAL DESCRIPTION — The μA741 is a high performance monolithic operational amplifier constructed on a single silicon chip, using the Fairchild Planar* epitaxial process. It is intended for a wide range of analog applications. High common mode voltage range and absence of "latch-up" tendencies make the μA741 ideal for use as a voltage follower. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier, and general feedback applications. The μA741 is short-circuit protected, has the same pin configuration as the popular μA709 operational amplifier, but requires no external components for frequency compensation. The internal 6dB/octave roll-off insures stability in closed loop applications.

ABSOLUTE MAXIMUM RATINGS

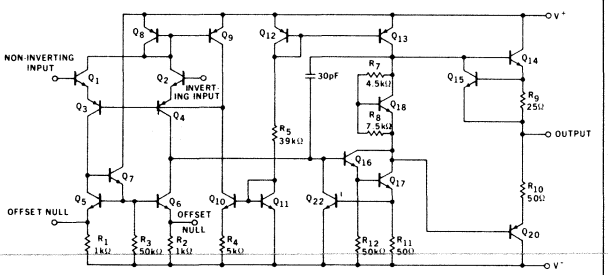
Supply Voltage	±22 V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Voltage between Offset Null and V⁻	±0.5 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 60 sec)	300°C
Output Short-Circuit Duration (Note 3)	Indefinite

PHYSICAL DIMENSIONS
in accordance with
JEDEC (TO-99) outline

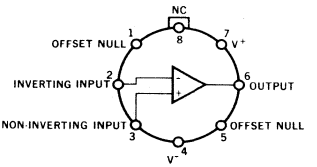


ORDER PART NO. U5B7741312

EQUIVALENT CIRCUIT



CONNECTION DIAGRAM
(TOP VIEW)



NOTE: PIN 4 CONNECTED TO CASE

***ALSO AVAILABLE IN DIL ORDER PART NO. U6A7741312**

NOTES:

(1) Rating applies for case temperatures to 125°C; derate linearly at 6.5 mW/°C for ambient temperatures above +75°C.
(2) For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
(3) Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

*Planar is a patented Fairchild process.

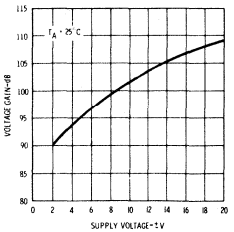
FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified)

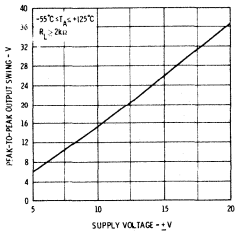
PARAMETERS (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	5.0	mV
Input Offset Current			20	200	nA
Input Bias Current			80	500	nA
Input Resistance		0.3	2.0		MΩ
Input Capacitance			1.4		pF
Offset Voltage Adjustment Range			±15		mV
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	50,000	200,000		
Output Resistance			75		Ω
Output Short-Circuit Current			25		mA
Supply Current			1.7	2.8	mA
Power Consumption			50	85	mW
Transient Response (unity gain)	$V_{in} = 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF				
Risetime			0.3		μs
Overshoot			5.0		%
Slew Rate	$R_L \geq 2$ kΩ		0.5		V/μs
The following specifications apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	6.0	mV
Input Offset Current	$T_A = +125°C$		7.0	200	nA
	$T_A = -55°C$		85	500	nA
Input Bias Current	$T_A = +125°C$		0.03	0.5	μA
	$T_A = -55°C$		0.3	1.5	μA
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150	μV/V
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	25,000			
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		V
Supply Current	$T_A = +125°C$		1.5	2.5	mA
	$T_A = -55°C$		2.0	3.3	mA
Power Consumption	$T_A = +125°C$		45	75	mW
	$T_A = -55°C$		60	100	mW

TYPICAL PERFORMANCE CURVES

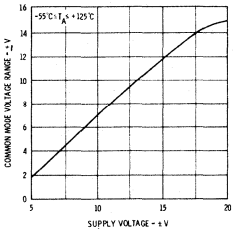
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE

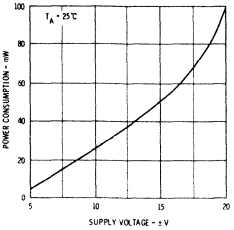


INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

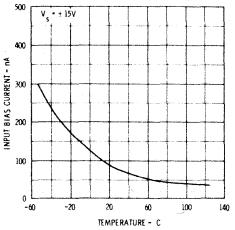


TYPICAL PERFORMANCE CURVES

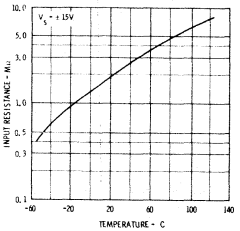
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



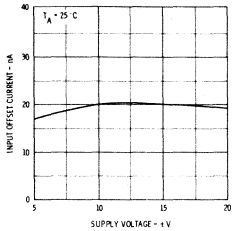
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



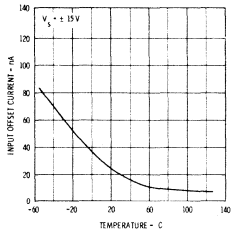
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



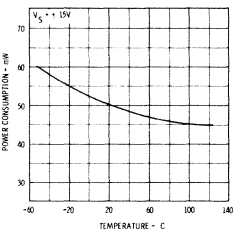
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



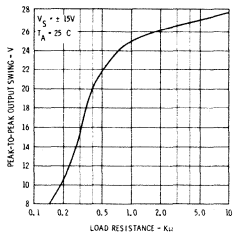
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



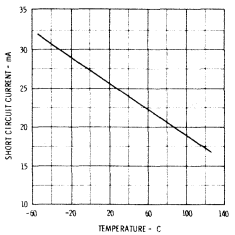
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



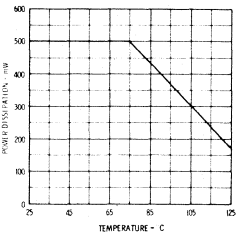
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



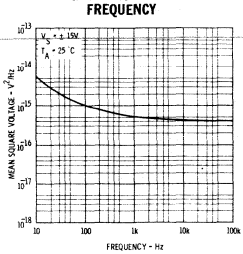
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



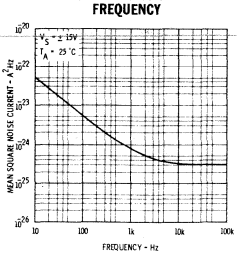
ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



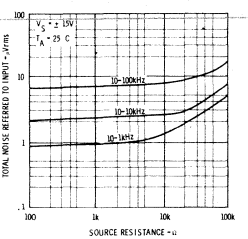
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY

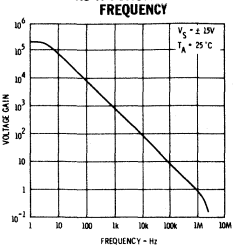


BROADBAND NOISE FOR VARIOUS BANDWIDTHS

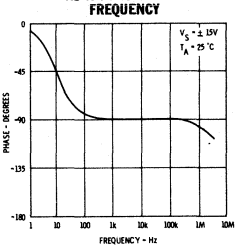


TYPICAL PERFORMANCE CURVES

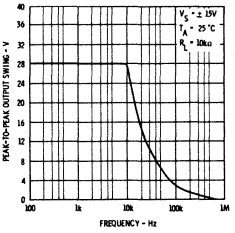
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



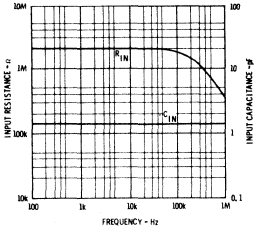
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



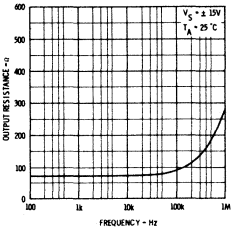
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



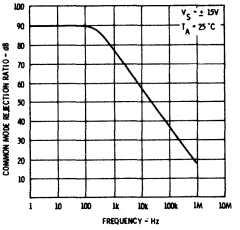
INPUT RESISTANCE AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY



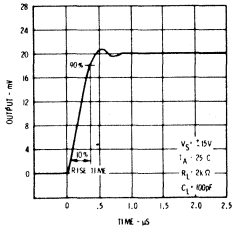
OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY



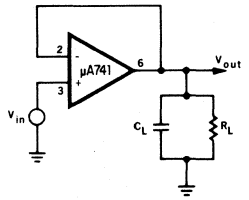
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



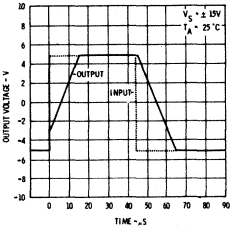
TRANSIENT RESPONSE



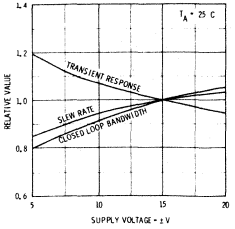
TRANSIENT RESPONSE TEST CIRCUIT



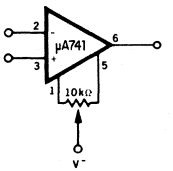
VOLTAGE FOLLOWER LARGE-SIGNAL PULSE RESPONSE



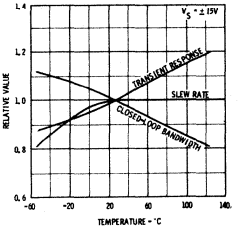
FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE



VOLTAGE OFFSET NULL CIRCUIT



FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE

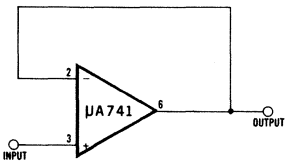


DEFINITION OF TERMS

INPUT OFFSET VOLTAGE — That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.
INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the output at zero volts.
INPUT BIAS CURRENT — The average of the two input currents.
INPUT RESISTANCE — The resistance looking into either input terminal with the other grounded.
INPUT CAPACITANCE — The capacitance looking into either input terminal with the other grounded.
LARGE-SIGNAL VOLTAGE GAIN — The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.
OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.
OUTPUT SHORT-CIRCUIT CURRENT — The maximum output current available from the amplifier with the output shorted to ground or to either supply.
SUPPLY CURRENT — The DC current from the supplies required to operate the amplifier with the output at zero and with no load current.
POWER CONSUMPTION — The DC power required to operate the amplifier with the output at zero and with no load current.
TRANSIENT RESPONSE — The closed-loop step-function response of the amplifier under small-signal conditions.
INPUT VOLTAGE RANGE — The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.
INPUT COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.
SUPPLY VOLTAGE REJECTION RATIO — The ratio of the change in input offset voltage to the change in supply voltage producing it.
OUTPUT VOLTAGE SWING — The peak output swing, referred to zero, that can be obtained without clipping.

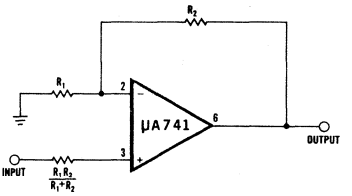
TYPICAL APPLICATIONS

UNITY-GAIN VOLTAGE FOLLOWER



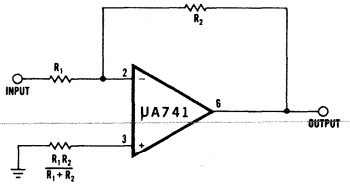
$R_{IN} = 400\ M\Omega$
$C_{IN} = 1\ pF$
$R_{out} << 1\ \Omega$
B.W. $= 1$ MHz

NON-INVERTING AMPLIFIER



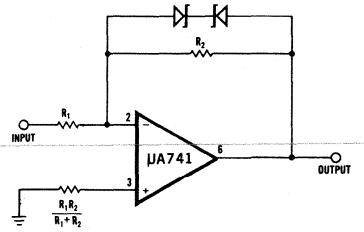
GAIN	R_1	R_2	B.W.	R_{IN}
10	1 kΩ	9 kΩ	100 kHz	400 MΩ
100	100 Ω	9.9 kΩ	10 kHz	280 MΩ
1000	100 Ω	99.9 kΩ	1 kHz	80 MΩ

INVERTING AMPLIFIER



GAIN	R_1	R_2	B.W.	R_{IN}
1	10 kΩ	10 kΩ	1 MHz	10 kΩ
10	1 kΩ	10 kΩ	100 kHz	1 kΩ
100	1 kΩ	100 kΩ	10 kHz	1 kΩ
1000	100 Ω	100 kΩ	1 kHz	100 Ω

CLIPPING AMPLIFIER

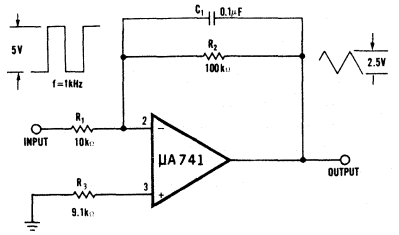


$\frac{E_{out}}{E_{IN}} = \frac{R_2}{R_1}$ if $|E_{out}| \leq V_Z + 0.7\ V$

where V_Z = Zener breakdown voltage

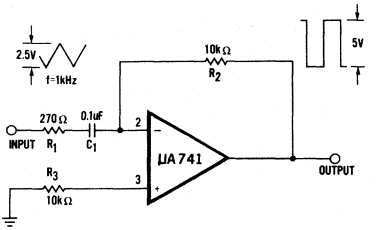
TYPICAL APPLICATIONS

SIMPLE INTEGRATOR



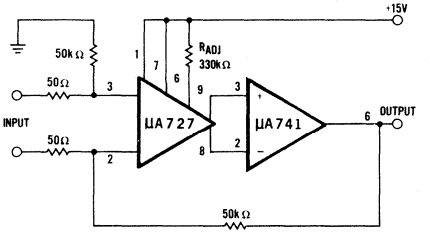
$$E_{out} = -\frac{1}{R_1 C_1}\int E_{IN}dt$$

SIMPLE DIFFERENTIATOR



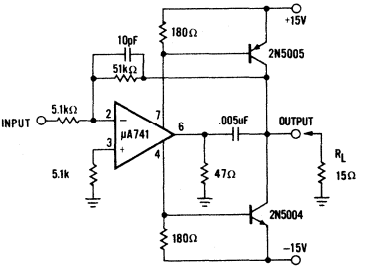
$$E_{out} = -R_2 C_1 \frac{dE_{IN}}{dt}$$

LOW DRIFT LOW NOISE AMPLIFIER

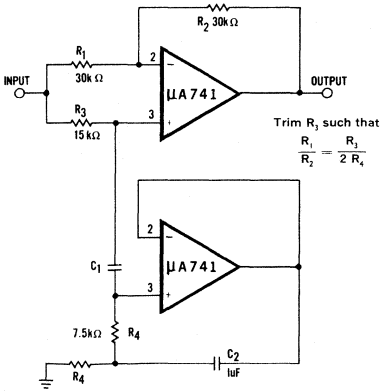


Voltage Gain = 10^9
Input Offset Voltage Drift = 0.6 μV/°C
Input Offset Current Drift = 2.0 pA/°C

HIGH SLEW RATE POWER AMPLIFIER

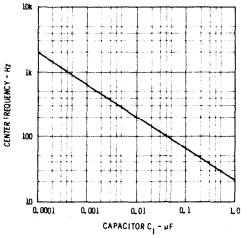


NOTCH FILTER USING THE μA741 AS A GYRATOR



Trim R_3 such that $\frac{R_1}{R_2} = \frac{R_3}{2R_4}$

NOTCH FREQUENCY AS A FUNCTION OF C_1



μA741C

INTERNALLY-COMPENSATED OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

FEATURES:

- **NO FREQUENCY COMPENSATION REQUIRED**
- **SHORT-CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **LOW POWER CONSUMPTION**
- **NO LATCH UP**

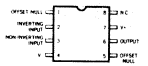
GENERAL DESCRIPTION — The μA741C is a high performance monolithic operational amplifier constructed on a single silicon chip, using the Fairchild Planar* epitaxial process. It is intended for a wide range of analog applications. High common mode voltage range and absence of "latch-up" tendencies make the μA741C ideal for use as a voltage follower. The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier, and general feedback applications. The μA741C is short-circuit protected, has the same pin configuration as the popular μA709C operational amplifier, but requires no external components for frequency compensation. The internal 6dB/octave roll-off insures stability in closed loop applications. For full temperature range operation (−55°C to +125°C) see μA741 data sheet.

ABSOLUTE MAXIMUM RATINGS

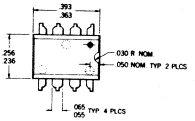
Supply Voltage	±18 V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Voltage between Offset Null and V⁻	±0.5 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 60 sec)	300°C
Output Short-Circuit Duration (Note 3)	Indefinite

PHYSICAL DIMENSIONS
in accordance with
JEDEC (TO-99) outline

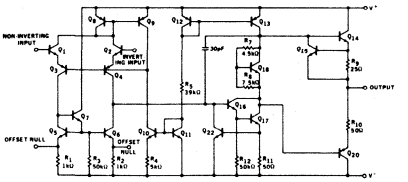
MINI DIP



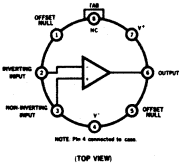
ORDER PART NO. U9T7741393

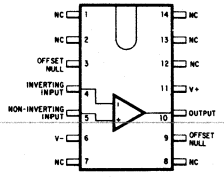


EQUIVALENT CIRCUIT



CONNECTION DIAGRAMS





ORDER INFORMATION

PART NO. U5B7741393

PACKAGE IN ACCORDANCE WITH TO99

PART NO. U6A7741393

CERAMIC PACKAGE IN ACCORDANCE WITH TO116

NOTES:

(1) Rating applies for ambient temperatures to +70°C.

(2) For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

(3) Short circuit may be to ground or either supply.

*Planar is a patented Fairchild process.

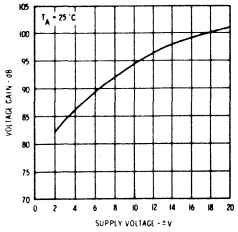
FAIRCHILD SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified)

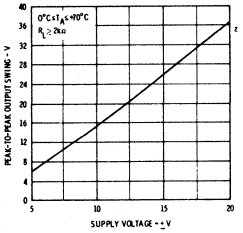
PARAMETERS (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ		2.0	6.0	mV
Input Offset Current			20	200	nA
Input Bias Current			80	500	nA
Input Resistance		0.3	2.0		MΩ
Input Capacitance			1.4		pF
Offset Voltage Adjustment Range			±15		mV
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150	μV/V
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	20,000	200,000		
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		V
Output Resistance			75		Ω
Output Short-Circuit Current			25		mA
Supply Current			1.7	2.8	mA
Power Consumption			50	85	mW
Transient Response (unity gain)	$V_{in} = 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF				
Risetime			0.3		μs
Overshoot			5.0		%
Slew Rate	$R_L \geq 2$ kΩ		0.5		V/μs
The following specifications apply for $0°C \leq T_A \leq +70°C$:					
Input Offset Voltage				7.5	mV
Input Offset Current				300	nA
Input Bias Current				800	nA
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	15,000			
Output Voltage Swing	$R_L \geq 2$ kΩ	±10	±13		V

TYPICAL PERFORMANCE CURVES

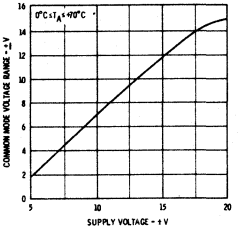
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE

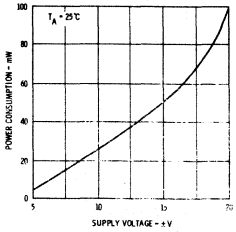


INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

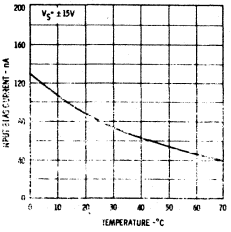


TYPICAL PERFORMANCE CURVES

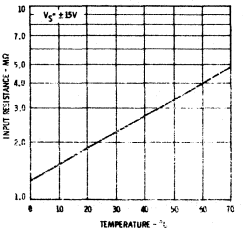
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



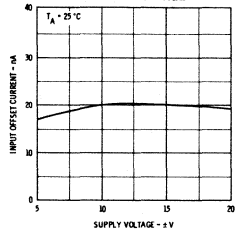
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



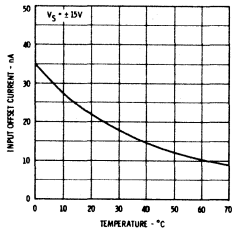
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



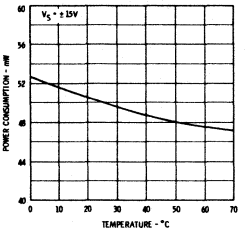
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



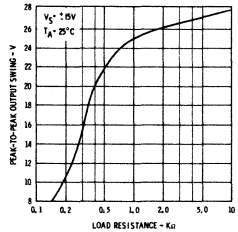
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



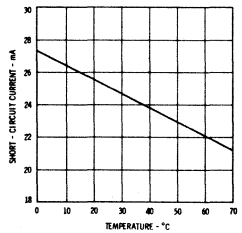
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



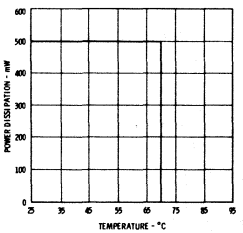
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



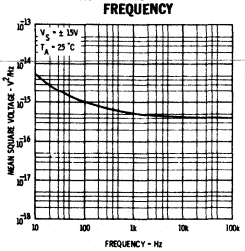
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



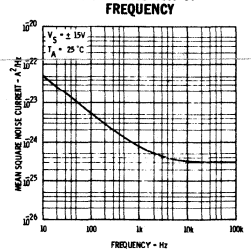
ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



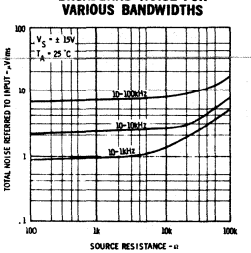
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY

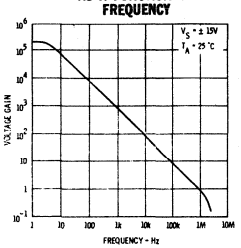


BROADBAND NOISE FOR VARIOUS BANDWIDTHS

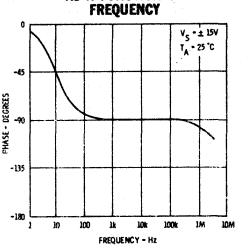


TYPICAL PERFORMANCE CURVES

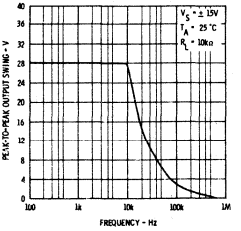
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



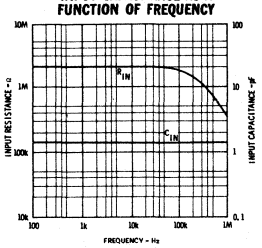
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



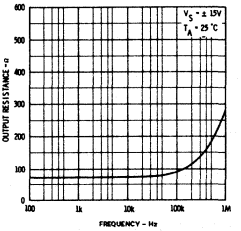
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



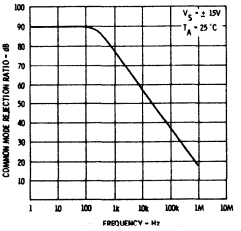
INPUT RESISTANCE AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY



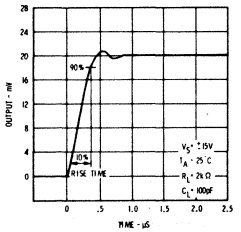
OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY



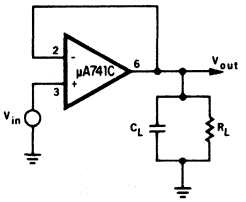
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



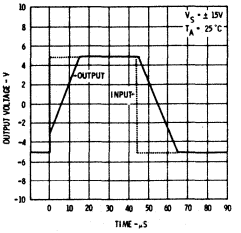
TRANSIENT RESPONSE



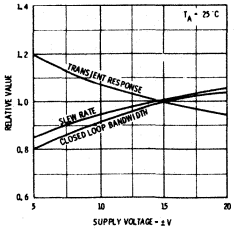
TRANSIENT RESPONSE TEST CIRCUIT



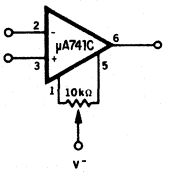
VOLTAGE FOLLOWER LARGE-SIGNAL PULSE RESPONSE



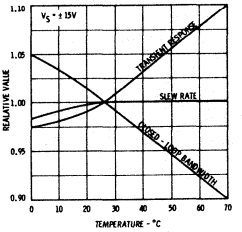
FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE



VOLTAGE OFFSET NULL CIRCUIT



FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE

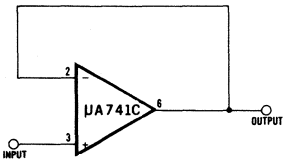


DEFINITION OF TERMS

INPUT OFFSET VOLTAGE — That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.
INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the output at zero volts.
INPUT BIAS CURRENT — The average of the two input currents.
INPUT RESISTANCE — The resistance looking into either input terminal with the other grounded.
INPUT CAPACITANCE — The capacitance looking into either input terminal with the other grounded.
LARGE-SIGNAL VOLTAGE GAIN — The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.
OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.
OUTPUT SHORT-CIRCUIT CURRENT — The maximum output current available from the amplifier with the output shorted to ground or to either supply.
SUPPLY CURRENT — The DC current from the supplies required to operate the amplifier with the output at zero and with no load current.
POWER CONSUMPTION — The DC power required to operate the amplifier with the output at zero and with no load current.
TRANSIENT RESPONSE — The closed-loop step-function response of the amplifier under small-signal conditions.
INPUT VOLTAGE RANGE — The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.
INPUT COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.
SUPPLY VOLTAGE REJECTION RATIO — The ratio of the change in input offset voltage to the change in supply voltage producing it.
OUTPUT VOLTAGE SWING — The peak output swing, referred to zero, that can be obtained without clipping.

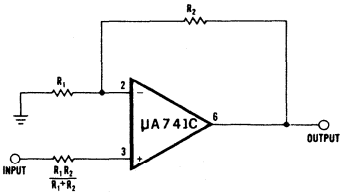
TYPICAL APPLICATIONS

UNITY-GAIN VOLTAGE FOLLOWER



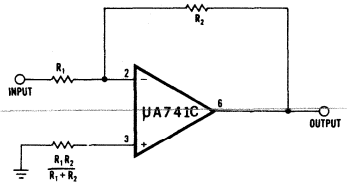
$R_{IN} = 400\ M\Omega$
$C_{IN} = 1\ pF$
$R_{out} << 1\ \Omega$
B.W. = 1 MHz

NON-INVERTING AMPLIFIER



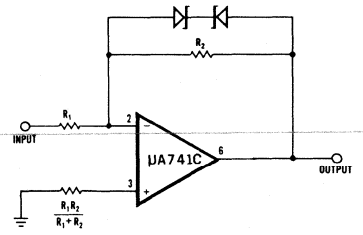
GAIN	R_1	R_2	B.W.	R_{IN}
10	1 kΩ	9 kΩ	100 kHz	400 MΩ
100	100 Ω	9.9 kΩ	10 kHz	280 MΩ
1000	100 Ω	99.9 kΩ	1 kHz	80 MΩ

INVERTING AMPLIFIER



GAIN	R_1	R_2	B.W.	R_{IN}
1	10 kΩ	10 kΩ	1 MHz	10 kΩ
10	1 kΩ	10 kΩ	100 kHz	1 kΩ
100	1 kΩ	100 kΩ	10 kHz	1 kΩ
1000	100 Ω	100 kΩ	1 kHz	100 Ω

CLIPPING AMPLIFIER

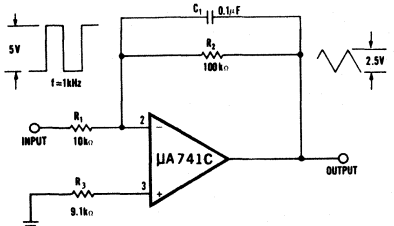


$\frac{E_{out}}{E_{IN}} = \frac{R_2}{R_1}$ if $|E_{out}| \leq V_Z + 0.7\ V$

where V_Z = Zener breakdown voltage

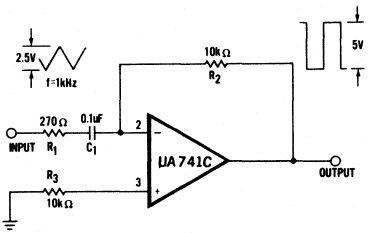
TYPICAL APPLICATIONS

SIMPLE INTEGRATOR



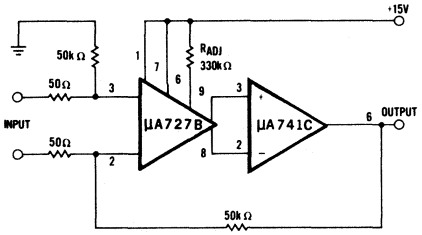
$$E_{out} = -\frac{1}{R_1 C_1}\int E_{IN}dt$$

SIMPLE DIFFERENTIATOR



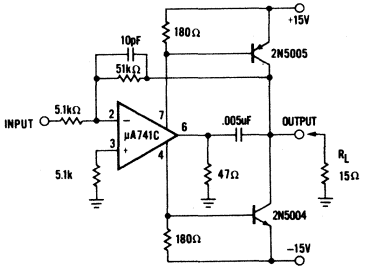
$$E_{out} = -R_2 C_1 \frac{dE_{IN}}{dt}$$

LOW DRIFT LOW NOISE AMPLIFIER

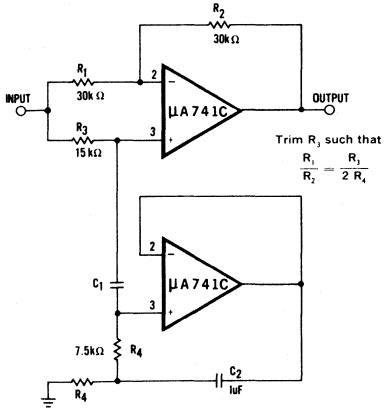


Voltage Gain = 10^3
Input Offset Voltage Drift = 0.6 μV/°C
Input Offset Current Drift = 2.0 pA/°C

HIGH SLEW RATE POWER AMPLIFIER



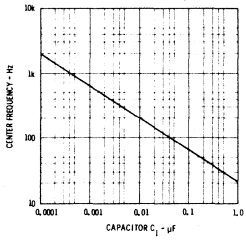
NOTCH FILTER USING THE μA741C AS A GYRATOR



Trim R_3 such that

$$\frac{R_1}{R_2} = \frac{R_3}{2R_4}$$

NOTCH FREQUENCY AS A FUNCTION OF C_1



μA742
ZERO CROSSING AC TRIGGER-TRIGAC
FAIRCHILD LINEAR INTEGRATED CIRCUITS

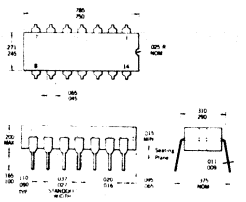
FEATURES
- **DESIGNED FOR APPLICATIONS IN 60 Hz AND 400 Hz AC POWER CONTROL SYSTEMS HAVING RESISTIVE OR INDUCTIVE LOADS**
- **OPERATES DIRECTLY FROM AN AC LINE OR FROM A DC SUPPLY**
- **INPUT COMPATIBLE WITH A WIDE RANGE OF SENSOR IMPEDANCES**
- **BRIDGE SENSING WITH ADJUSTABLE HYSTERESIS SET POINTS**
- **PROVISIONS FOR TIME PROPORTIONING OPERATION**
- **PROVIDES ZERO CROSSING THYRISTOR TRIGGERING FOR MINIMUM RFI**
- **EVEN NUMBER OF CONSECUTIVE HALF-CYCLE TRIGGERING FOR TRIACS AND INVERSE PARALLEL SCR's IN MOST APPLICATIONS**

GENERAL DESCRIPTION — The μA742 is a Zero Crossing AC Trigger - TRIGAC which is constructed on a single chip utilizing the Fairchild Planar* Epitaxial Process. It is intended for use in AC power control circuits for operation directly off the AC line or with a separate AC or DC power supply. The TRIGAC functions as a threshold detector and a driver for triacs and SCR's; as a threshold detector, it senses level changes at the inputs and as a driver it supplies high energy pulses for thyristor triggering. The trigger pulses occur at the zero crossing of the load current and therefore minimize RFI generation for either resistive or inductive loads.

ABSOLUTE MAXIMUM RATINGS

Peak Current into Supply Terminal (AC Operation)	±30 mA
Continuous Current into Supply Terminal (DC Operation)	20 mA
RMS Current into Sync Input Terminal	15 mA
Current into Switch Terminal	10 mA
Power Dissipation	440 mW
Voltage at (+) or (−) Input Terminal	(Note 1)
Differential Voltage between (+) and (−) Input Terminals	±7 V
Current into Clamp Terminal (Clamp ON)	20 mA
Voltage at Clamp Terminal (Clamp OFF)	20 V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 10 second time limit)	260°C
Trigger Output Short-Circuit Duration (Note 2)	Continuous

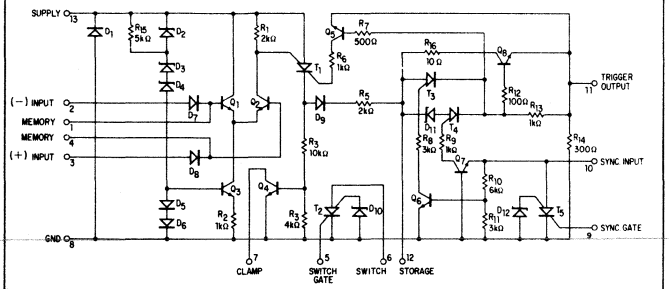
PHYSICAL DIMENSIONS
(Typical Dual In-Line Package)



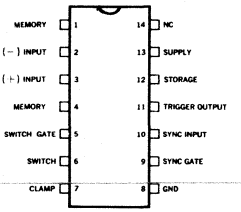
NOTES
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers.
They are purposely shipped with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for .020 inch diameter lead.
Leads are tin-plated kovar
Package weight is 2.0 grams

ORDER PART NO. U6A7742393

EQUIVALENT CIRCUIT



CONNECTION DIAGRAM
(TOP VIEW)



*Planar is a patented Fairchild process.

See notes on Page 2

FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS

(T_A = 25°C, Voltage Range at the (+) and (−) Input Terminals: 0.15 to 0.75·(V_{Supply}); $V_{(+)Input} - V_{(-)Input} \geq 100$ mV, Test Circuit 1, unless otherwise specified.

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Peak Supply Voltage	S_1 in DC position		20		Volts
	S_1 in AC position, positive half cycles of AC line		20		Volts
	S_1 in AC position, negative half cycle of AC line		−0.7		Volts
Peak Trigger Output Pulse	S_1 in AC position, beginning ot positive half cycles		0.9		Amp
	S_1 in AC or DC position, beginning of negative half cycles		1.3		Amp
	S_1 in DC position beginning of positive half cycles		2.2		Amp
Bias Current at (+) and (−) Input Terminals			10		μA
ON Voltage at Clamp Terminal	i_C = 1 mA		0.1		Volts
ON Voltage at Switch Terminal	I_F = 5 mA		1.0		Volts
ON Voltage at Sync Input Terminal	I_F = 10 mA		1.0		Volts
Switching Voltage at Sync Input Terminal			6.0		Volts
Switching Voltage at Switch Terminal			7.0		Volts
Holding Current at Switch Terminal			25		μA
Sync Input Threshold Current for Trigger Output	Beginning of positive half cycles Beginning of negative half cycles		0.3 −0.7		mA mA
Sync Input Threshold Voltage for Trigger Output	Beginning of positive half cycles Beginning of negative half cycles		2.0 −0.7		Volts Volts

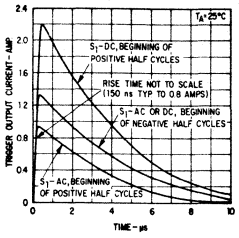
DEFINITIONS

VOLTAGE RANGE: The range of voltage on the (+) or (−) input terminals, which, if exceeded, could cause the TRIGAC to cease functioning.
BIAS CURRENT: The average of the two currents into the (+) and (−) input terminals.

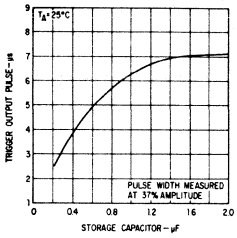
NOTES:
(1) The maximum voltage should not exceed the instantaneous supply voltage of the μA742.
(2) Rating applies for an external storage capacitor having a value of not more than 2μF.

TYPICAL ELECTRICAL CHARACTERISTICS
(TEST CIRCUIT 1 UNLESS OTHERWISE SPECIFIED)

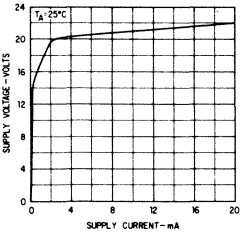
TRIGGER OUTPUT PULSE WAVE FORMS



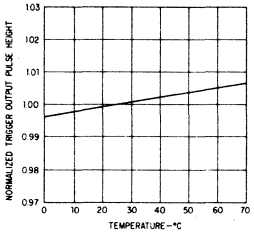
TRIGGER OUTPUT PULSE WIDTH VERSUS STORAGE CAPACITOR



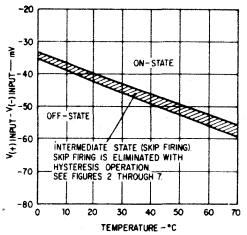
SUPPLY VOLTAGE VERSUS SUPPLY CURRENT



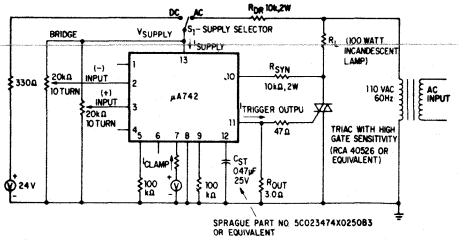
NORMALIZED TRIGGER OUTPUT PULSE HEIGHT VERSUS TEMPERATURE



OPERATING STATE AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE AND TEMPERATURE



μA742 TEST CIRCUIT 1



TYPICAL APPLICATIONS

FIG. 1 — ZERO CROSSING CONTROL CIRCUIT WITHOUT HYSTERESIS

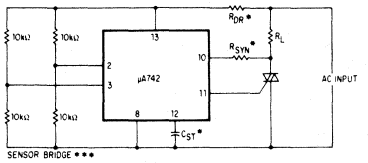


FIG. 2 — ZERO CROSSING CIRCUIT WITH DC SUPPLY

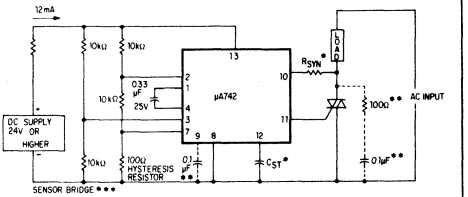


FIG. 3 — ZERO CROSSING CIRCUIT

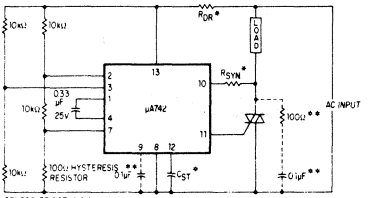


FIG. 4 — SCR FIRING — HALF WAVE

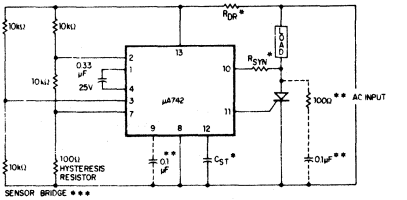


FIG. 5 — INVERSE PARALLEL SCR PAIR FIRING WITH A PULSE TRANSFORMER

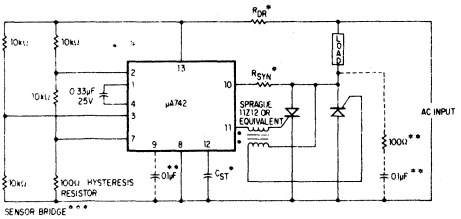


FIG. 6 — INVERSE PARALLEL SCR PAIR FIRING WITH A THIRD SCR

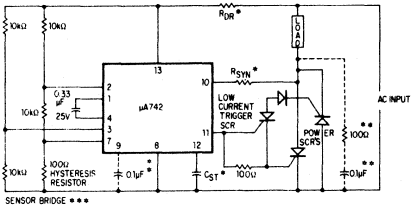
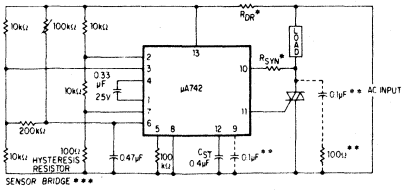


FIG. 7 — ZERO CROSSING WITH PROPORTIONAL CONTROL



*Recommended Values

AC Supply Voltage 60 Hz Volts - RMS	R_{DR}	R_{SYN}	C_{ST}
24	1.0 kΩ	2.2 kΩ	0.47 μF/25 V
110	10 kΩ	10 kΩ	0.47 μF/25 V
220	22 kΩ	22 kΩ	0.47 μF/25 V

FOR SUPPLY VOLTAGE FREQUENCY OF 400 Hz REDUCE C_{ST} TO .047 μF/25 V

**Necessary with inductive loads.

***The sensor resistance will determine the values of the bridge resistors. For the values of R_{DR} shown, the total current into the bridge should not exceed 5 mA at 20 V.

μA744

RADIATION RESISTANT OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

FEATURES

- **OPERATION AFTER TRANSIENT IONIZATION TO ABOVE 5 x 10^{10} rad/sec**
- **OPERATION AFTER CUMULATIVE DOSE TO ABOVE 10^{14} NEUTRONS/cm^2**
- **OPERATION DURING IONIZING RADIATION TO ABOVE 5 x 10^{6} rad/sec**
- **SHORT CIRCUIT PROTECTION**
- **NO LATCH UP**
- **LARGE COMMON MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **LOW POWER CONSUMPTION**

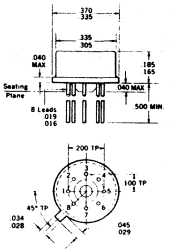
GENERAL DESCRIPTION — The μA744 is a radiation-resistant operational amplifier constructed on a single silicon chip using Fairchild Planar* epitaxial process. The device is designed specifically for operation in radiation environments including fast neutrons, X-rays and gamma-rays. Individual active components are separated by dielectric isolation and compatible thin film resistors are used throughout the design. Photocurrent compensation diodes improve performance during ionization and advanced surface passivation techniques substantially reduce leakages after irradiation. These processing methods allow circuit operation under moderate ionizing radiation and provide protection during intense ionizing pulses. In addition, the μA744 has the usual features such as low input offset, high gain, high input impedance, large input common mode range, high output swing, absence of "latch-up", and short circuit protection. The device displays excellent temperature stability, will operate over a wide range of supply voltages and is pin compatible with the popular μA741 operational amplifier. The μA744 is useful in AC servo systems, analog computers, instrumentation amplifiers and other general feedback applications requiring operation during and after exposure to radiation environments.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±1.8V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage (Note 2)	±30 V
Input Voltage (Note 3)	±15 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 60 seconds)	300°C
Output Short Circuit Duration (T_A = 25°C)	Indefinite

PHYSICAL DIMENSIONS

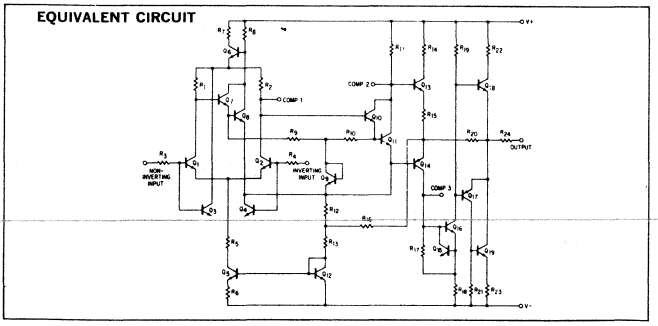
In accordance with JEDEC (TO-99) outline



NOTES:
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.22 grams

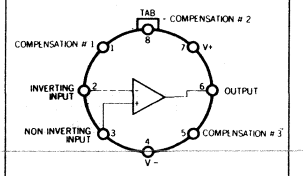
ORDER PART NO. U5B7744312

EQUIVALENT CIRCUIT



CONNECTION DIAGRAM

(TOP VIEW)



NOTE: Pin 4 connected to case

Notes on Page 2

*Planar is a patented Fairchild process.

SPECIAL ORDER

FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V_S = \pm 15$ V, unless otherwise specified)

PARAMETER (Note 4)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ, ± 9 V $\leq V_S \leq \pm 15$ V		2.0		mV
Input Offset Current			100		nA
Input Bias Current			0.3		μA
Input Resistance			250		kΩ
Output Resistance			150		Ω
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V		45,000		
Output Voltage Swing	$R_L \geq 10$ kΩ		±14		V
	$R_L \geq 2$ kΩ		±13		V
Input Voltage Range			±10		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ		90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		25		μV/V
Power Consumption			80		mW
Transient Response	$V_{in} = 20$ mV, $R_L = 2$ kΩ				
Risetime	$C_1 = 5000$ pF, $R_1 = 1.5$ kΩ, $C_2 = 200$ pF, $R_2 = 50$ Ω		0.3		μs
Overshoot	$C_L \leq 100$ pF		10		%

NOTES:
(1) Rating applies for case temperatures to +125°C; derate linearly at 6.5 mW/°C for ambient temperatures above +75°C.
(2) Rating applies for pulses of 10 ms duration with 10% duty cycle; derate to ±5V for continuous operation.
(3) For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
(4) For details on post-irradiation performance contact Security Officer, Fairchild Semiconductor, 464 Ellis St., Mountain View, California 94040.

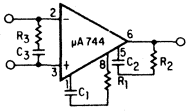
TABLE 1
STANDARD FREQUENCY COMPENSATION
($R_2 = 0$, R_3 = Open, $C_3 = 0$, $R_S = 10$ kΩ)

CLOSED LOOP GAIN	R_1	C_1	C_2	SLEW RATE
1,000	0	10 pF	3 pF	20 V/μs
100	1.5 kΩ	100 pF	3 pF	12 V/μs
10	1.5 kΩ	500 pF	20 pF	4.0 V/μs
1	1.5 kΩ	5,000 pF	200 pF	0.4 V/μs

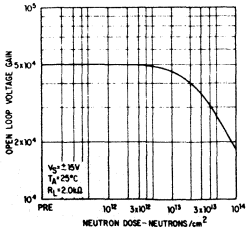
TABLE 2
HIGH SLEW RATE, HIGH POWER BANDWIDTH, UNITY GAIN FREQUENCY COMPENSATION
($R_S = 10$ k)

TYPE	R_1	C_1	R_2	C_2	R_3	C_3	SLEW RATE
Standard	1.5 kΩ	5,000 pF	0	200 pF	Open	0	0.4 V/μs
Input Lag	0	10 pF	0	3 pF	39 Ω	.47 μF	20 V/μs
Intermediate	1.5 kΩ	250 pF	0	10 pF	1.0 kΩ	.47 μF	6.0 V/μs
40 dB/decade	1.5 kΩ	250 pF	1.8 kΩ	10 pF	Open	0	5.0 V/μs

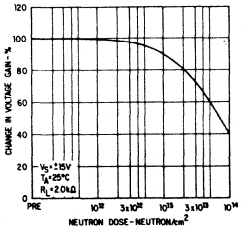
FREQUENCY COMPENSATION CIRCUIT



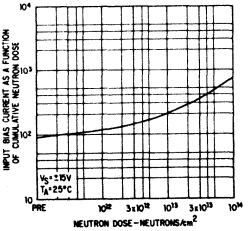
OPEN LOOP GAIN AS A FUNCTION OF CUMULATIVE NEUTRON DOSE



CHANGE IN VOLTAGE GAIN AS A FUNCTION OF CUMULATIVE NEUTRON DOSE



INPUT BIAS CURRENT AS A FUNCTION OF CUMULATIVE NEUTRON DOSE



μA745
DUAL AC AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

FEATURES

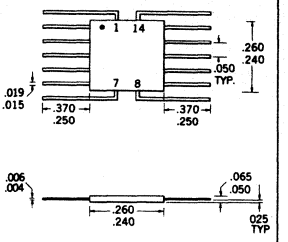
- **LOW DISTORTION . . . . . 0.5% TYPICAL**
- **BUILT-IN ZENER**
- **OUTPUT TRANSISTOR FLEXIBILITY . . . ALL THREE LEADS AVAILABLE**
- **COMPENSATION FLEXIBILITY**

GENERAL DESCRIPTION — The μA745 is a dual three-stage cascaded direct coupled amplifier constructed on a single silicon chip using the Fairchild Planar* epitaxial process. The μA745 is useful for application in active filters, audio oscillators, low distortion AC amplifiers, and special functions or waveform generation.

ABSOLUTE MAXIMUM RATINGS (Note 1)

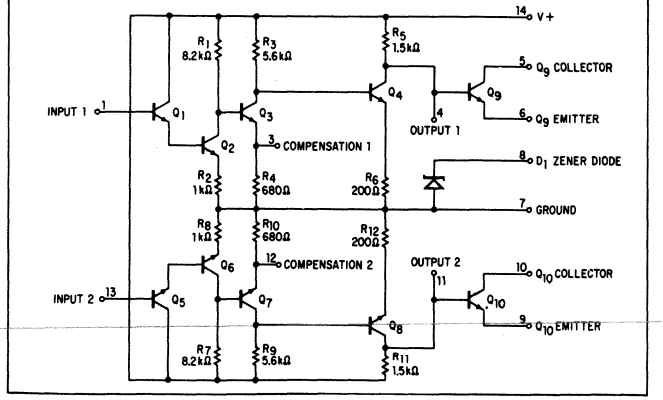
Internal Power Dissipation	300 mW
Amplifier Supply Voltage	8.0 V
V_{CE} of Q_9 and Q_{10}	25 V
D1 Zener Current	5.0 mA
Storage Temperature Range	−65° to +200°C
Operating Temperature Range	−40°C to +60°C
Lead Temperature (Soldering, 60 seconds)	300°C

PHYSICAL DIMENSIONS
in accordance with JEDEC (TO-86) outline
14-LEAD CERPAK

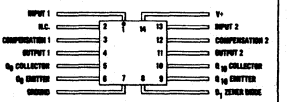


NOTE: All dimensions in inches
ORDER PART NO. U3I7745343

EQUIVALENT CIRCUIT



CONNECTION DIAGRAM
(TOP VIEW)



NOTE:
(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

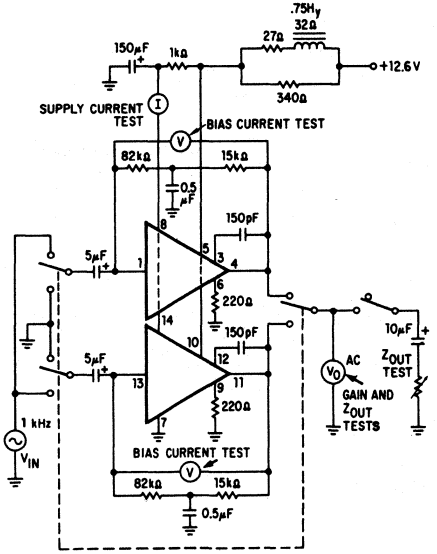
*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR

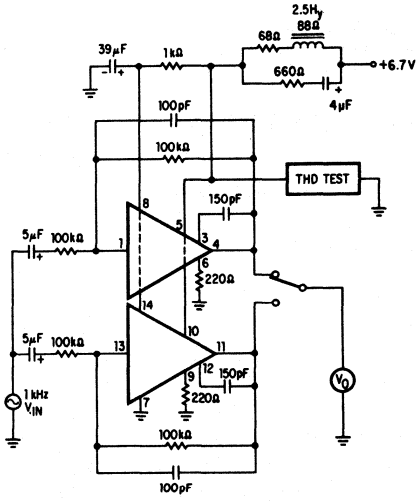
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

PARAMETER	CONDITIONS	TYP.	UNITS
Amplifier Gain	Test Circuit 1 $V_{I, I3}$ = 1.0 mV rms	46	dB
Amplifier Total Harmonic Distortion	Test Circuit 2 V_O = 1.2 V p-p	0.5	%
Amplifier Output Impedance	Test Circuit 1	1.3	kΩ
Input Bias Current	Test Circuit 1 V_{IN} = 0	100	nA
Amplifier Supply Current	Test Circuit 1 V_{IN} = 0	6.5	mA
h_{FE} of Q_9 & Q_{10}	I_C = 2 mA, V_{CE} = 5 V	100	
BV_{CEO} of Q_9 & Q_{10}	I_C = 1 mA	35	Volts
I_{CES} of Q_9 & Q_{10}	V_{CE} = 15 V	1.0	nA
D1 Zener Voltage	I_Z = 1 mA	6.3	Volts

TEST CIRCUIT 1



TEST CIRCUIT 2



μA746
COLOR TV CHROMA DEMODULATOR
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA746 is a color TV chroma demodulator constructed on a single silicon chip using the Fairchild Planar* epitaxial process. This device demodulates the chroma subcarrier information contained in a color television video signal and provides color-difference signals at the outputs. The low voltage drift of the D.C. output insures excellent performance in direct-coupled chrominance output circuitry. For μA746 applications information, and other Fairchild communications integrated circuits, see listing on last page.

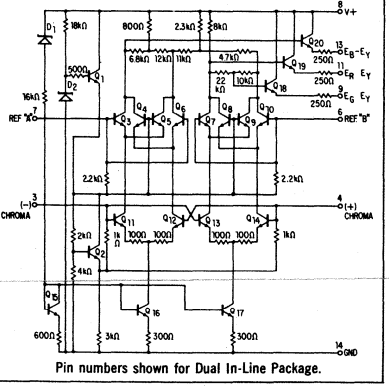
FEATURES

- **LOW OUTPUT VOLTAGE DRIFT WITH TEMPERATURE**
- **DOUBLY BALANCED DEMODULATION**
- **INTERNAL COLOR-DIFFERENCE MATRIX FOR NTSC COLOR TV**
- **10 VOLT PEAK-TO-PEAK E_B - E_Y OUTPUT**

ABSOLUTE MAXIMUM RATINGS

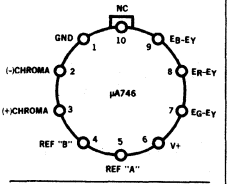
Supply Voltage	+28 V
Minimum Load Resistance	3 kΩ
Peak-to-Peak Reference Input Voltage	5.0 V
Peak-to-Peak Chroma Input Voltage	5.0 V
Internal Power Dissipation	450 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	
(5E and 6A Packages)	−65°C to +150°C
(9A Package)	−55°C to +125°C
Lead Temperature (Soldering, 10 seconds)	
(5E and 6A Packages)	+300°C
(9A Package)	+260°C

EQUIVALENT CIRCUIT

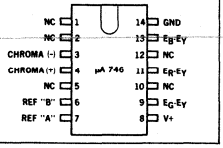


Pin numbers shown for Dual In-Line Package.

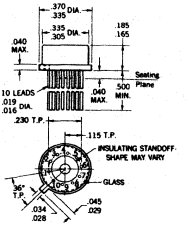
CONNECTION DIAGRAMS
(TOP VIEWS)
METAL CAN



DIP

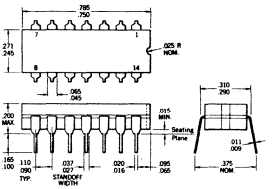


PHYSICAL DIMENSIONS

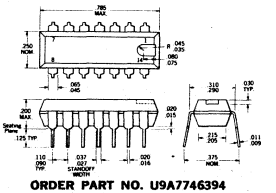


NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.32 grams

ORDER PART NO. U5E7746394



ORDER PART NO. U6A7746394



ORDER PART NO. U9A7746394

NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Package weight is 2.0 grams for 6A, 0.9 gram for 9A.

*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V^+ = 24$ V, Test Circuit 1 unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current	$e_C = 0$, $R_L = 1$ MΩ	5.5	9.0	12.5	mA
	$e_C = 0$, $R_L = 1$ MΩ, $T_A = 70°C$		9.0	13.0	mA
	$e_C = 0$	16.5	22	25.5	mA
	$e_C = 0$, $T_A = 70°C$		22		mA
Internal Power Dissipation	$e_C = 0$		340	430	mW
	$e_C = 0$, $T_A = 70°C$		340	445	mW
DC Voltage at any Output Terminal	$e_C = 0$	13.2	14.5	15.8	Volts
	$e_C = 0$, $T_A = 70°C$	13.0	14.5	16.0	Volts
Temperature Coefficient of DC Voltage at any Output Terminal	$e_C = 0$	−5.0	−0.3	+5.0	mV/°C
Absolute Value of DC Difference Voltage between any Two Outputs	$e_C = 0$		0.15	0.6	Volts
DC Voltage at either Reference Terminal	$e_A = e_B = e_C = 0$		5.8		Volts
DC Voltage at either Chroma Terminal	$e_C = 0$		3.2		Volts
Reference Input Resistance	$e_C = 0$		1.7		kΩ
Reference Input Capacitance	$e_C = 0$		6.0		pF
Chroma Input Resistance			0.8		kΩ
Chroma Input Capacitance			5.0		pF
Peak-to-Peak Chroma Input Voltage	$E_B - E_Y = 5$ Vp-p		0.4	0.7	Volts
Peak-to-Peak $E_R - E_Y$ Output Voltage	$E_B - E_Y = 5$ Vp-p	3.5	3.8	4.2	Volts
Peak-to-Peak $E_G - E_Y$ Output Voltage	$E_B - E_Y = 5$ Vp-p	0.75	1.0	1.25	Volts
Maximum Peak-to-Peak $E_B - E_Y$ Output Voltage	$e_C = 1.5$ Vp-p	8.0	10		Volts
$E_B - E_Y$ Demodulation Angle	$E_B - E_Y = 5$ Vp-p		3		Degrees
$E_R - E_Y$ Demodulation Angle	$E_B - E_Y = 5$ Vp-p		109		Degrees
$E_G - E_Y$ Demodulation Angle	$E_B - E_Y = 5$ Vp-p		259		Degrees
$E_R - E_Y$ Demodulation Angle relative to $E_B - E_Y$ Demodulation Angle	$E_B - E_Y = 5$ Vp-p	101	106	111	Degrees
$E_B - E_Y$ Demodulation Angle relative to $E_G - E_Y$ Demodulation Angle	$E_B - E_Y = 5$ Vp-p	96	104	112	Degrees
Highest Peak-to-Peak Demodulator AC Unbalance Voltage at any Output Terminal	$e_C = 0$		0.3	0.8	Volts

DEFINITIONS

Color-Difference Demodulation Angle — A color-difference demodulation angle is defined as the instantaneous phase of the (+) Chroma input signal which produces the most positive voltage at the respective color-difference output with the phase of Reference "A" taken at 3 degrees and the phase of Reference "B" taken at 106 degrees.

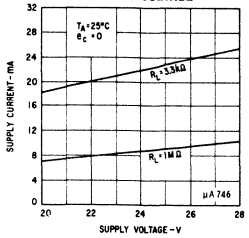
(+) Chroma Input — A composite chroma signal containing the burst at a phase of 180 degrees is demodulated to produce specified color-difference demodulation angles when applied to the (+) Chroma input.

(—) Chroma Input — A composite chroma signal containing the burst at a phase of 0 degrees is demodulated to produce specified color-difference demodulation angles when applied to the (—) Chroma input.

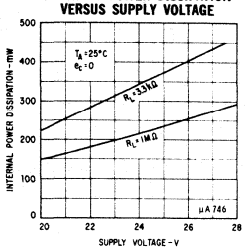
TYPICAL ELECTRICAL CHARACTERISTICS

(TEST CIRCUIT 1 UNLESS OTHERWISE SPECIFIED)

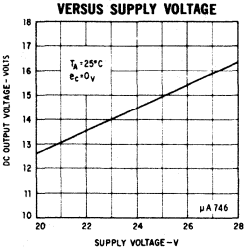
SUPPLY CURRENT VERSUS SUPPLY VOLTAGE



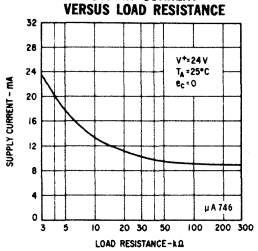
INTERNAL POWER DISSIPATION VERSUS SUPPLY VOLTAGE



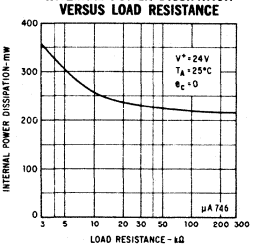
DC VOLTAGE AT ANY OUTPUT VERSUS SUPPLY VOLTAGE



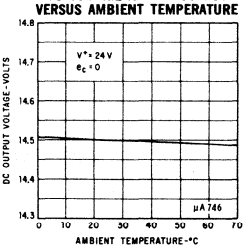
SUPPLY CURRENT VERSUS LOAD RESISTANCE



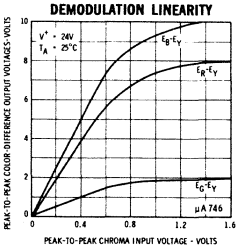
INTERNAL POWER DISSIPATION VERSUS LOAD RESISTANCE



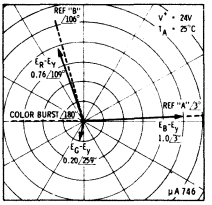
DC VOLTAGE AT ANY OUTPUT VERSUS AMBIENT TEMPERATURE



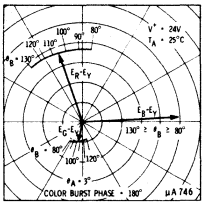
DEMODULATION LINEARITY



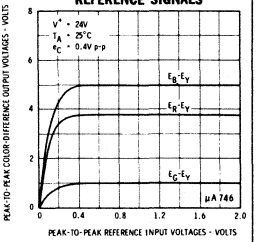
DEMODULATION ANGLES AND RELATIVE GAINS



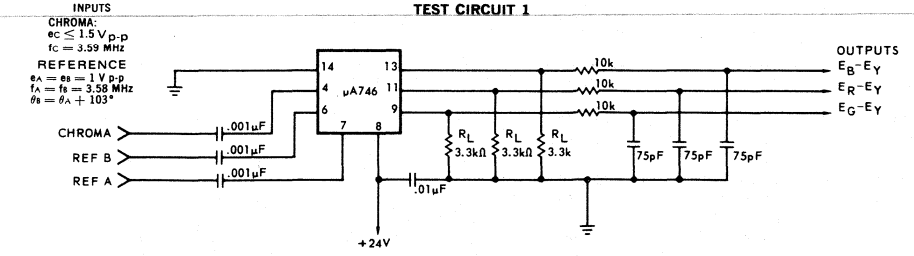
DEMODULATION SENSITIVITY TO RELATIVE PHASING OF REFERENCE SIGNALS



DEMODULATION SENSITIVITY TO AMPLITUDE OF REFERENCE SIGNALS



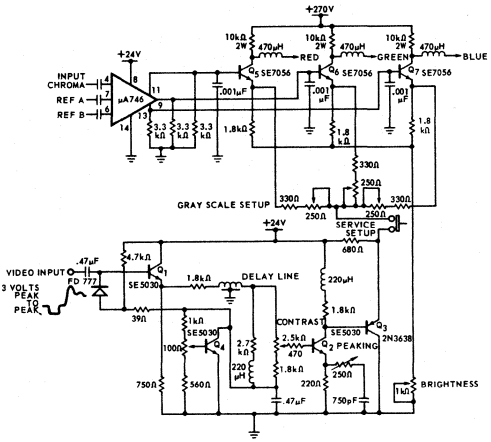
TEST CIRCUIT 1



Pin numbers shown for Dual In-Line Package.

TYPICAL APPLICATION

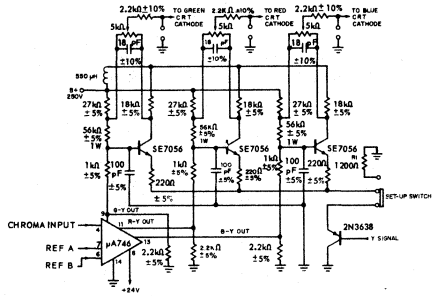
COMPLETE R-G-B VIDEO OUTPUT STAGE



PIN NUMBER SHOWN FOR DUAL-IN-LINE PACKAGE

Fully D.C. coupled circuit exhibits negligible drift with temperature, eliminates interaction between contrast and brightness controls, and minimizes gray-scale set-up time. For further applications information, see Application Brief 104.

COMPLETE R-G-B VIDEO OUTPUT STAGE



Pin numbers shown for Dual In-Line Package.

From:

"A Semiconductor Video Output Amplifier for a Red Blue Green Large Screen Color Television Receiver", by D. Poppy. IEEE Transactions on Broadcast and Television Receivers, BTR-15, #2, pp. 167-70, July 1969.

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μA746 APPLICATIONS INFORMATION

TP 48	— A Monolithic Chroma Demodulator IC for Color TV Receivers	APP BRIEF 124	— The μA746 Color TV Chroma Demodulator IC
APP BRIEF 104	— Black Level Considerations in High Quality Color TV Receivers	APP BRIEF 105	— Uses and Abuses of the Chroma Demodulator

For information on other Fairchild Communications Integrated Circuits, see the following data sheets:

RF/IF Limiting Amp — μA703C
RF/IF Limiting Amp — μA703D
Fixed Gain, Low Distortion Amp — μA716C
High Frequency Communications System — μA719C
FM Stereo Multiplex Decoder — μA729
FM Stereo Multiplex Decoder — μA732, μA767
Dual Low Noise, High Gain Op-Amp — μA739C
Dual AC Amp — μA745
Dual Operational Amplifier — μA749D
TV/FM Sound System — μA754C, μA3065
Gain Controlled IF Amp — μA757C
Balanced Modulator-Demodulator — μA796C

μA747
DUAL FREQUENCY COMPENSATED OPERATIONAL AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

FEATURES:
- **NO FREQUENCY COMPENSATION REQUIRED**
- **SHORT-CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **LOW POWER CONSUMPTION**
- **NO LATCH UP**

GENERAL DESCRIPTION — The μA747 is a pair of high performance monolithic operational amplifiers constructed on a single silicon chip, using the Fairchild Planar* epitaxial process. They are intended for a wide range of analog applications where board space or weight are important. High common mode voltage range and absence of "latch-up" make the μA747 ideal for use as a voltage follower. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier, and general feedback applications. The μA747 is short-circuit protected and requires no external components for frequency compensation. The internal 6dB/octave roll-off insures stability in closed loop applications. For single amplifier performance, see μA741 data sheet.

ABSOLUTE MAXIMUM RATINGS

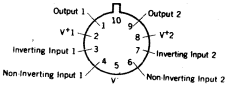
Supply Voltage	±22 V
Internal Power Dissipation (Note 1)	800 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Voltage between Offset Null and V−	±0.5 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 60 second)	300°C
Output Short-Circuit Duration (Note 3)	Indefinite

PHYSICAL DIMENSIONS

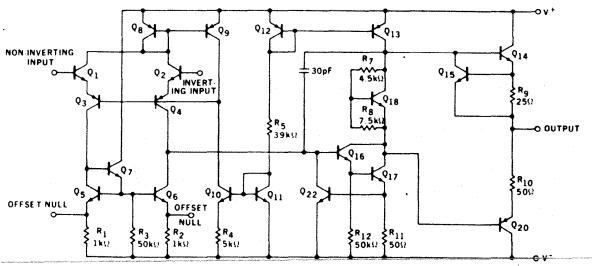
T05 (TO99)
ORDER PART NO. U5F7747312

DIL (T0116) CERAMIC
ORDER PART NO. U7A7747312

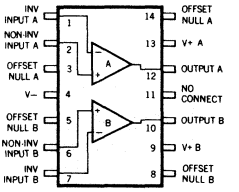
T05 PINNING DIAGRAM



EQUIVALENT CIRCUIT—EACH SIDE



CONNECTION DIAGRAM
(Top View)



NOTES:
(1) Rating applies for case temperatures to 125°C; derate linearly at 9.0 mW/°C for ambient temperatures above +60°C.
(2) For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
(3) Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +60°C ambient temperature for each side.

*Planar is a patented Fairchild process.

FAIRCHILD SEMICONDUCTOR

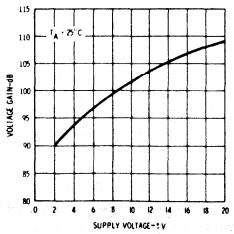
ELECTRICAL CHARACTERISTICS — Each Amplifier ($V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified)

PARAMETERS (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	5.0	mV
Input Offset Current			20	200	nA
Input Bias Current			80	500	nA
Input Resistance		0.3	2.0		MΩ
Input Capacitance			1.4		pF
Offset Voltage Adjustment Range			±15		mV
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	50,000	200,000		
Output Resistance			75		Ω
Output Short-Circuit Current			25		mA
Supply Current			1.7	2.8	mA
Power Consumption			50	85	mW
Transient Response (unity gain)	$V_{in} = 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF				
Risetime			0.3		μs
Overshoot			5.0		%
Slew Rate	$R_L \geq 2$ kΩ		0.5		V/μs
Channel Separation			120		dB
The following specifications apply for $-55°C \leq T_A \leq +125°C$.					
Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	6.0	mV
Input Offset Current	$T_A = +125°C$		7.0	200	nA
	$T_A = -55°C$		85	500	nA
Input Bias Current	$T_A = +125°C$		0.03	0.5	μA
	$T_A = -55°C$		0.3	1.5	μA
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150	μV/V
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	25,000			
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		V
Supply Current	$T_A = +125°C$		1.5	2.5	mA
	$T_A = -55°C$		2.0	3.3	mA
Power Consumption	$T_A = +125°C$		45	75	mW
	$T_A = -55°C$		60	100	mW

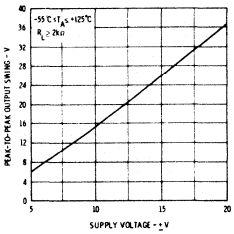
TYPICAL PERFORMANCE CURVES (Each Amplifier)

TYPICAL PERFORMANCE CURVES

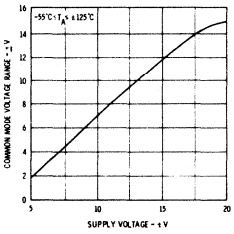
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE

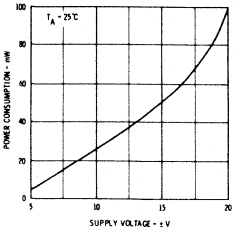


INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

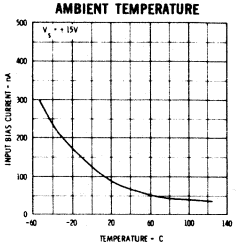


TYPICAL PERFORMANCE CURVES (Each Amplifier)

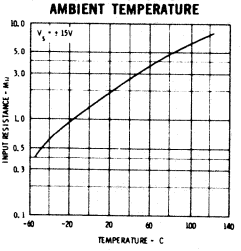
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



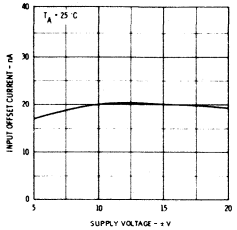
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



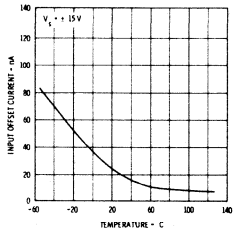
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



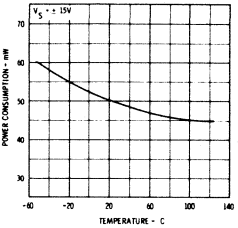
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



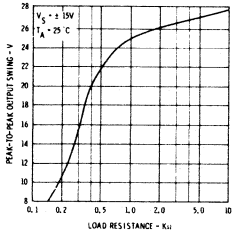
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



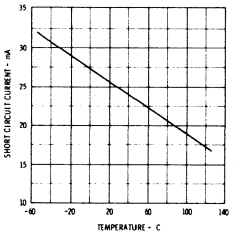
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



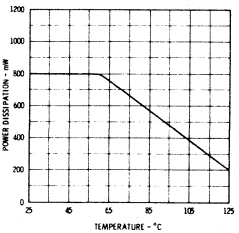
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



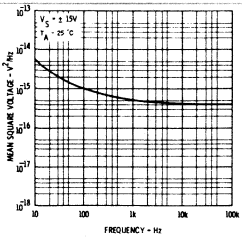
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



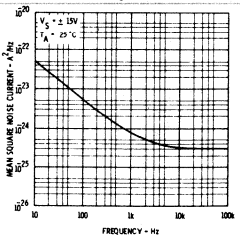
ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



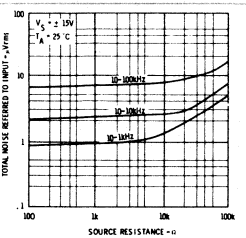
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY

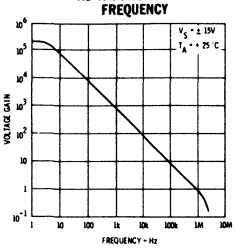


BROADBAND NOISE FOR VARIOUS BANDWIDTHS

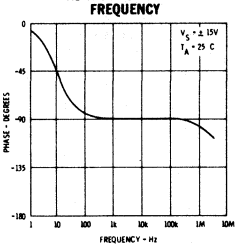


TYPICAL PERFORMANCE CURVES (Each Amplifier)

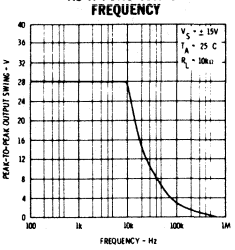
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



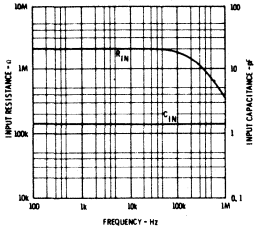
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



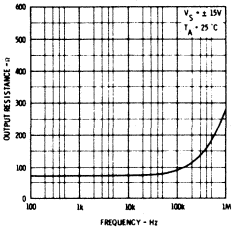
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



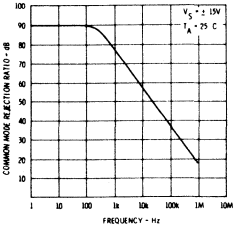
INPUT RESISTANCE AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY



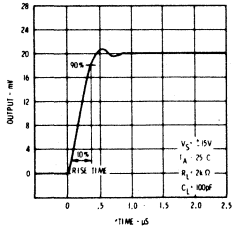
OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY



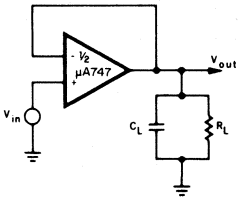
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



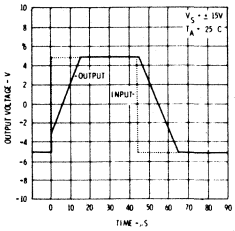
TRANSIENT RESPONSE



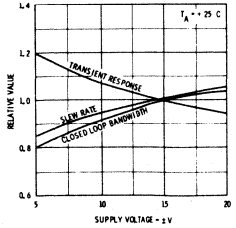
TRANSIENT RESPONSE TEST CIRCUIT



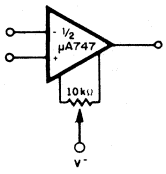
VOLTAGE FOLLOWER LARGE-SIGNAL PULSE RESPONSE



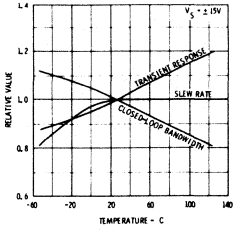
FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE



VOLTAGE OFFSET NULL CIRCUIT



FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE

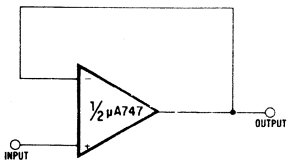


DEFINITION OF TERMS

INPUT OFFSET VOLTAGE — That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.
INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the output at zero volts.
INPUT BIAS CURRENT — The average of the two input currents.
INPUT RESISTANCE — The resistance looking into either input terminal with the other grounded.
INPUT CAPACITANCE — The capacitance looking into either input terminal with the other grounded.
LARGE-SIGNAL VOLTAGE GAIN — The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.
OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.
OUTPUT SHORT-CIRCUIT CURRENT — The maximum output current available from the amplifier with the output shorted to ground or to either supply.
SUPPLY CURRENT — The DC current from the supplies required to operate the amplifier with the output at zero and with no load current.
POWER CONSUMPTION — The DC power required to operate the amplifier with the output at zero and with no load current.
TRANSIENT RESPONSE — The closed-loop step-function response of the amplifier under small-signal conditions.
INPUT VOLTAGE RANGE — The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.
INPUT COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.
SUPPLY VOLTAGE REJECTION RATIO — The ratio of the change in input voltage to the change in supply voltage producing it.
OUTPUT VOLTAGE SWING — The peak output swing, referred to zero, that can be obtained without clipping.

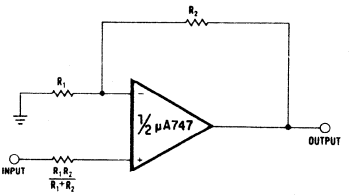
TYPICAL APPLICATIONS

UNITY-GAIN VOLTAGE FOLLOWER



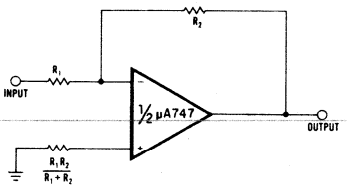
$R_{IN} = 400\ M\Omega$
$C_{IN} = 1\ pF$
$R_{out} << 1\ \Omega$
B.W. = 1 MHz

NON-INVERTING AMPLIFIER



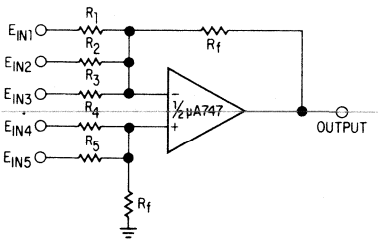
GAIN	R_1	R_2	B.W.	R_{IN}
10	1 kΩ	9 kΩ	100 kHz	400 MΩ
100	100 Ω	9.9 kΩ	10 kHz	280 MΩ
1000	100 Ω	99.9 kΩ	1 kHz	80 MΩ

INVERTING AMPLIFIER



GAIN	R_1	R_2	B.W.	R_{IN}
1	10 kΩ	10 kΩ	1 MHz	10 kΩ
10	1 kΩ	10 kΩ	100 kHz	1 kΩ
100	1 kΩ	100 kΩ	10 kHz	1 kΩ
1000	100 Ω	100 kΩ	1 kHz	100 Ω

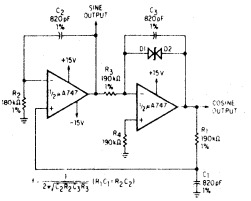
WEIGHTED AVERAGING AMPLIFIER



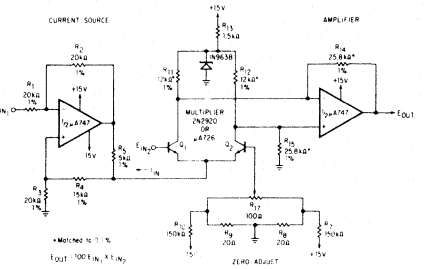
$$-E_{out} = E_{IN1}\left(\frac{R_f}{R_1}\right) + E_{IN2}\left(\frac{R_f}{R_2}\right) + E_{IN3}\left(\frac{R_f}{R_3}\right) - E_{IN4}\left(\frac{R_f}{R_4}\right) - E_{IN5}\left(\frac{R_f}{R_5}\right)$$

TYPICAL APPLICATIONS

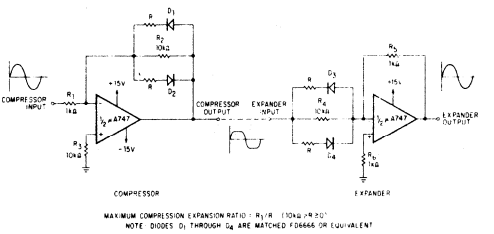
QUADRATURE OSCILLATOR



ANALOG MULTIPLIER



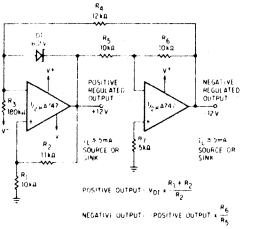
COMPRESSOR/EXPANDER AMPLIFIERS



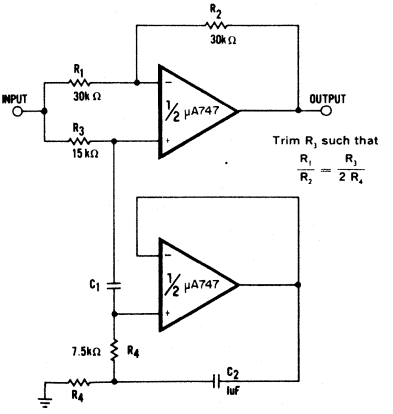
MAXIMUM COMPRESSION EXPANSION RATIO = R_1/R (10kΩ/R ≥ 1Ω)

NOTE: DIODES D_1 THROUGH D_4 ARE MATCHED FD6666 OR EQUIVALENT

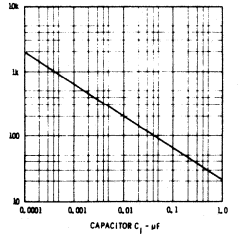
TRACKING POSITIVE AND NEGATIVE VOLTAGE REFERENCES



NOTCH FILTER USING THE μA747 AS A GYRATOR



NOTCH FREQUENCY AS A FUNCTION OF C_1



μA747C
DUAL FREQUENCY COMPENSATED OPERATIONAL AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

FEATURES:
- **NO FREQUENCY COMPENSATION REQUIRED**
- **SHORT-CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **LOW POWER CONSUMPTION**
- **NO LATCH UP**

GENERAL DESCRIPTION — The μA747C is a pair of high performance monolithic operational amplifiers constructed on a single silicon chip, using the Fairchild Planar* epitaxial process. They are intended for a wide range of analog applications where board space or weight are important. High common mode voltage range and absence of "latch-up" make the μA747C ideal for use as a voltage follower. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier, and general feedback applications. The μA747C is short-circuit protected and requires no external components for frequency compensation. The internal 6dB/octave roll-off insures stability in closed loop applications. For single amplifier performance, see μA741C data sheet. For full temperature range operation (−55°C to +125°C), see μA747 data sheet.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18 V
Internal Power Dissipation (Note 1)	800 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Voltage between Offset Null and V−	±0.5 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 60 second)	300°C
Output Short-Circuit Duration (Note 3)	Indefinite

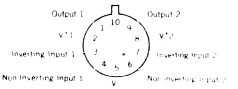
PHYSICAL DIMENSIONS

T05 (T099)

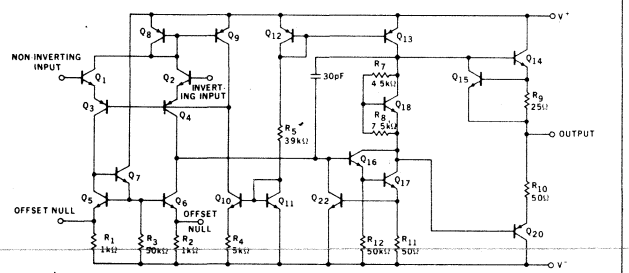
ORDER PART NO. U5F7747393

DIL (T0116) CERAMIC
ORDER PART NO. U7A7747393

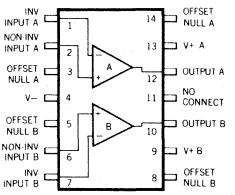
T05 PINNING DIAGRAM



EQUIVALENT CIRCUIT— EACH SIDE



CONNECTION DIAGRAM
(Top View)



NOTES:
(1) Rating applies for case temperatures to +70°C; derate linearly at 9.0 mW/°C for ambient temperatures above +60°C.
(2) For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
(3) Short circuit may be to ground or either supply. Rating applies to +70°C case temperature or +60°C ambient temperature for each side.

*Planar is a patented Fairchild process.

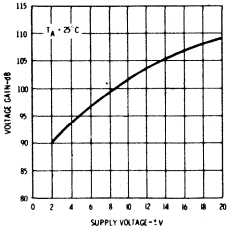
FAIRCHILD SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS — Each Amplifier ($V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified)

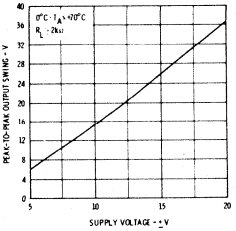
PARAMETERS (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	6.0	mV
Input Offset Current			20	200	nA
Input Bias Current			80	500	nA
Input Resistance		0.3	2.0		MΩ
Input Capacitance			1.4		pF
Offset Voltage Adjustment Range			±15		mV
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	25,000	200,000		
Output Resistance			75		Ω
Output Short-Circuit Current			25		mA
Supply Current			1.7	2.8	mA
Power Consumption			50	85	mW
Transient Response (unity gain)	$V_{in} = 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF				
Risetime			0.3		μs
Overshoot			5.0		%
Slew Rate	$R_L \geq 2$ kΩ		0.5		V/μs
Channel Separation			120		dB
The following specifications apply for $0°C \leq T_A \leq +70°C$.					
Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	7.5	mV
Input Offset Current			7.0	300	nA
Input Bias Current			0.03	0.8	μA
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150	μV/V
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	15,000			
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		V
Supply Current			2.0	3.3	mA
Power Consumption			60	100	mW

TYPICAL PERFORMANCE CURVES (Each Amplifier)

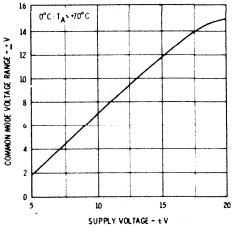
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE

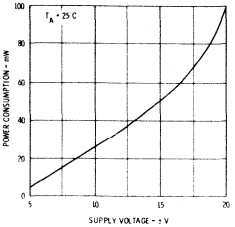


INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

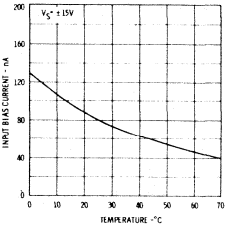


TYPICAL PERFORMANCE CURVES (Each Amplifier)

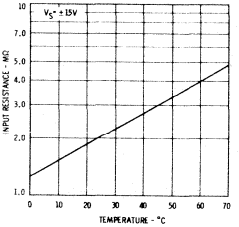
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



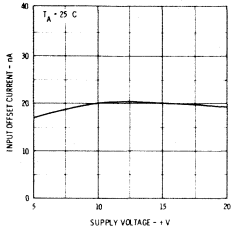
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



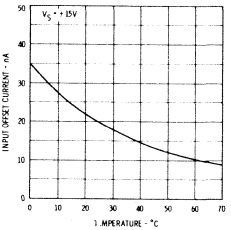
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



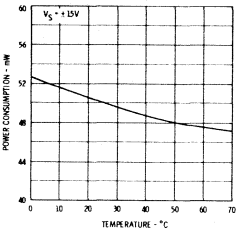
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



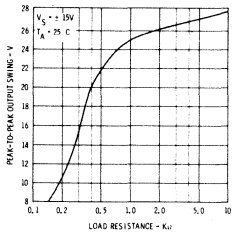
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



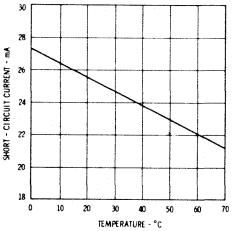
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



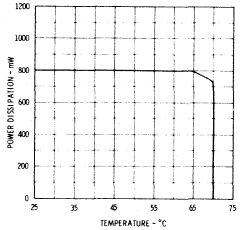
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



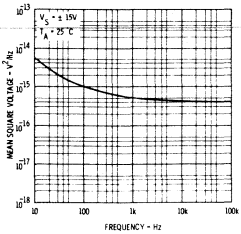
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



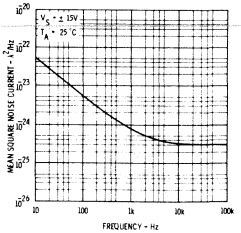
ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



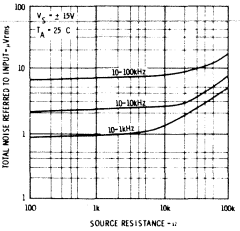
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY

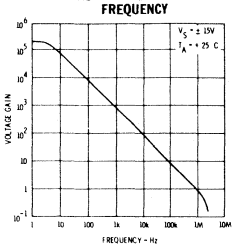


BROADBAND NOISE FOR VARIOUS BANDWIDTHS

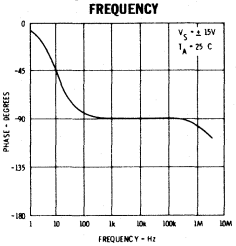


TYPICAL PERFORMANCE CURVES (Each Amplifier)

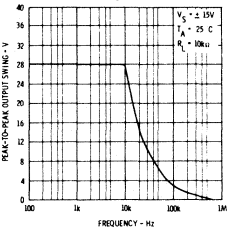
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



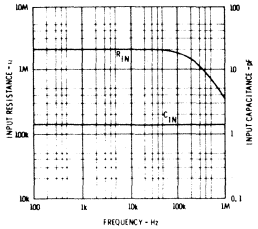
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



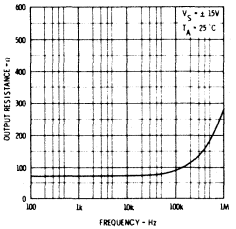
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



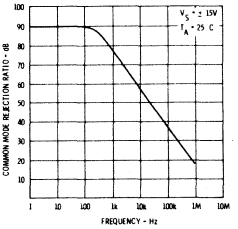
INPUT RESISTANCE AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY



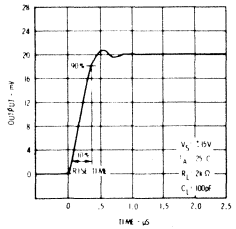
OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY



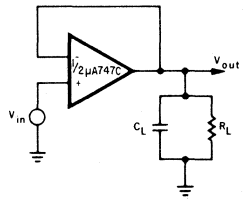
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



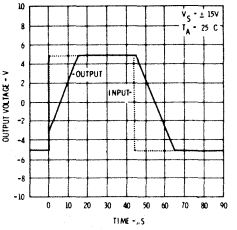
TRANSIENT RESPONSE



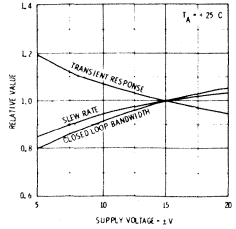
TRANSIENT RESPONSE TEST CIRCUIT



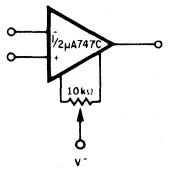
VOLTAGE FOLLOWER LARGE-SIGNAL PULSE RESPONSE



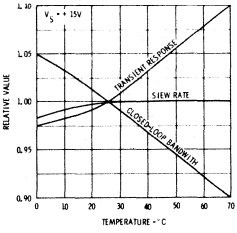
FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE



VOLTAGE OFFSET NULL CIRCUIT



FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE

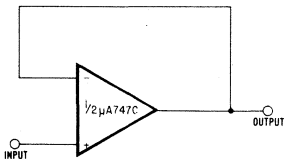


DEFINITION OF TERMS

INPUT OFFSET VOLTAGE — That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.
INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the output at zero volts.
INPUT BIAS CURRENT — The average of the two input currents.
INPUT RESISTANCE — The resistance looking into either input terminal with the other grounded.
INPUT CAPACITANCE — The capacitance looking into either input terminal with the other grounded.
LARGE-SIGNAL VOLTAGE GAIN — The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.
OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.
OUTPUT SHORT-CIRCUIT CURRENT — The maximum output current available from the amplifier with the output shorted to ground or to either supply.
SUPPLY CURRENT — The DC current from the supplies required to operate the amplifier with the output at zero and with no load current.
POWER CONSUMPTION — The DC power required to operate the amplifier with the output at zero and with no load current.
TRANSIENT RESPONSE — The closed-loop step-function response of the amplifier under small-signal conditions.
INPUT VOLTAGE RANGE — The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.
INPUT COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.
SUPPLY VOLTAGE REJECTION RATIO — The ratio of the change in input voltage to the change in supply voltage producing it.
OUTPUT VOLTAGE SWING — The peak output swing, referred to zero, that can be obtained without clipping.

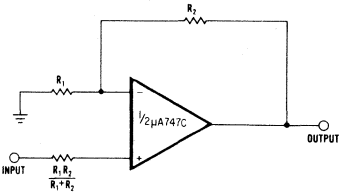
TYPICAL APPLICATIONS

UNITY-GAIN VOLTAGE FOLLOWER



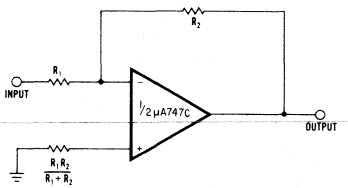
R_{IN} = 400 MΩ
C_{IN} = 1 pF
R_{OUT} < 1 Ω
B.W. = 1 MHz

NON-INVERTING AMPLIFIER



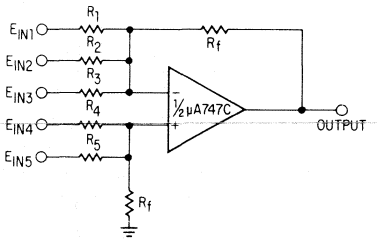
GAIN	R_1	R_2	B.W.	R_{IN}
10	1 kΩ	9 kΩ	100 kHz	400 MΩ
100	100 Ω	9.9 kΩ	10 kHz	280 MΩ
1000	100 Ω	99.9 kΩ	1 kHz	80 MΩ

INVERTING AMPLIFIER



GAIN	R_1	R_2	B.W.	R_{IN}
1	10 kΩ	10 kΩ	1 MHz	10 kΩ
10	1 kΩ	10 kΩ	100 kHz	1 kΩ
100	1 kΩ	100 kΩ	10 kHz	1 kΩ
1000	100 Ω	100 kΩ	1 kHz	100 Ω

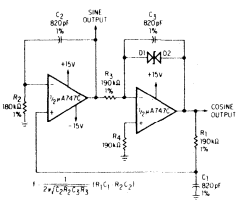
WEIGHTED AVERAGING AMPLIFIER



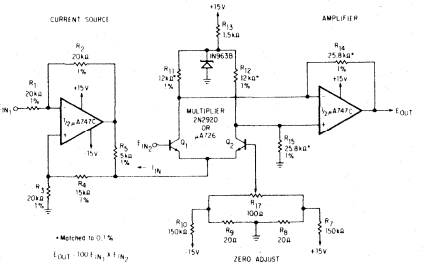
$$-E_{out} = E_{IN1}\left(\frac{R_f}{R_1}\right) + E_{IN2}\left(\frac{R_6}{R_2}\right) + E_{IN3}\left(\frac{R_6}{R_3}\right) - E_{IN4}\left(\frac{R_6}{R_4}\right) - E_{IN5}\left(\frac{R_6}{R_5}\right)$$

TYPICAL APPLICATIONS

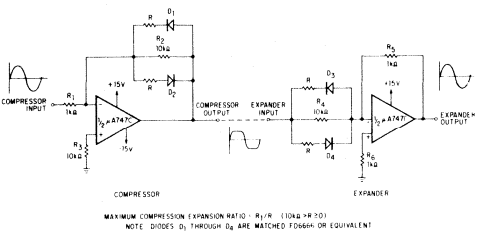
QUADRATURE OSCILLATOR



ANALOG MULTIPLIER



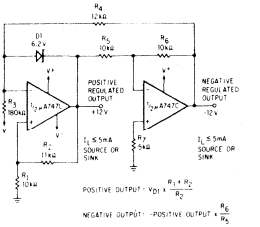
COMPRESSOR/EXPANDER AMPLIFIERS



MAXIMUM COMPRESSION EXPANSION RATIO = R_1/R = (10kΩ ÷ R Ω)

NOTE DIODES D_1 THROUGH D_4 ARE MATCHED FD666A OR EQUIVALENT

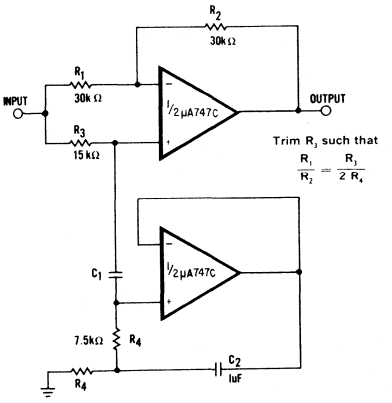
TRACKING POSITIVE AND NEGATIVE VOLTAGE REFERENCES



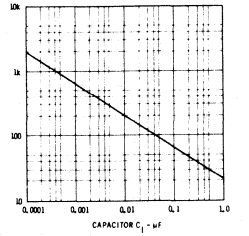
POSITIVE OUTPUT = $V_{D1} \times \frac{R_1 + R_2}{R_2}$

NEGATIVE OUTPUT = -POSITIVE OUTPUT $\times \frac{R_6}{R_5}$

NOTCH FILTER USING THE μA747C AS A GYRATOR



NOTCH FREQUENCY AS A FUNCTION OF C_1



μA748

HIGH PERFORMANCE OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

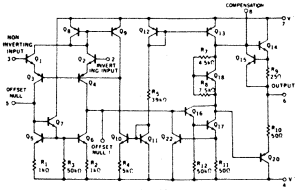
- **SHORT-CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **LOW POWER CONSUMPTION**
- **NO LATCH UP**

GENERAL DESCRIPTION — The μA748 is a high performance monolithic operational amplifier constructed on a single silicon chip, using the Fairchild Planar® epitaxial process. It is intended for a wide range of analog applications where tailoring of frequency characteristics is desirable. High common mode voltage range and absence of "latch-up" make the μA748 ideal for use as a voltage follower. The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier, and general feedback applications. The μA748 is short-circuit protected and has the same pin configuration as the popular μA741 operational amplifier. Unity gain frequency compensation is achieved by means of a single 30 pF capacitor. (For other Fairchild Operational Amplifiers, see page 5.)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22 V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 60 seconds)	300°C
Output Short-Circuit Duration (Note 3)	Indefinite

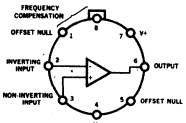
EQUIVALENT CIRCUIT



CONNECTION DIAGRAMS

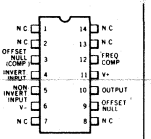
(TOP VIEW)

8 LEAD METAL CAN

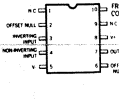


NOTE: Pin 4 connected to case

14 LEAD DIP

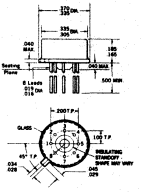


10 LEAD FP



PHYSICAL DIMENSIONS

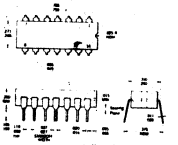
in accordance with JEDEC (TO-99) outline



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.22 grams

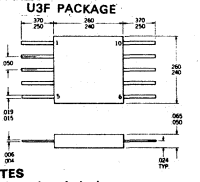
PART NO. U6A7748312

CERAMIC DIP 6A PACKAGE



PART NO. U5B7748312

U3F PACKAGE



NOTES
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers.
They are purposely shipped with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for .020 inch diameter lead.
Leads are gold-plated kovar for 8 lead.
Leads are tin-plated kovar for 14 lead.
Package weight is 0.6 gram for 8 lead, 2.0 gram for 14 lead package.

ORDER PART NO. U3F7748312

NOTES:
(1) Rating applies for case temperatures to +70°C.
(2) For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
(3) Short circuit may be to ground or either supply. Rating applies to +70°C ambient temperature.

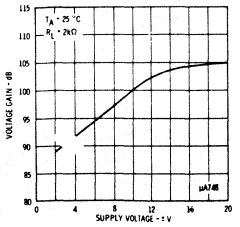
FAIRCHILD SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = 25°C$, $C_C = 30$ pF unless otherwise specified)

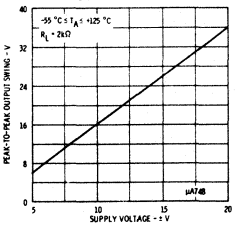
PARAMETERS (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	5.0	mV
Input Offset Current			20	200	nA
Input Bias Current			80	500	nA
Input Resistance		0.3	2.0		MΩ
Input Capacitance			2.0		pF
Offset Voltage Adjustment Range			±15		mV
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	50,000	150,000		
Output Resistance			75		Ω
Output Short-Circuit Current			25		mA
Supply Current			1.9	2.8	mA
Power Consumption			60	85	mW
Transient Response (Voltage Follower, Gain of 1)	$V_{IN} = 20$ mV, $C_C = 30$ pF, $R_L = 2$ kΩ, $C_L \leq 100$ pF				
Risetime			0.3		μs
Overshoot			5.0		%
Slew Rate (Voltage Follower, Gain of 1)	$R_L \geq 2$ kΩ		0.5		V/μs
Transient Response (Voltage Follower, Gain of 10)	$V_{IN} = 20$ mV, $C_C = 3.5$ pF, $R_L = 2$ kΩ, $C_L \leq 100$ pF				
Risetime			0.2		μs
Overshoot			5.0		%
Slew Rate (Voltage Follower, Gain of 10)	$R_L \geq 2$ kΩ, $C_C = 3.5$ pF		5.5		V/μs
The following specifications apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	6.0	mV
Input Offset Current	$T_A = +125°C$		10	200	nA
	$T_A = -55°C$		50	500	nA
Input Bias Current	$T_A = +125°C$		0.03	0.5	μA
	$T_A = -55°C$		0.3	1.5	μA
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150	μV/V
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	25,000			
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		V
Supply Current	$T_A = +125°C$		1.5	2.5	mA
	$T_A = -55°C$		2.0	3.3	mA
Power Consumption	$T_A = +125°C$		45	75	mW
	$T_A = -55°C$		60	100	mW

TYPICAL PERFORMANCE CURVES

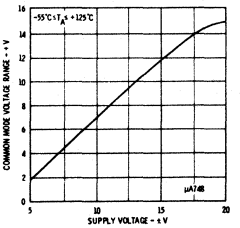
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE

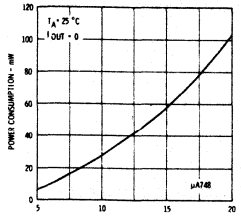


INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

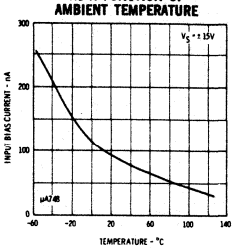


TYPICAL PERFORMANCE CURVES

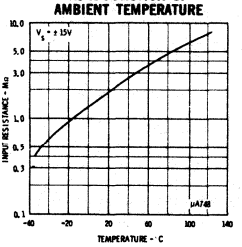
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



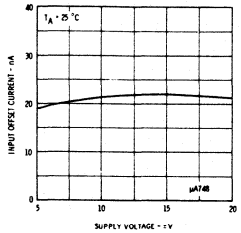
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



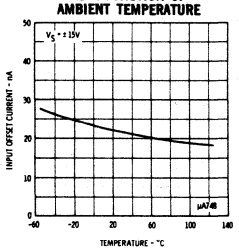
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



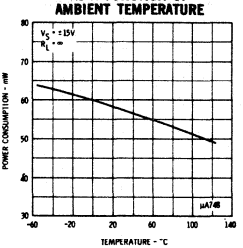
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



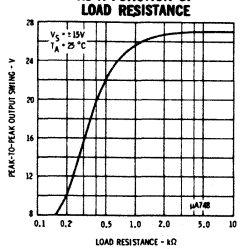
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



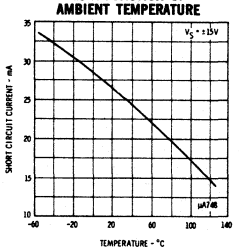
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



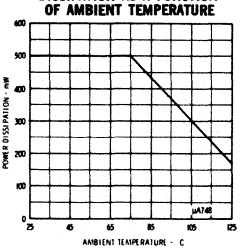
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



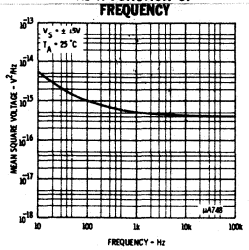
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



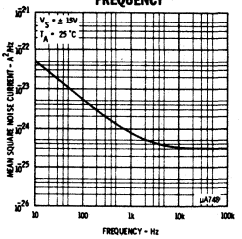
ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



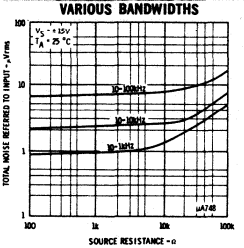
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY

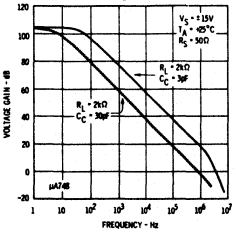


BROADBAND NOISE FOR VARIOUS BANDWIDTHS

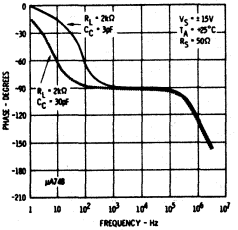


TYPICAL PERFORMANCE CURVES

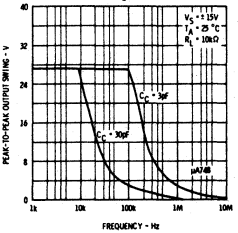
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



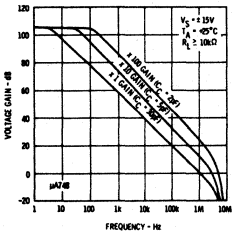
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



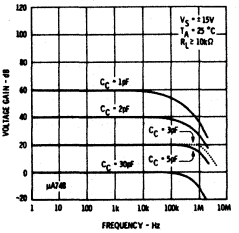
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



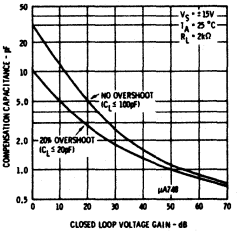
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY FOR VARIOUS GAIN/COMPENSATION OPTIONS



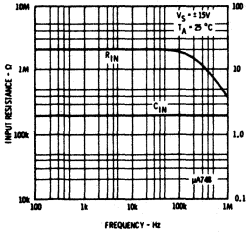
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS



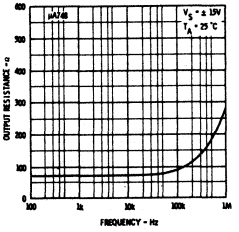
COMPENSATION CAPACITANCE AS A FUNCTION OF CLOSED LOOP VOLTAGE GAIN



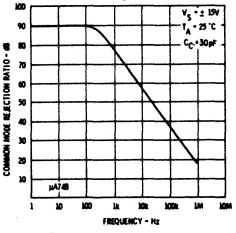
INPUT RESISTANCE AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY



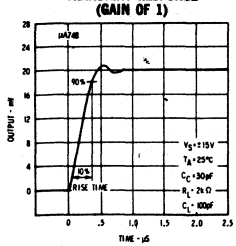
OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY



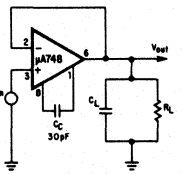
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



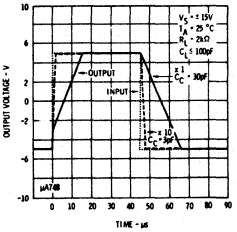
VOLTAGE FOLLOWER TRANSIENT RESPONSE (GAIN OF 1)



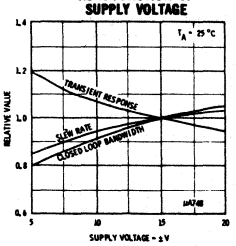
TRANSIENT RESPONSE TEST CIRCUIT



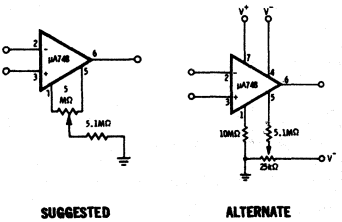
VOLTAGE FOLLOWER LARGE-SIGNAL PULSE RESPONSE



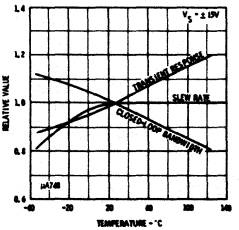
FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE



VOLTAGE OFFSET NULL CIRCUIT



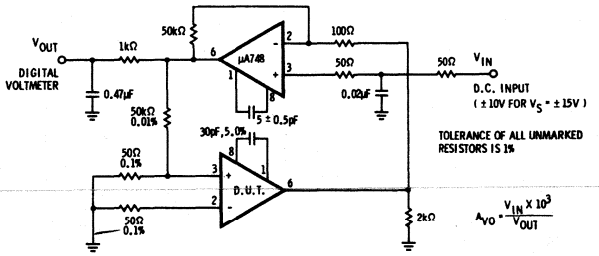
FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



DEFINITION OF TERMS

INPUT OFFSET VOLTAGE — That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.
INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the output at zero volts.
INPUT BIAS CURRENT — The average of the two input currents.
INPUT RESISTANCE — The resistance looking into either input terminal with the other grounded.
INPUT CAPACITANCE — The capacitance looking into either input terminal with the other grounded.
LARGE-SIGNAL VOLTAGE GAIN — The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.
OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.
OUTPUT SHORT-CIRCUIT CURRENT — The maximum output current available from the amplifier with the output shorted to ground or to either supply.
SUPPLY CURRENT — The DC current from the supplies required to operate the amplifier with the output at zero and with no load current.
POWER CONSUMPTION — The DC power required to operate the amplifier with the output at zero and with no load current.
TRANSIENT RESPONSE — The closed-loop step-function response of the amplifier under small-signal conditions.
INPUT VOLTAGE RANGE — The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.
INPUT COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.
SUPPLY VOLTAGE REJECTION RATIO — The ratio of the change in input offset voltage to the change in supply voltage producing it.
OUTPUT VOLTAGE SWING — The peak output swing, referred to zero, that can be obtained without clipping.

GAIN TEST CIRCUIT

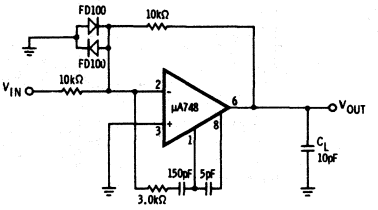


NOTES:

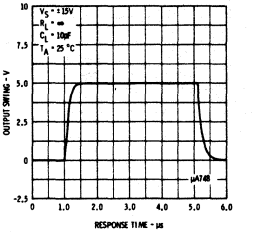
For other Fairchild Operational Amplifiers, see the following data sheets:

High Speed — μA715, μA715C.
Instrumentation — μA725, μA725B, μA725C.
Temperature Stable Preamps — μA727, μA727B.
Micropower — μA735, μA735B, μA735C.
Frequency Compensated — μA741, μA741C.
Duals — μA739C, μA749, μA749C, μA747, μA747C.
High Performance — μA101, μA201, μA748C.
Precision — μA777, μA777B, μA777C, μA101A, μA201A, μA301A.

FEED-FORWARD COMPENSATION

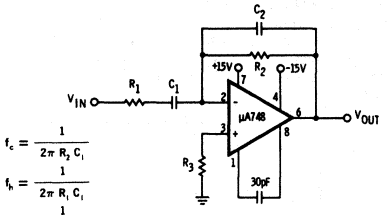


LARGE SIGNAL FEED-FORWARD TRANSIENT RESPONSE



TYPICAL APPLICATIONS

PRACTICAL DIFFERENTIATOR

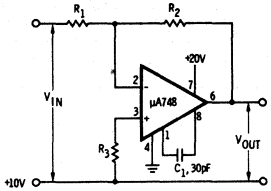


$$f_c = \frac{1}{2\pi R_2 C_1}$$

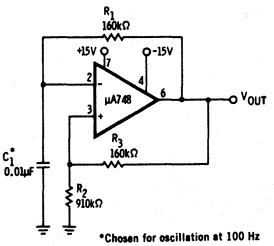
$$f_h = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi R_2 C_2}$$

$f_c < f_h < f_{unity\ gain}$

CIRCUIT FOR OPERATING THE μA748 WITHOUT A NEGATIVE SUPPLY

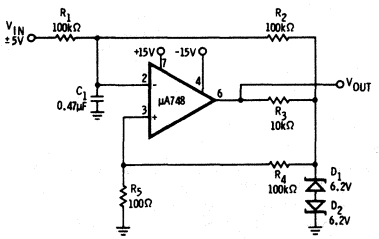


FREE-RUNNING MULTIVIBRATOR



*Chosen for oscillation at 100 Hz

PULSE WIDTH MODULATOR



μA748C

HIGH PERFORMANCE OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED AMPLIFIER

- **SHORT-CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **LOW POWER CONSUMPTION**
- **NO LATCH UP**

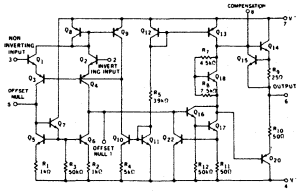
GENERAL DESCRIPTION — The μA748C is a high performance monolithic operational amplifier constructed on a single silicon chip, using the Fairchild Planar* epitaxial process. It is intended for a wide range of analog applications where tailoring of frequency characteristics is desirable. High common mode voltage range and absence of "latch-up" make the μA748C ideal for use as a voltage follower. The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier, and general feedback applications. The μA748C is short-circuit protected and has the same pin configuration as the popular μA741 operational amplifier. Unity gain frequency compensation is achieved by means of a single 30 pF capacitor. For full temperature range operation (−55°C to +125°C), see μA748 data sheet.

(For other Fairchild Operational Amplifiers, see page 5.)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22 V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range DIP	−55°C to +125°C
Metal Can	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 60 seconds) DIP	260°C
Metal Can	300°C
Output Short-Circuit Duration (Note 3)	Indefinite

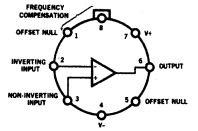
EQUIVALENT CIRCUIT



CONNECTION DIAGRAMS

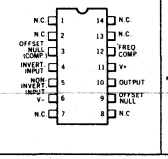
(TOP VIEW)

8 LEAD METAL CAN

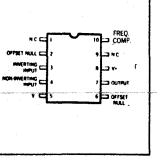


NOTE: Pin 4 connected to case

14 LEAD DIP



10 LEAD FP



NOTES:

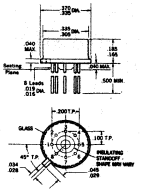
(1) Rating applies for case temperatures to +70°C.

(2) For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

(3) Short circuit may be to ground or either supply. Rating applies to +70°C ambient temperature.

PHYSICAL DIMENSIONS

in accordance with JEDEC (TO-99) outline



NOTES:

All dimensions in inches

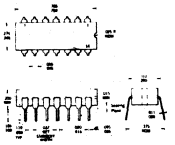
Leads are gold-plated kovar

Package weight is 1.22 grams

ORDER PART NO. U5B7748393

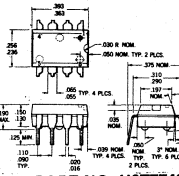
CERAMIC DIP

6A PACKAGE



ORDER PART NO. U6A7748393

8 LEAD DIP



ORDER PART NO. U9T7748393

NOTES:

All dimensions in inches

Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion

Board-drilling dimensions should equal your practice for .020 inch diameter lead

Leads are gold-plated kovar

Package weight is 0.6 gram for 8 lead, 0.9 gram for 14 lead package

*Planar is a patented Fairchild process.

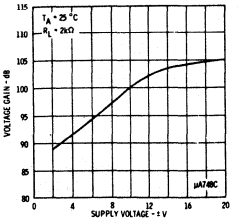
FAIRCHILD SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = 25°C$, $C_C = 30$ pF unless otherwise specified)

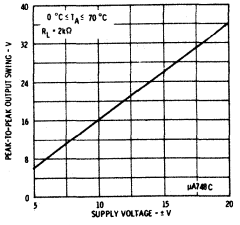
PARAMETERS (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ		2.0	6.0	mV
Input Offset Current			20	200	nA
Input Bias Current			80	500	nA
Input Resistance		0.3	2.0		MΩ
Input Capacitance			2.0		pF
Offset Voltage Adjustment Range			±15		mV
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	20,000	150,000		
Output Resistance			75		Ω
Output Short-Circuit Current			25		mA
Supply Current			1.9	2.8	mA
Power Consumption			60	85	mW
Transient Response (Voltage Follower, Gain of 1)	$V_{IN} = 20$ mV, $C_C = 30$ pF, $R_L = 2$ kΩ, $C_L \leq 100$ pF				
Risetime			0.3		μs
Overshoot			5.0		%
Slew Rate (Voltage Follower, Gain of 1)	$R_L \geq 2$ kΩ		0.5		V/μs
Transient Response (Voltage Follower, Gain of 10)	$V_{IN} = 20$ mV, $C_C = 3.5$ pF, $R_L = 2$ kΩ, $C_L \leq 100$ pF				
Risetime			0.2		μs
Overshoot			5.0		%
Slew Rate (Voltage Follower, Gain of 10)	$R_L \geq 2$ kΩ		5.5		V/μs
The following specifications apply for $0°C \leq T_A \leq +70°C$:					
Input Offset Voltage	$R_S \leq 10$ kΩ			7.5	mV
Input Offset Current				300	nA
Input Bias Current				800	nA
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150	μV/V
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	15,000			
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		V
Power Consumption			60	100	mW

TYPICAL PERFORMANCE CURVES

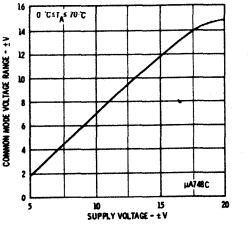
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE

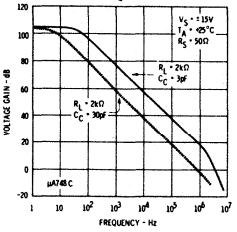


INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

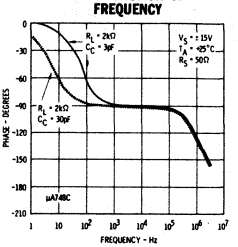


TYPICAL PERFORMANCE CURVES

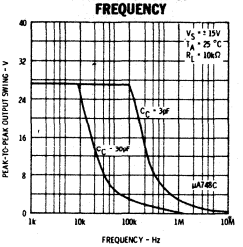
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



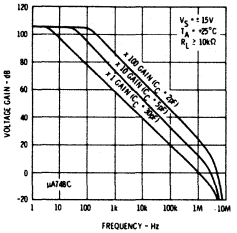
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



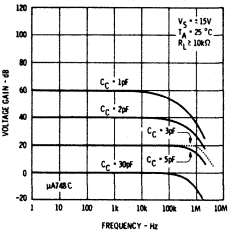
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



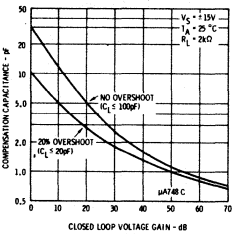
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY FOR VARIOUS GAIN/COMPENSATION OPTIONS



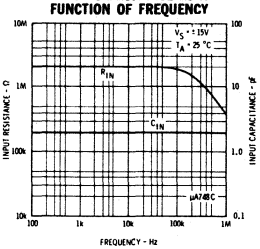
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS



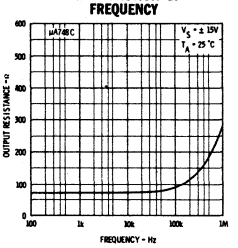
COMPENSATION CAPACITANCE AS A FUNCTION OF CLOSED LOOP VOLTAGE GAIN



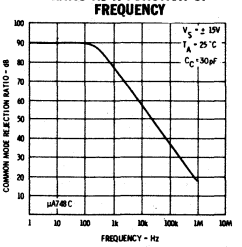
INPUT RESISTANCE AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY



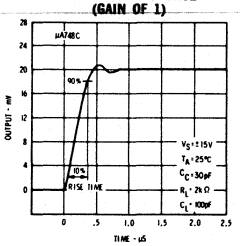
OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY



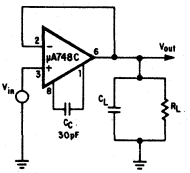
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



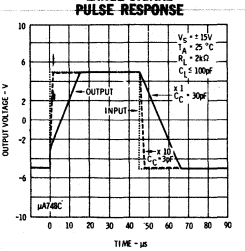
VOLTAGE FOLLOWER TRANSIENT RESPONSE (GAIN OF 1)



TRANSIENT RESPONSE TEST CIRCUIT

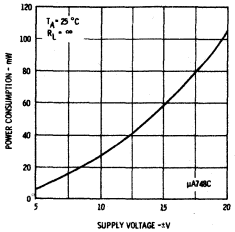


VOLTAGE FOLLOWER LARGE-SIGNAL PULSE RESPONSE

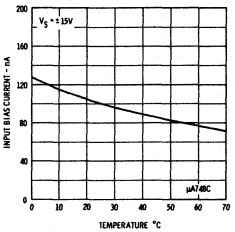


TYPICAL PERFORMANCE CURVES

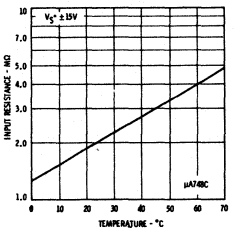
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



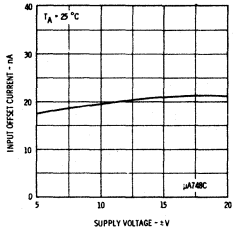
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



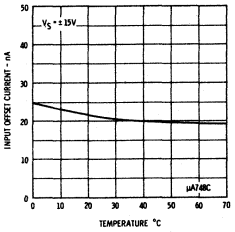
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



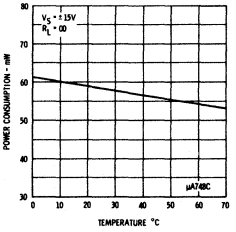
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



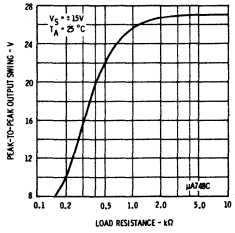
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



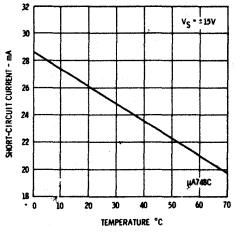
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



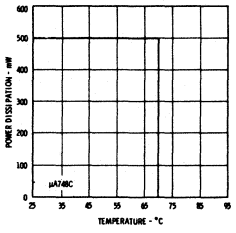
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



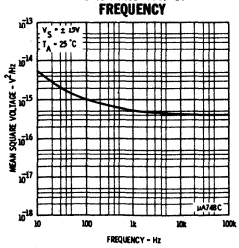
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



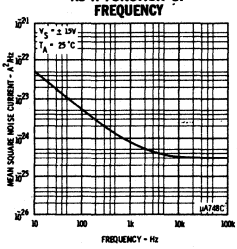
ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



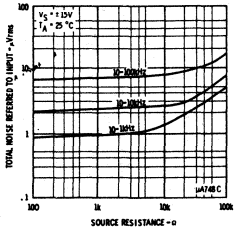
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



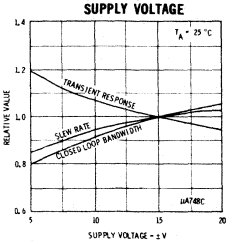
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



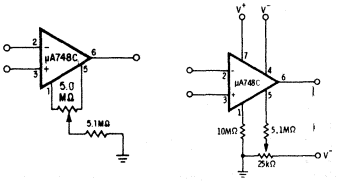
BROADBAND NOISE FOR VARIOUS BANDWIDTHS



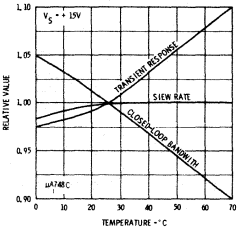
FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE



VOLTAGE OFFSET NULL CIRCUIT



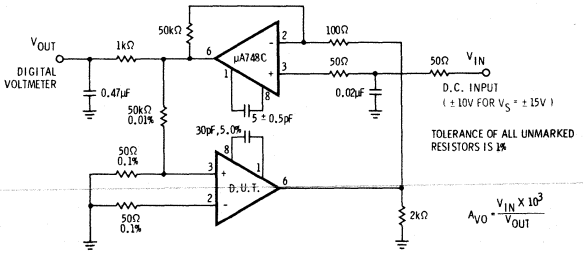
FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



DEFINITION OF TERMS

INPUT OFFSET VOLTAGE — That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.
INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the output at zero volts.
INPUT BIAS CURRENT — The average of the two input currents.
INPUT RESISTANCE — The resistance looking into either input terminal with the other grounded.
INPUT CAPACITANCE — The capacitance looking into either input terminal with the other grounded.
LARGE-SIGNAL VOLTAGE GAIN — The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.
OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.
OUTPUT SHORT-CIRCUIT CURRENT — The maximum output current available from the amplifier with the output shorted to ground or to either supply.
SUPPLY CURRENT — The DC current from the supplies required to operate the amplifier with the output at zero and with no load current.
POWER CONSUMPTION — The DC power required to operate the amplifier with the output at zero and with no load current.
TRANSIENT RESPONSE — The closed-loop step-function response of the amplifier under small-signal conditions.
INPUT VOLTAGE RANGE — The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.
INPUT COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.
SUPPLY VOLTAGE REJECTION RATIO — The ratio of the change in input offset voltage to the change in supply voltage producing it.
OUTPUT VOLTAGE SWING — The peak output swing, referred to zero, that can be obtained without clipping.

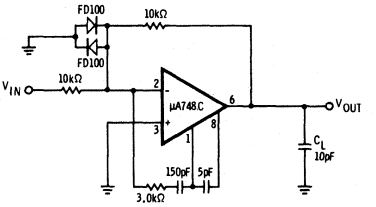
GAIN TEST CIRCUIT



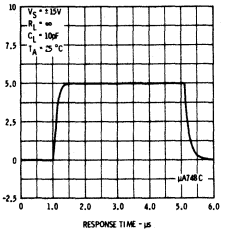
NOTE:
FOR OTHER FAIRCHILD OPERATIONAL AMPLIFIERS, SEE THE FOLLOWING DATA SHEETS:

HIGH SPEED — μA715, μA715C
INSTRUMENTATION OPERATIONAL AMPLIFIER — μA725, μA725B μA725C
TEMPERATURE STABLE PREAMPS — μA727, μA727B
MICROPOWER — μA735, μA735B, μA735C
FET INPUT — μA740, μA740C
FREQUENCY COMPENSATED — μA741, μA741C
DUALS — μA739C, μA749, μA749C, μA747, μA747C
HIGH PERFORMANCE — μA748, μA748C
PRECISION — μA777, μA777B, μA777C

FEED-FORWARD COMPENSATION

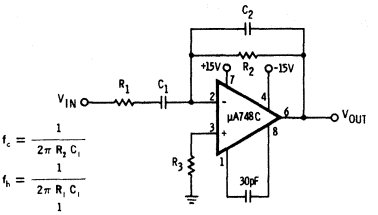


LARGE SIGNAL FEED-FORWARD TRANSIENT RESPONSE



TYPICAL APPLICATIONS

PRACTICAL DIFFERENTIATOR

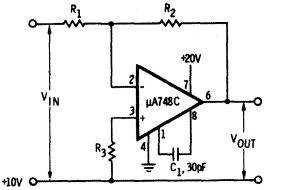


$$f_c = \frac{1}{2\pi R_2 C_1}$$

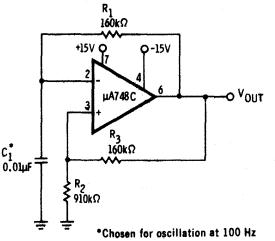
$$f_h = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi R_2 C_2}$$

$f_c < f_h < f_{unity\ gain}$

CIRCUIT FOR OPERATING THE μA748 WITHOUT A NEGATIVE SUPPLY

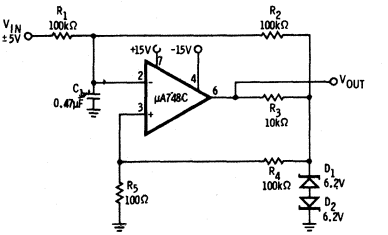


FREE-RUNNING MULTIVIBRATOR



*Chosen for oscillation at 100 Hz

PULSE WIDTH MODULATOR



μA749
DUAL OPERATIONAL AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

FEATURES:

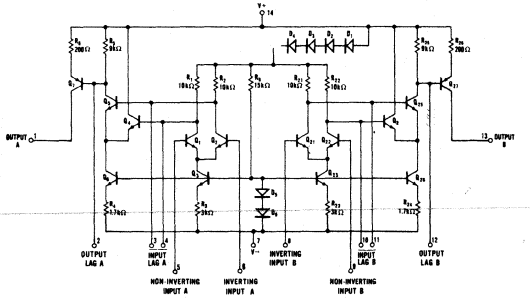
- **SINGLE OR DUAL SUPPLY OPERATION**
- **LOW POWER CONSUMPTION**
- **HIGH GAIN, 20,000 V/V**
- **LARGE COMMON MODE RANGE, ±11 V**
- **EXCELLENT GAIN STABILITY VS. SUPPLY VOLTAGE**
- **NO LATCH-UP**
- **OUTPUT SHORT CIRCUIT PROTECTED**

GENERAL DESCRIPTION — The μA749 consists of two identical high gain operational amplifiers constructed on a single silicon chip using the Fairchild Planar* epitaxial process. These three-stage amplifiers use class A PNP transistor output stages with uncommitted collectors. This enables a variety of loads to be employed for general purpose applications from DC to 10 MHz where two high performance operational amplifiers are required. In addition, the outputs may be 'OR'ed for use as a dual comparator or they may function as diodes in low threshold rectifying circuits such as absolute value amplifiers, peak detectors, etc.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18 V
Internal Power Dissipation (Note 1)	DIP 500 mW
	Flat Pack 350 mW
Differential Input Voltage	±5 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 60 seconds)	300°C
Output Short-Circuit Duration, $T_A = 25°C$ (Note 3)	30 seconds

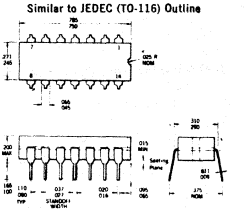
EQUIVALENT CIRCUIT



Notes on Page 4.

TYPICAL DUAL IN-LINE PACKAGE

Similar to JEDEC (TO-116) Outline

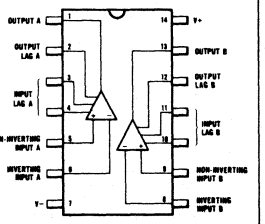


NOTES:
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.
Board drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

ORDER PART NO. U6A7749312

CONNECTION DIAGRAM

(TOP VIEW)



*Planar is a patented Fairchild process.

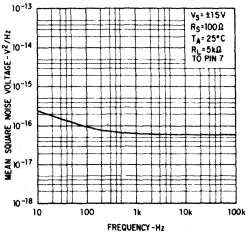
FAIRCHILD SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $R_L = 5$ kΩ to Pin 7, $T_A = 25°C$ unless otherwise specified)

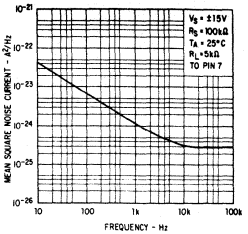
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S = 200\ \Omega$		1.0		mV
Input Offset Current			50		nA
Input Bias Current			300		nA
Input Resistance			150		kΩ
Large-Signal Voltage Gain	$V_{OUT} = \pm 10$ V		20,000		V/V
Positive Output Voltage Swing			+13		V
Negative Output Voltage Swing			−15		V
Output Resistance	f = 1.0 kHz		5.0		kΩ
Common Mode Rejection Ratio	$R_S = 200\ \Omega$, $V_{IN} = +10$ V to −10 V		90		dB
Supply Voltage Rejection Ratio	$R_S = 200\ \Omega$		50		μV/V
Internal Power Dissipation	$V_{OUT} = 0$		180		mW
Supply Current	$V_{OUT} = 0$		9.0		mA
Broadband Noise Figure	$R_S = 10$ kΩ, BW = 10 Hz to 10 kHz		2.5		dB
Turn On Delay (See Figure 1)	Open Loop, $V_{IN} = \pm 20$ mV		0.2		μs
Turn Off Delay (See Figure 1)	Open Loop, $V_{IN} = \pm 20$ mV		0.3		μs
Slew Rate (unity gain) (See Figure 2)	$C_1 = .02\ \mu$F, $R_1 = 33\ \Omega$, $C_2 = 10$ pF		2.0		V/μs
Channel Separation (See Figure 3)	$R_S = 1$ kΩ, f = 10 kHz		140		dB
The following specifications apply for $V_S = \pm 4.0$ V, $R_L = 10$ kΩ to Pin 7					
Input Offset Voltage	$R_S = 200\ \Omega$		1.0		mV
Input Offset Current			50		nA
Input Bias Current			300		nA
Supply Current	$V_{OUT} = 0$		2.5		mA
Internal Power Dissipation	$V_{OUT} = 0$		20		mW
Large-Signal Voltage Gain	$V_{OUT} = \pm 1.0$ V		15,000		V/V
Positive Output Voltage Swing			+2.8		V
Negative Output Voltage Swing			−4.0		V
The following specifications apply for $-55°C < T_A < +125°C$: $V_S = \pm 15$ V, $R_L = 5$ kΩ to Pin 7:					
Large Signal Voltage Gain	$V_{OUT} = \pm 5.0$ V		20,000		V/V
Positive Output Voltage Swing			+13		V
Negative Output Voltage Swing			−15		V
Input Offset Voltage	$R_S = 200\ \Omega$		1.0		mV
Input Offset Current			50		nA
Input Bias Current			300		nA
Input Offset Voltage Drift	$R_S = 200\ \Omega$, $+25°C \le T_A \le +125°C$		3.0		μV/°C
	$R_S = 200\ \Omega$, $-55°C \le T_A \le +25°C$		3.0		μV/°C
Input Offset Current Drift	$+25°C \le T_A \le +125°C$		0.5		nA/°C
	$-55°C \le T_A \le +25°C$		2.0		nA/°C
Input Bias Current Drift	$-55°C \le T_A \le +125°C$		5.0		nA/°C
The following specifications apply for $-55°C \le T_A \le +125°C$: $V_S = \pm 4$ V, $R_L = 10$ kΩ to Pin 7:					
Input Offset Voltage	$R_S = 200\ \Omega$		1.5		mV
Input Offset Current			50		nA
Input Bias Current			300		nA
Large-Signal Voltage Gain	$V_{OUT} = \pm 1.0$ V		15,000		V/V
Positive Output Voltage Swing			+2.8		V
Negative Output Voltage Swing			−4.0		V

TYPICAL PERFORMANCE CURVES

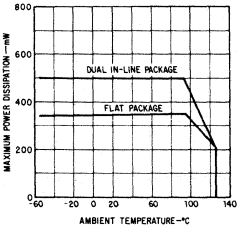
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



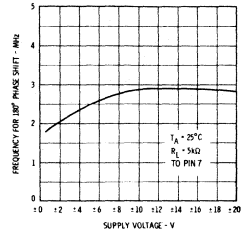
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



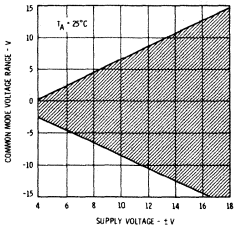
ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



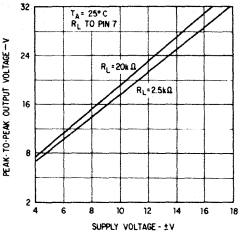
OPEN LOOP 180° PHASE SHIFT FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



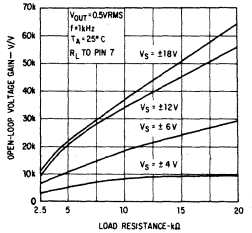
COMMON MODE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



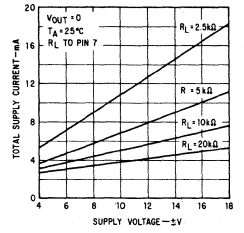
TYPICAL OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



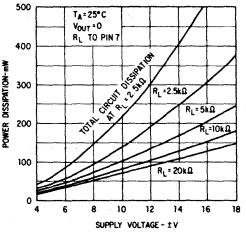
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF LOAD RESISTANCE



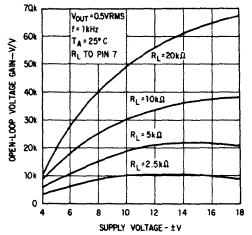
TOTAL SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



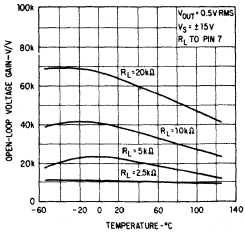
TOTAL POWER DISSIPATION AS A FUNCTION OF SUPPLY VOLTAGE AND LOAD



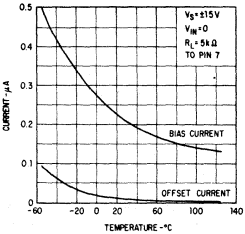
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



OPEN LOOP GAIN AS A FUNCTION OF TEMPERATURE

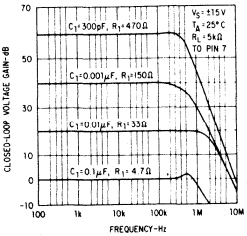


INPUT OFFSET CURRENT AND BIAS CURRENT AS FUNCTIONS OF TEMPERATURE

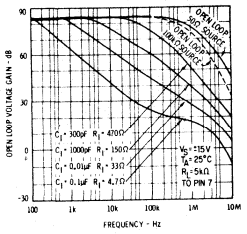


TYPICAL PERFORMANCE CURVES

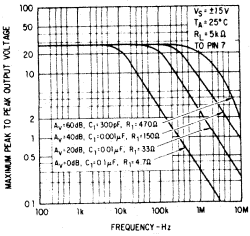
CLOSED LOOP GAIN AS A FUNCTION OF FREQUENCY



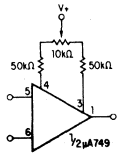
OPEN LOOP FREQUENCY RESPONSE USING RECOMMENDED COMPENSATION NETWORKS



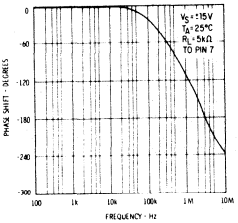
OUTPUT CAPABILITY AS A FUNCTION OF FREQUENCY AND COMPENSATION



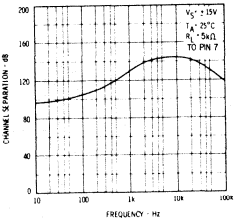
OFFSET NULL NETWORK



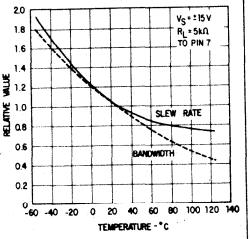
OPEN LOOP PHASE SHIFT WITHOUT COMPENSATION



CHANNEL SEPARATION AS A FUNCTION OF FREQUENCY



CHANGE OF A.C. CHARACTERISTICS WITH TEMPERATURE



PULSE RESPONSE WAVEFORMS

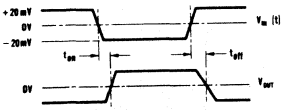


Figure 1

FREQUENCY RESPONSE TEST CIRCUIT

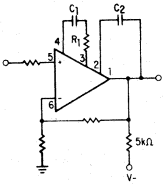


Figure 2

CHANNEL SEPARATION TEST CIRCUIT

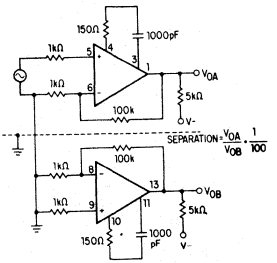


Figure 3

NOTES:

(1) Derate Dual In-line at 9.0 mW/°C above 95°C and Flat Pack at 4.5 mW/°C above 95°C.

(2) For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

(3) Short circuit may be to ground or either supply.

μA749C
DUAL OPERATIONAL AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

FEATURES:

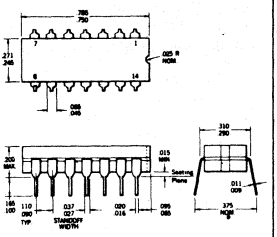
- **SINGLE OR DUAL SUPPLY OPERATION**
- **LOW POWER CONSUMPTION**
- **HIGH GAIN, 20,000 V/V**
- **LARGE COMMON MODE RANGE, ±11 V**
- **EXCELLENT GAIN STABILITY VS. SUPPLY VOLTAGE**
- **NO LATCH-UP**
- **OUTPUT SHORT CIRCUIT PROTECTED**

GENERAL DESCRIPTION — The μA749C consists of two identical high gain operational amplifiers constructed on a single silicon chip using the Fairchild Planar* epitaxial process. These three-stage amplifiers use class A PNP transistor output stages with uncommitted collectors. This enables a variety of loads to be employed for general purpose applications from DC to 10 MHz where two high performance operational amplifiers are required. In addition, the outputs may be 'OR'ed for use as a dual comparator or they may function as diodes in low threshold rectifying circuits such as absolute value amplifiers, peak detectors, etc.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18 V
Internal Power Dissipation	500 mW
Differential Input Voltage	±5 V
Input Voltage (Note 1)	±15 V
Storage Temperature Range	−55°C to +125°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 60 seconds)	300°C
Output Short-Circuit Duration, $T_A = 25°C$ (Note 2)	30 seconds

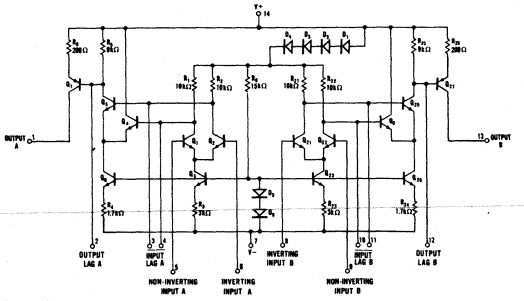
TYPICAL DUAL IN-LINE PACKAGE
Similar to JEDEC (TO-116) Outline



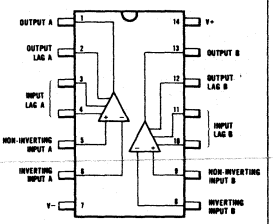
NOTES:
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.
Board drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

ORDER PART NO. U6A7749393

EQUIVALENT CIRCUIT



CONNECTION DIAGRAM
(TOP VIEW)



Notes on Page 4.

*Planar is a patented Fairchild process.

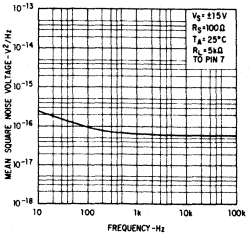
FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $R_L = 5$ kΩ to Pin 7, $T_A = 25°C$ unless otherwise specified)

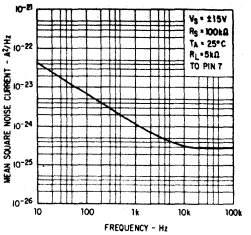
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S = 200\ \Omega$		1.0		mV
Input Offset Current			50		nA
Input Bias Current			300		nA
Input Resistance			150		kΩ
Large-Signal Voltage Gain	$V_{OUT} = \pm 10$ V		20,000		V/V
Positive Output Voltage Swing			+13		V
Negative Output Voltage Swing			−15		V
Output Resistance	f = 1.0 kHz		5.0		kΩ
Common Mode Rejection Ratio	$R_S = 200\ \Omega$, $V_{IN} = +10$ V to −10 V		90		dB
Supply Voltage Rejection Ratio	$R_S = 200\ \Omega$		50		μV/V
Internal Power Dissipation	$V_{OUT} = 0$		180		mW
Supply Current	$V_{OUT} = 0$		9.0		mA
Broadband Noise Figure	$R_S = 10$ kΩ, BW = 10 Hz to 10 kHz		2.5		dB
Turn On Delay (See Figure 1)	Open Loop, $V_{IN} = \pm 20$ mV		0.2		μs
Turn Off Delay (See Figure 1)	Open Loop, $V_{IN} = \pm 20$ mV		0.3		μs
Slew Rate (unity gain) (See Figure 2)	$C_1 = .02\ \mu$F, $R_1 = 33\ \Omega$, $C_2 = 10$ pF		2.0		V/μs
Channel Separation (See Figure 3)	$R_S = 1$ kΩ, f = 10 kHz		140		dB
The following specifications apply for $V_S = \pm 4.0$ V, $R_L = 10$ kΩ to Pin 7:					
Input Offset Voltage	$R_S = 200\ \Omega$		1.0		mV
Input Offset Current			50		nA
Input Bias Current			300		nA
Supply Current	$V_{OUT} = 0$		2.5		mA
Internal Power Dissipation	$V_{OUT} = 0$		20		mW
Large-Signal Voltage Gain	$V_{OUT} = \pm 1.0$ V		15,000		V/V
Positive Output Voltage Swing			+2.8		V
Negative Output Voltage Swing			−4.0		V
The following specifications apply for $0°C \leq T_A \leq +70°C$: $V_S = \pm 15$ V, $R_L = 5$ kΩ to Pin 7:					
Large Signal Voltage Gain	$V_{OUT} = \pm 5.0$ V		20,000		V/V
Positive Output Voltage Swing			+13		V
Negative Output Voltage Swing			−15		V
Input Offset Voltage	$R_S = 200\ \Omega$		1.0		mV
Input Offset Current			50		nA
Input Bias Current			300		nA
Input Offset Voltage Drift	$R_S = 200\ \Omega$, $+25°C \leq T_A \leq +70°C$		3.0		μV/°C
	$R_S = 200\ \Omega$, $+25°C \leq T_A \leq 0°C$		3.0		
Input Offset Current Drift	$+25°C \leq T_A \leq +70°C$		0.5		nA/°C
	$+25°C \leq T_A \leq 0°C$		2.0		nA/°C
Input Bias Current Drift	$0°C \leq T_A \leq +70°C$		4.0		nA/°C
The following specifications apply for $0°C \leq T_A \leq +70°C$: $V_S = \pm 4$ V, $R_L = 10$ kΩ to Pin 7:					
Input Offset Voltage	$R_S = 200\ \Omega$		1.5		mV
Input Offset Current			50		nA
Input Bias Current			300		nA
Large-Signal Voltage Gain	$V_{OUT} = \pm 1.0$ V		15,000		V/V
Positive Output Voltage Swing			+2.8		V
Negative Output Voltage Swing			−4.0		V

TYPICAL PERFORMANCE CURVES

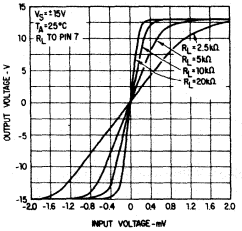
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



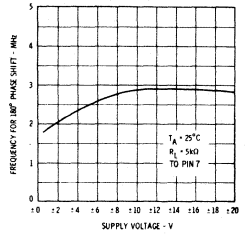
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



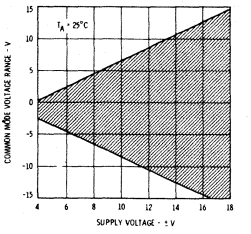
OPEN LOOP DC TRANSFER CHARACTERISTICS



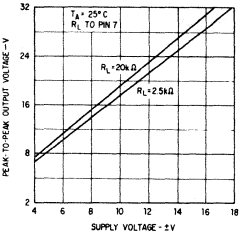
OPEN LOOP 180° PHASE SHIFT FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



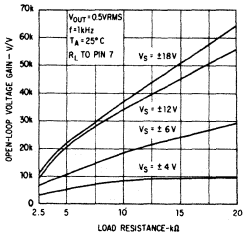
COMMON MODE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



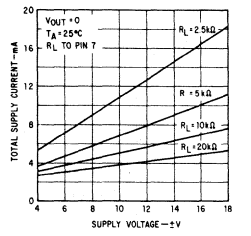
DC OUTPUT VOLTAGE CAPABILITY AS A FUNCTION OF SUPPLY VOLTAGE



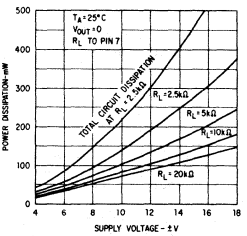
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF LOAD RESISTANCE



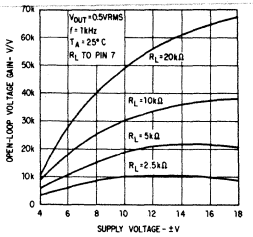
TOTAL SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



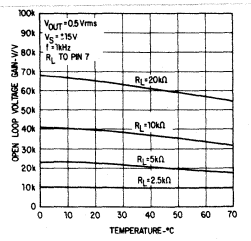
DEVICE POWER DISSIPATION AS A FUNCTION OF SUPPLY VOLTAGE AND LOAD



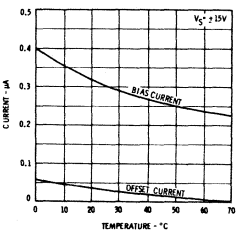
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



OPEN LOOP GAIN AS A FUNCTION OF TEMPERATURE

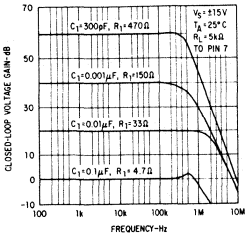


INPUT OFFSET CURRENT AND BIAS CURRENT AS FUNCTIONS OF TEMPERATURE

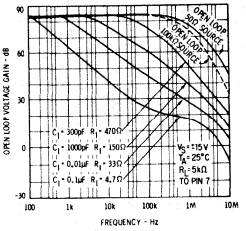


TYPICAL PERFORMANCE CURVES

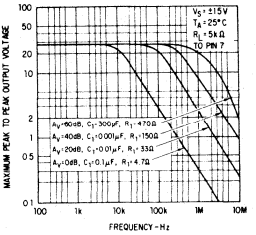
CLOSED LOOP GAIN AS A FUNCTION OF FREQUENCY



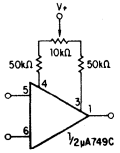
OPEN LOOP FREQUENCY RESPONSE USING RECOMMENDED COMPENSATION NETWORKS



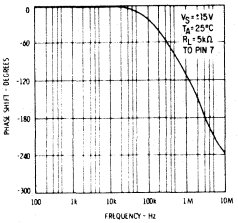
OUTPUT CAPABILITY AS A FUNCTION OF FREQUENCY AND COMPENSATION



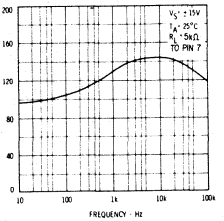
OFFSET NULL NETWORK



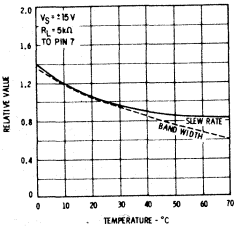
OPEN LOOP PHASE SHIFT WITHOUT COMPENSATION



CHANNEL SEPARATION AS A FUNCTION OF FREQUENCY



CHANGE OF A.C. CHARACTERISTICS WITH TEMPERATURE



PULSE RESPONSE WAVEFORMS

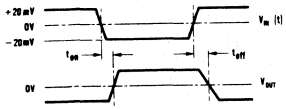


Figure 1

FREQUENCY RESPONSE TEST CIRCUIT

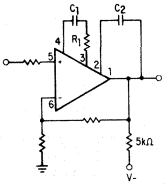


Figure 2

CHANNEL SEPARATION TEST CIRCUIT

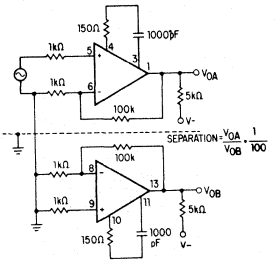


Figure 3

NOTES:
(1) For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.
(2) Short circuit may be to ground or either supply.

μA749D
DUAL CHANNEL AUDIO AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA749D consists of two identical amplifiers constructed on a single silicon chip using the Fairchild Planar* epitaxial process. These high-gain amplifiers exhibit stable operating characteristics over a wide range of supply voltage and temperatures. The device is intended for a variety of applications requiring two high gain audio amplifiers.

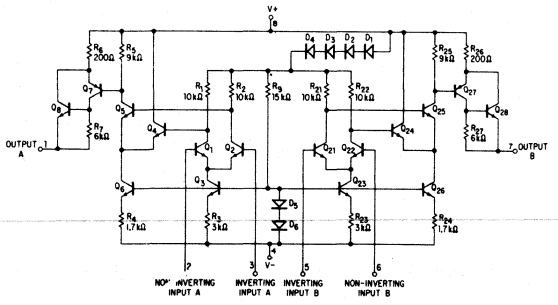
FEATURES
- **SINGLE OR DUAL SUPPLY OPERATION**
- **HIGH VOLTAGE GAIN, 20,000**
- **EXCELLENT GAIN STABILITY VS. SUPPLY VOLTAGE**
- **NO LATCH-UP**
- **OUTPUT SHORT CIRCUIT PROTECTED**

TYPICAL APPLICATIONS
- **STEREO TAPE PREAMPLIFIER**
- **TV REMOTE CONTROL RECEIVER**
- **DUAL COMPARATOR**
- **SENSE AMPLIFIER**
- **OSCILLATOR**

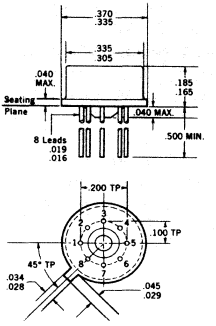
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±12 V
Internal Power Dissipation	500 mW
Differential Input Voltage	±5 V
Input Voltage (Note 1)	±12 V
Storage Temperature Range	−55°C to +125°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 60 seconds)	300°C
Output Short-Circuit Duration, T_A = 25°C (Note 2)	30 seconds

SCHEMATIC DIAGRAM



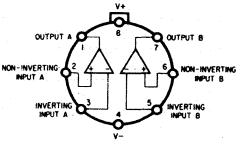
PHYSICAL DIMENSIONS
in accordance with JEDEC (TO-99) outline



NOTES:
All dimensions in inches
Leads are gold plated Kovar
Package weight is 1.22 grams

ORDER PART NO. U5B7749394

CONNECTION DIAGRAM
(TOP VIEW)



Note: Pin 4 connected to case

Notes on Page 2

*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS ($V_S = \pm 6$ V, $R_L = 10$ kΩ to Pin 4, $T_A = 25°C$ unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 200\ \Omega$		1.0	10	mV
Input Offset Current			50	600	nA
Input Bias Current			300	1500	nA
Input Resistance		50	150		kΩ
Large-Signal Voltage Gain	$V_{OUT} = \pm 4.0$ V	10,000	20,000		V/V
Positive Output Voltage Swing		+4.5	+5		Volts
Negative Output Voltage Swing		−5.5	−6		Volts
Output Resistance	f = 1.0 kHz		10		kΩ
Input Voltage Range		−4		+2.5	Volts
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		50	100	μV/V
Power Consumption (including load)	$V_{OUT} = 0$	24	36	54	mW
Supply Current (including load)	$V_{OUT} = 0$	2.0	3.0	4.5	mA
Turn On Delay (See Figure 1)	Open Loop, $V_{IN} = \pm 20$ mV, $R_L = 5$ kΩ		0.2		μs
Turn Off Delay (See Figure 1)	Open Loop, $V_{IN} = \pm 20$ mV, $R_L = 5$ kΩ		0.3		μs
Channel Separation (See Figure 3)	$R_S \leq 10$ kΩ, f = 10 kHz		140		dB

PULSE RESPONSE WAVEFORMS

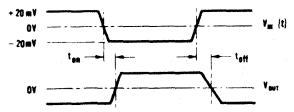


Figure 1

FREQUENCY RESPONSE TEST CIRCUIT

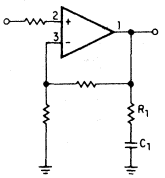


Figure 2

CHANNEL SEPARATION TEST CIRCUIT

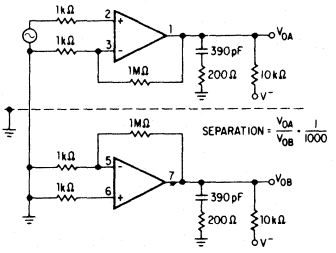
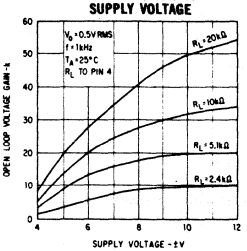


Figure 3

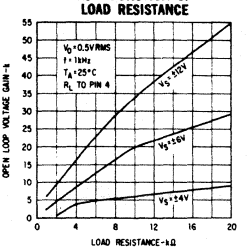
NOTES:
(1) For supply voltages less than ±12 V, the absolute maximum input voltage is equal to the supply voltage.
(2) Short circuit may be to ground or either supply.

TYPICAL PERFORMANCE CURVES

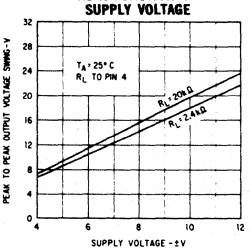
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



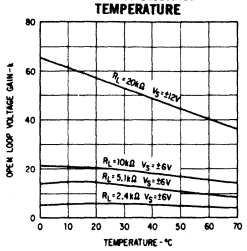
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF LOAD RESISTANCE



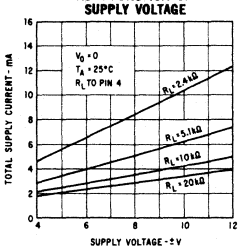
TYPICAL OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



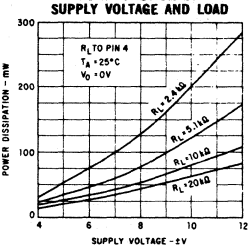
OPEN LOOP GAIN AS A FUNCTION OF TEMPERATURE



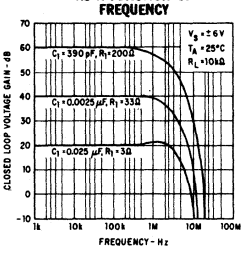
TOTAL SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



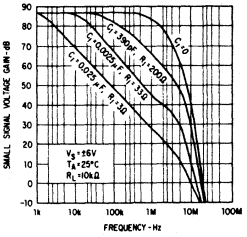
TOTAL POWER DISSIPATION AS A FUNCTION OF SUPPLY VOLTAGE AND LOAD



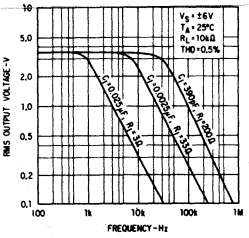
CLOSED LOOP GAIN AS A FUNCTION OF FREQUENCY



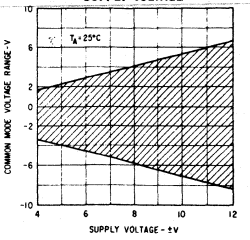
OPEN LOOP FREQUENCY RESPONSE USING RECOMMENDED COMPENSATION NETWORKS



OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS COMPENSATION NETWORKS

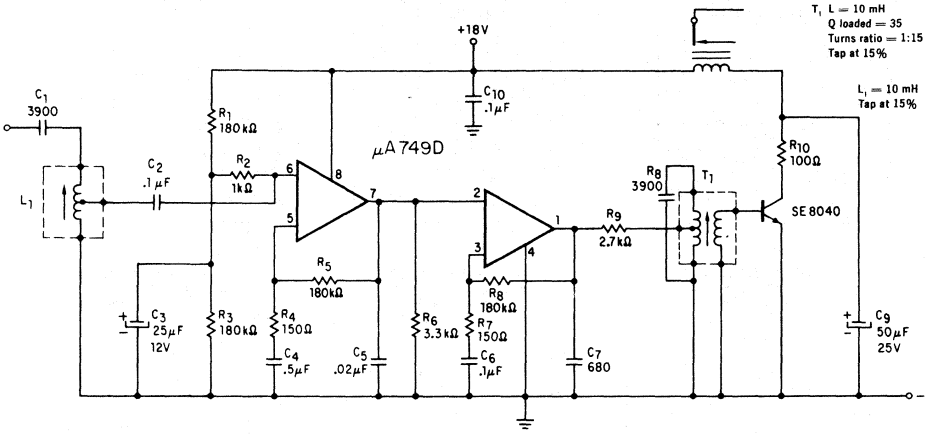


COMMON MODE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

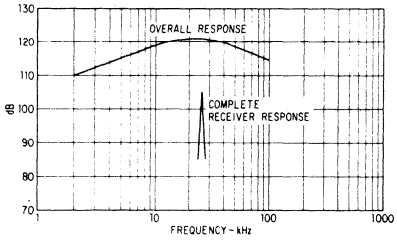


APPLICATIONS

Figure 4. T.V. REMOTE CONTROL RECEIVER

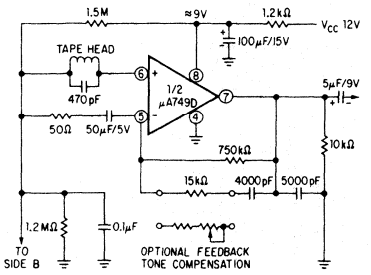


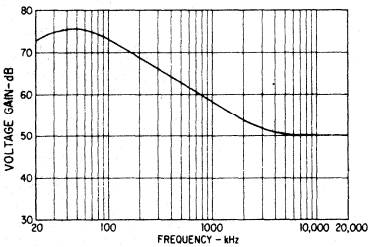
TYPICAL PERFORMANCE



Gain at 25 kHz	121 dB	without tuned circuits
Gain at 25 kHz	105 dB	with tuned circuits, measured at base of relay trans.
Sensitivity for:		
relay on at 26 kHz	7.8 μV	14 V supply
relay on at 26 kHz	5.1 μV	24 V supply
Noise output	25 mV	measured at the base of relay transistor.
Bandwidth 3 dB	1 kHz	
S/N Ratio	25 dB	at sensitivity Level

Figure 5. STEREO TAPE PREAMPLIFIER





TYPICAL PERFORMANCE

Gain at 1 kHz	60 dB
Output Voltage Swing	2.8 V rms
Power Consumption	30 mW

Note: For additional applications information, see Application Notes App 171 and App 175.

μA751C
DIFFERENTIAL VIDEO AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

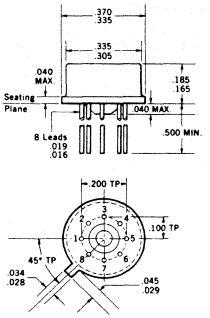
FEATURES
- **VOLTAGE GAIN 600**
- **200Ω INPUT LINE TERMINATION**
- **10 ns TYPICAL PROPAGATION DELAY**
- **NO FREQUENCY COMPENSATION REQUIRED**

GENERAL DESCRIPTION — The μA751C is a monolithic two-stage differential input differential output video amplifier constructed on a single silicon chip using the Fairchild Planar* epitaxial process. Internal series feedback is used for high gain and excellent gain stability. Internal sense line termination minimizes line reflections and eliminates the need for external termination components. External frequency compensation is not required. The device is particularly useful as a read amplifier in high-speed thin film memories. Other applications include general purpose video and pulse amplifiers where high gain and excellent gain stability are required. For applications where lower gain is required and where input termination is not desirable, see the μA733 data sheet.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±8 V
Differential Input Voltage	±2 V
Common Mode Input Voltage (Note 1)	±1 V
Output Current	7.5 mA
Internal Power Dissipation (Note 2)	250 mW
Operating Temperature Range	−0° to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 60 second time limit)	300°C

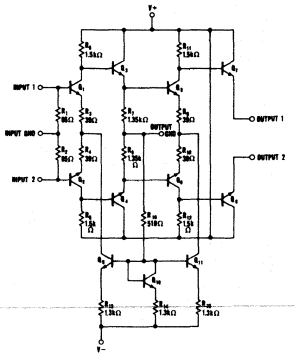
PHYSICAL DIMENSIONS
in accordance with
JEDEC (TO-99) outline



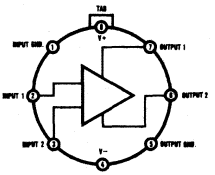
NOTES: Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.22 grams

ORDER PART NO. U5B7751393

SCHEMATIC DIAGRAM



CONNECTION DIAGRAMS
(TOP VIEW)



NOTES:
(1) Input voltage limited due to internal resistor between inputs and ground.
2) Rating applies for ambient temperatures to 70°C.

*Planar is a patented Fairchild process.

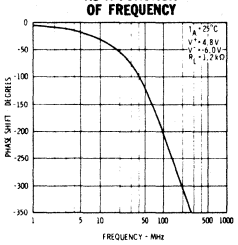
FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V^+ = +4.8$ V, $V^- = -6.0$ V unless otherwise specified)

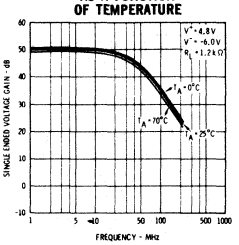
PARAMETER (see definitions, page 4)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Voltage Gain		375	600	825	
Bandwidth			30		MHz
Risetime	$V_{IN} = 1.0$ mV		12	25	ns
Propagation Delay	$V_{IN} = 1.0$ mV		10	20	ns
Differential Input Resistance		140	180	220	Ω
Input Capacitance			2.0		pF
Output Noise Voltage	BW = 20 Hz to 30 MHz		7.5		mVrms
Common Mode Rejection Ratio	$V_{CM} = 20$ mV		46		dB
Supply Voltage Rejection Ratio			60		dB
Output Offset Voltage			0.5	1.5	V
Output Common Mode Voltage		0.9	1.8	3.5	V
Output Voltage Swing			1.2		V_{pp}
Output Resistance			50		Ω
Positive Power Supply Current			11	14	mA
Negative Power Supply Current			9.0	12	mA

TYPICAL PERFORMANCE CURVES

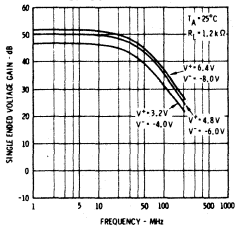
PHASE SHIFT AS A FUNCTION OF FREQUENCY



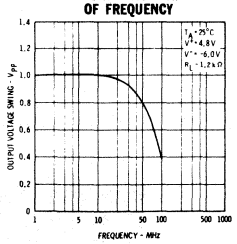
GAIN VERSUS FREQUENCY AS A FUNCTION OF TEMPERATURE



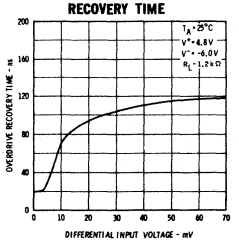
GAIN VERSUS FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY

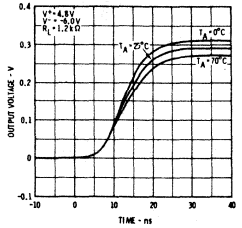


DIFFERENTIAL OVERDRIVE RECOVERY TIME

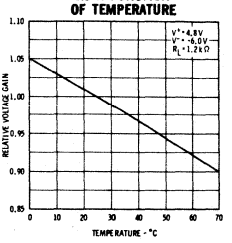


TYPICAL PERFORMANCE CURVES

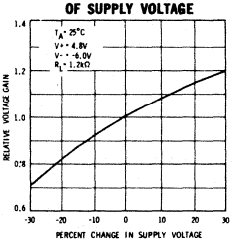
PULSE RESPONSE AS A FUNCTION OF TEMPERATURE



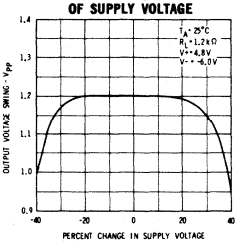
VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



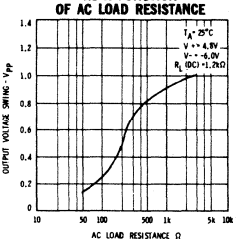
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



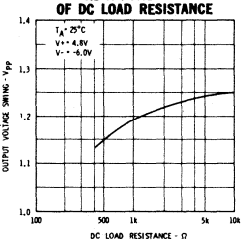
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



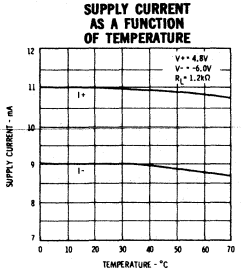
OUTPUT VOLTAGE SWING AS A FUNCTION OF AC LOAD RESISTANCE



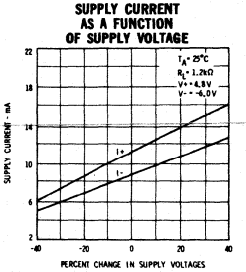
OUTPUT VOLTAGE SWING AS A FUNCTION OF DC LOAD RESISTANCE



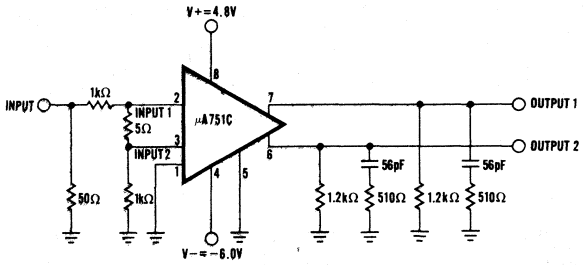
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



TEST CIRCUIT



NOTE: Circuit measures device performance with common mode and differential pulses simultaneously applied and typical output loading. Pin numbers are for TO-99 package.

DEFINITION OF TERMS

DIFFERENTIAL VOLTAGE GAIN — The ratio of the change in the differential output voltage to the change in voltage between the input terminals producing it.

BANDWIDTH — The frequency at which the differential gain is 3 dB below its low frequency value.

RISE TIME — The time required for an output voltage step to change from 10% to 90% of its final value.

PROPAGATION DELAY — The interval between the application of an input voltage step and its arrival at either output, measured at 50% of the final value.

INPUT RESISTANCE — The resistance seen between the two input terminals.

INPUT VOLTAGE RANGE — The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

COMMON MODE REJECTION RATIO — The ratio of a change in input common mode voltage to the resulting change in output offset voltage referred to the input.

SUPPLY VOLTAGE REJECTION RATIO — The ratio of a change in supply voltage to the resulting change in output offset voltage referred to the input.

OUTPUT OFFSET VOLTAGE — The difference between the voltages at the two output terminals with the inputs grounded.

OUTPUT COMMON MODE VOLTAGE — The average of the voltages at the two output terminals.

OUTPUT VOLTAGE SWING — The peak-to-peak output swing that can be obtained without distortion. This includes the unbalance caused by output offset voltage.

OUTPUT RESISTANCE — The resistance seen looking into either output terminal.

POWER SUPPLY CURRENT — The current required from the power supplies to operate the device with each output externally loaded with 1.2 kΩ.

μA754C
TV/FM SOUND SYSTEM
FAIRCHILD LINEAR INTEGRATED CIRCUITS

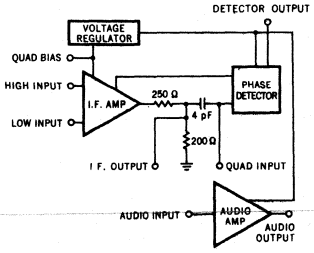
- **70 μV SENSITIVITY**
- **50 dB AM REJECTION**
- **INTERNALLY REGULATED SUPPLY**
- **SINGLE COIL QUADRATURE DETECTOR**
- **3 VRMS AUDIO OUTPUT**
- **LOW EXTERNAL COMPONENT COUNT**

GENERAL DESCRIPTION – The μA754C monolithic TV/FM Sound System consists of a four-stage limiting IF amplifier, doubly-balanced Quadrature FM Detector and a high output audio driver stage constructed on a single silicon chip using the Fairchild Planar* Epitaxial Process. Excellent sensitivity, high AM rejection and an internally regulated power supply coupled with low external component requirement make the μA754C suitable for a wide variety of applications including TV sound channels, line operated and automobile FM radios and mobile communications equipment. Other applications include analog multipliers, phase-locked loops, and synchronous detectors. (For μA754C applications information, and other Fairchild Communications Integrated Circuits, see listing on last page.)

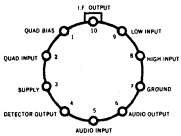
ABSOLUTE MAXIMUM RATINGS

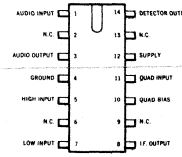
Voltage at any terminal must not exceed V_{SUPPLY}	
Supply Current	40 mA
Input Voltage (Note 1)	±5 Volts
Internal Power Dissipation (Note 2)	500 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range (TO-100 and Ceramic Dip)	−65°C to +150°C
(Silicone Dip)	−55°C to +125°C
Lead Temperature (TO-100 and Ceramic Dip, soldering, 60 seconds)	+300°C
(Silicone Dip, soldering, 10 seconds)	+260°C
Audio Output Short Circuit Duration	60 seconds

BLOCK DIAGRAM

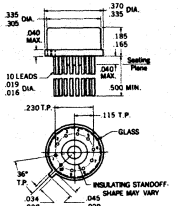


CONNECTION DIAGRAMS
(TOP VIEW)





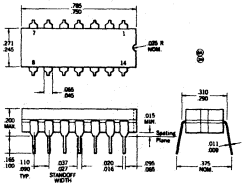
PHYSICAL DIMENSIONS
In accordance with JEDEC (TO-100) Outline



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.32 grams
Pin 7 connected to package with substrate

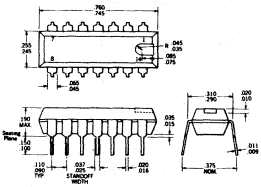
ORDER PART NO. U5E7754393

14 LEAD CERAMIC DIP



ORDER PART NO. U6A7754394

14 LEAD SILICONE DIP



ORDER PART NO. U9A7754394

(U6A pkg. may be supplied in lieu of U9A)

NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar

See Notes on page 2.

*Planar is a patented Fairchild process.

FAIRCHILD SEMICONDUCTOR

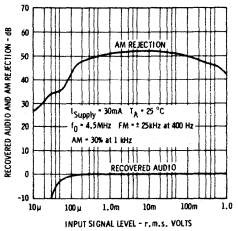
ELECTRICAL CHARACTERISTICS (T_A = 25°C, I^+ = 35 mA, unless otherwise specified)

PARAMETERS	CONDITIONS	TEST CIRCUIT	MIN.	TYP.	MAX.	UNITS
Static Characteristics						
Voltage at SUPPLY terminal		1	11.8	13	13.5	Volts
Supply Current	V_{supply} = 9.0 V	1	11.8	23	28	mA
Voltage at LOW INPUT terminal		1	1.2	1.4	1.8	Volts
Voltage at QUAD BIAS terminal		1	2.5	2.8	3.5	Volts
Voltage at I.F. OUTPUT terminal		1		0.7		Volts
Voltage at AUDIO INPUT terminal		1	1.2	1.5	1.7	Volts
Voltage at AUDIO OUTPUT terminal		1	4.8	5.7	7.5	Volts
Internal Power Dissipation		1	400	450	480	mW
Voltage at DETECTOR OUTPUT terminal		1	5.8	8.0	9.5	Volts
Short-circuit Current at AUDIO OUTPUT terminal		1		35	45	mA
Dynamic Characteristics of IF Amplifier & Detector at 4.5 MHz (FM = ±25 kHz at 400 Hz, V_{in} = 10 mV)						
Input Voltage for −3 dB Limiting		2		70	200	μV
IF Amplifier Voltage Gain		2	65	72		dB
A.M. Rejection	AM = 30% at 1 kHz	2	40	50		dB
Recovered Audio Voltage at Detector Output		2	250	450		mV
Total Harmonic Distortion		2		1.0	2.0	%
Detector Output Resistance				8.0		kΩ
Quad. Input Resistance				90		kΩ
Quad. Input Capacitance				7.0		pF
IF Amplifier Input Resistance				10		kΩ
IF Amplifier Input Capacitance				4.0		pF
IF Output Voltage		2	0.4	0.6		V_{p-p}
IF Output Resistance				125		Ω
IF Output Capacitance				7.0		pF
Dynamic Characteristics of IF Amplifier & Detector at 10.7 MHz (FM = ±75 kHz at 400 Hz, V_{in} = 10 mV)						
Input Voltage for −3 dB Limiting		2		200	300	μV
IF Amplifier Voltage Gain		2	55	62		dB
A.M. Rejection	AM = 30% at 1 kHz	2	35	45		dB
Recovered Audio Voltage at Detector Output		2	200	300		mV
Total Harmonic Distortion		2		0.5	2.0	%
Detector Output Resistance				8.0		kΩ
Quad. Input Resistance				100		kΩ
Quad. Input Capacitance				7.0		pF
IF Amplifier Input Resistance				10		kΩ
IF Amplifier Input Capacitance				4.0		pF
IF Output Voltage		2	0.4	0.6		V_{p-p}
IF Output Resistance				150		Ω
IF Output Capacitance				7.0		pF
Dynamic Characteristics of Audio Section (f = 1 kHz, R_s = 50 Ω)						
Open Loop Voltage Gain		3	12.5	16		V/V
Input Resistance			0.1	1.0		kΩ
Output Resistance				30		Ω
Maximum Output Voltage	THD = 5%, R_L = 2.4 kΩ	3	2.5	3.0		Vrms
Total Harmonic Distortion	V_{out} = 2 Vrms, R_L = 2.4 kΩ	3		0.8	3.0	%

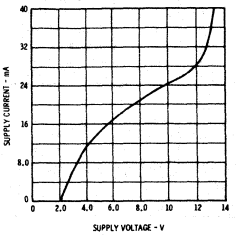
NOTES:
(1) Voltage applied from High Input to Low Input.
(2) Rating applies to an ambient temperature of +70°C. For TO-100, rating applies to an ambient temperature of 60°C; derate at 6.5 mW/°C above 60°C. For Silicone Dip, rating applies to an ambient temperature of 45°C; derate at 6.2 mW/°C above 45°C. Initial dissipation of 800 mW is permissible at an ambient temperature of +25°C for 30 seconds.

TYPICAL PERFORMANCE CURVES

RECOVERED AUDIO AND AM REJECTION AS A FUNCTION OF INPUT LEVEL

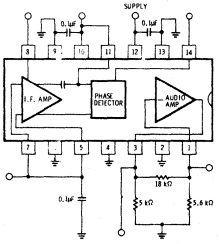


SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

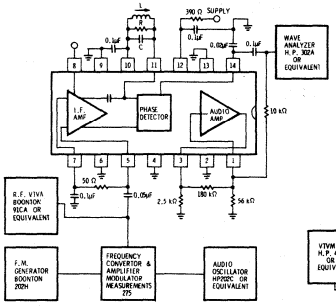


TEST CIRCUITS

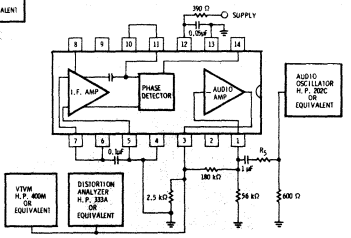
TEST CIRCUIT 1 STATIC CHARACTERISTICS



TEST CIRCUIT 2 DYNAMIC CHARACTERISTICS OF IF AMPLIFIER & QUADRATURE DETECTOR

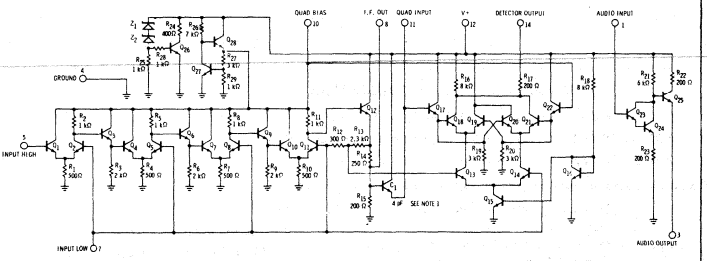


TEST CIRCUIT 3 AUDIO AMPLIFIER DYNAMIC CHARACTERISTICS



NOTE: For values of Quadrature Components — see Table 1 below

EQUIVALENT CIRCUIT



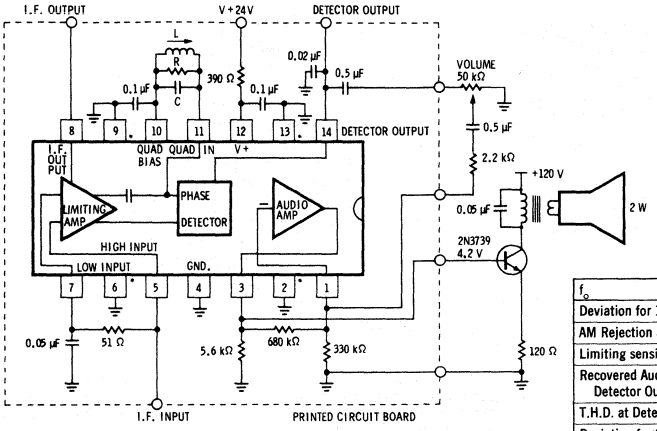
NOTES:
(1) C_J is a reverse-biased E-B Junction Capacitor.
(2) Pin numbers shown for Dual In-Line Package.

TABLE 1 VALUE OF QUADRATURE COMPONENTS

TABLE I

f_o	4.5 MHz	10.7 MHz
FM	± 25 kHz	75 kHz
L	10.4 μH	3.1 μH
C	120 pF	68 pF
Q_U	40	40
Q_L	30	15
Separation	300 kHz	1.1 MHz

TYPICAL APPLICATION



I.F. AMPLIFIER-DETECTOR 2W CLASS A OUTPUT STAGE

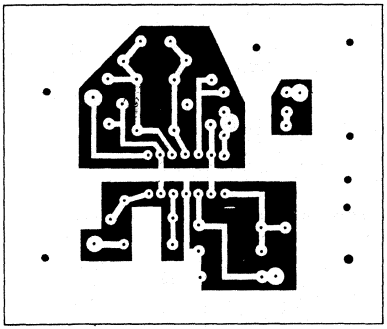
f_o	4.5	10.7	MHz
L	10.4	3.1	μH
C	120	68	pF
R	20 k	3.3 k	Ω

TYPICAL PERFORMANCE OF 2W CIRCUIT

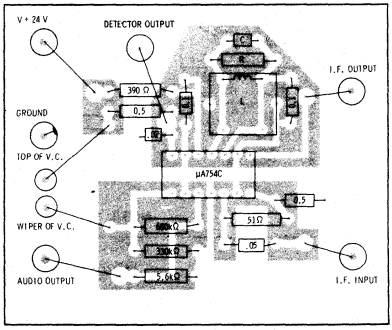
f_o	4.5 MHz	10.7 MHz
Deviation for 100% FM	±25 kHz	±75 kHz
AM Rejection at 1 mV	45 dB	35 dB
Limiting sensitivity	80 μV	150 μV
Recovered Audio at Detector Output	380 mV	160 mV
T.H.D. at Detector Output	1.0%	0.5%
Deviation for 2W output	±15 kHz	—

NOTES:
(1) Circuitry on printed circuit board shown inside dotted lines.
*(2) Unused pins should be grounded for shielding.

SUGGESTED CIRCUIT LAYOUT



COPPER SIDE



COMPONENT SIDE

μA754C APPLICATIONS INFORMATION

APP NOTE 190 – The μA754C TV/FM Sound System
APP BRIEF 152 – Quadrature FM Detectors Using Ceramic Filters
APP BRIEF 153 – Applications of the μA754C

For information on other Fairchild Communications Integrated Circuits, see the following data sheets:

RF/IF Limiting Amp – μA703C
RF/IF Limiting Amp – μA703D
Fixed Gain, Low Distortion Amp – μA716C
High Frequency Communication System – μA719C
FM Stereo Multiplex Decoder – μA729
FM Stereo Multiplex Decoder – μA732
Dual Low Noise, High Gain Op-Amp – μA739C
Dual AC Amp – μA745
Color TV Chroma Demodulator – μA746
Dual AC Amplifier – μA749D
Gain Controlled IF Amp – μA757C
FM Stereo Multiplex Decoder – μA767
Color TV Chroma Subcarrier Regenerator – μA780
Color TV Chroma IF – μA781
TV Sound System – μA784, μA3065
TV Signal Processing Circuit – μA785
P.A.L. Color TV Chroma Demodulator – μA786
Balanced Modulator-Demodulator – μA796C
TV Automatic Fine Tuning Circuit – μA3064

μA757C
GAIN CONTROLLED IF AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

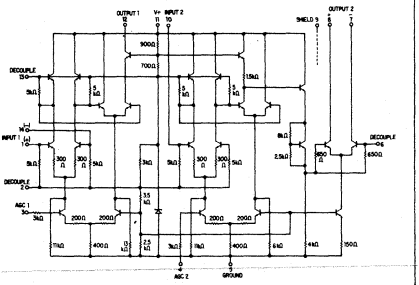
GENERAL DESCRIPTION — The μA757C is a high performance, gain-controlled IF amplifier constructed on a silicon chip using the Fairchild Planar* epitaxial process. The amplifier contains two sections which may be operated independently, or in cascade, from audio frequencies to 25 MHz. The μA757C is intended primarily as a gain-controlled, intermediate-frequency amplifier in AM and FM communications receivers. It also has excellent performance when operated in FM receivers as a limiting-amplifier. For full temperature range operation (−55°C to +125°C) see the μA757 data sheet. (Note 1).

- **70 dB GAIN AT 10.7 MHz**
- **70 dB AGC RANGE AT 10.7 MHz**
- **300 mV SIGNAL HANDLING CAPABILITY AT INPUT**
- **CONSTANT INPUT AND OUTPUT IMPEDANCE WITH AGC**
- **STABLE GAIN WITH SUPPLY VOLTAGE AND TEMPERATURE AT ALL LEVELS OF GAIN REDUCTION**

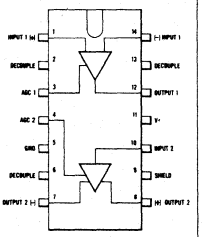
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+15 V
Voltage at any Output Terminal	+24 V
Voltage at either AGC Terminal (Note 2)	±12 V
Differential Voltage at either Input (Pins 1 and 14, Pins 2 and 10)	±5 V
Internal Power Dissipation	400 mW
Storage Temperature Range	−55°C to +125°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 10 seconds)	+260°C

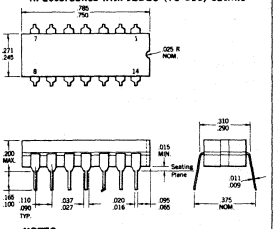
EQUIVALENT CIRCUIT



CONNECTION DIAGRAM
(TOP VIEW)



PHYSICAL DIMENSIONS
In accordance with JEDEC (TO-116) outline



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams

ORDER PART NO. U6A7757393

NOTES:
(1) For other Fairchild Communications Integrated Circuits, see list on last page.
(2) For supply voltages less than +12 V, the absolute maximum voltage at either AGC Terminal is equal to the supply voltage.

*Planar is a patented Fairchild process.

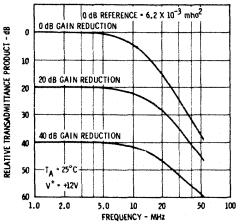
FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS ($V^+ = +12$ V, $T_A = +25°C$, unless otherwise specified)

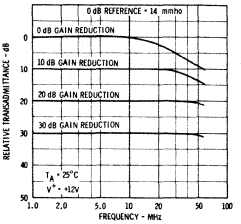
PARAMETERS	CONDITIONS	TEST CIRCUIT	MIN.	TYP.	MAX.	UNITS
Supply Current	$V_{AGC\ 1,2} = +1.0$ V	1		14	17	mA
	$V_{AGC\ 1,2} = +3.0$ V			18	22	mA
Internal Power Dissipation	$V_{AGC\ 1,2} = +1.0$ V	1		170	210	mW
	$V_{AGC\ 1,2} = +3.0$ V			220	270	mW
Voltage Gain at no Gain Reduction	$V_{AGC\ 1,2} = +1.0$ V, f = 500 kHz	2	65	74		dB
	$V_{AGC\ 1,2} = +1.0$ V, f = 10.7 MHz	2	60	70		dB
Voltage Gain at Partial Gain Reduction	$V_{AGC\ 1,2} = +1.7$ V, f = 500 kHz	2	20	39	46	dB
	$V_{AGC\ 1,2} = +1.7$ V, f = 10.7 MHz	2		37		dB
Voltage Gain at Full Gain Reduction	$V_{AGC\ 1,2} = +3.0$ V, f = 500 kHz	2		2.0	10	dB
	$V_{AGC\ 1,2} = +3.0$ V, f = 10.7 MHz	2		1.0	8	dB
Current into either AGC Terminal	$V_{AGC\ 1,2} = +3.0$ V	1		15	50	μA
Gain Reduction Sensitivity	$V_{AGC\ 1,2} = +1.7$ V, f = 500 kHz	2		50		dB/V
Input Voltage for −3 dB Limiting at Output	$V_{AGC\ 1,2} = +1.0$ V, f = 500 kHz	2		0.5		mV
Intermodulation Products	Two-tone signal $f_1 = 500$ kHz, $e_i = 100$ mV $f_2 = 510$ kHz, $e_2 = 100$ mV $I_{OUT} = 1$ mA p-p	2		−50		dB
SECTION 1						
Input Resistance at either Input Terminal	$V_{AGC\ 1} = +1.0$ V, f = 10.7 MHz		3.0	5.0		kΩ
	$V_{AGC\ 1} = +3.0$ V, f = 10.7 MHz			4.5		kΩ
Input Capacitance at either Input Terminal	$V_{AGC\ 1} = +1.0$ V, f = 10.7 MHz			2.5		pF
	$V_{AGC\ 1} = +3.0$ V, f = 10.7 MHz			2.2		pF
Output Resistance	$V_{AGC\ 1} = +1.0$ V, f = 10.7 MHz			100		kΩ
	$V_{AGC\ 1} = +3.0$ V, f = 10.7 MHz			100		kΩ
Output Capacitance	$V_{AGC\ 1} = +1.0$ V, f = 10.7 MHz			2.6		pF
	$V_{AGC\ 1} = +3.0$ V, f = 10.7 MHz			2.2		pF
Forward Transadmittance	$V_{AGC\ 1} = +1.0$ V, f = 500 kHz			14		mmho
	$V_{AGC\ 1} = +1.0$ V, f = 10.7 MHz			13		mmho
Peak-to-Peak Output Current	$V_{AGC\ 1} = +3.0$ V, f = 500 kHz Output in full limiting		.25	0.4		mA
Output Saturation Voltage	$I_{OUT} = 0.1$ mA, $V_{AGC\ 1} = +3.0$ V			8.0	9.0	Volts
Noise Figure	$R_S = 1.0$ kΩ, f = 10.7 MHz			8.0		dB
Noise Figure	$R_S = 1.0$ kΩ, f = 500 kHz			8.0		dB
Interfering Signal Voltage at Input for 1.0% Cross Modulation	Carrier signal, $f_c = 500$ kHz Interfering signal, $f_i = 510$ kHz $I_{OUT} = 0.5$ mA p-p, $V_{AGC\ 1} = +1.0$ V			15		mV
SECTION 2						
Input Resistance	$V_{AGC\ 2} = +1.0$ V, f = 10.7 MHz		3.0	5.0		kΩ
	$V_{AGC\ 2} = +3.0$ V, f = 10.7 MHz			4.5		kΩ
Input Capacitance	$V_{AGC\ 2} = +1.0$ V, f = 10.7 MHz			2.5		pF
	$V_{AGC\ 2} = +3.0$ V, f = 10.7 MHz			2.2		pF
Output Resistance at either Output Terminal	$V_{AGC\ 2} = +1.0$ V, f = 10.7 MHz			26		kΩ
	$V_{AGC\ 2} = +3.0$ V, f = 10.7 MHz			20		kΩ
Output Capacitance at either Output Terminal	$V_{AGC\ 2} = +1.0$ V, f = 10.7 MHz			2.2		pF
	$V_{AGC\ 2} = +3.0$ V, f = 10.7 MHz			2.5		pF
Forward Transadmittance	$V_{AGC\ 2} = +1.0$ V, f = 500 kHz			440		mmho
	$V_{AGC\ 2} = +1.0$ V, f = 10.7 MHz			280		mmho
Quiescent Output Current at either Output Terminal	$V_{AGC\ 2} = +3.0$ V, f = 500 kHz		1.7	2.4	3.5	mA
Peak-to-Peak Current at either Output Terminal	$V_{AGC\ 2} = +3.0$ V, f = 500 kHz Output in full limiting		3.8	4.8	7.0	mA
Output Saturation Voltage at either Output Terminal	$I_{OUT} = 1.0$ mA, $V_{AGC\ 2} = +3.0$ V			5.0	6.0	Volts
Power Supply Sensitivity	$V_S = 12$ V to 15 V					
	0 dB Gain Reduction			0.5		dB/V
	30 dB Gain Reduction			0.8		dB/V
	60 dB Gain Reduction			1.0		dB/V

TYPICAL PERFORMANCE CURVES

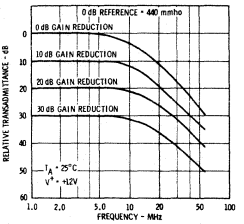
PRODUCT OF SECTIONS 1 AND 2 FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



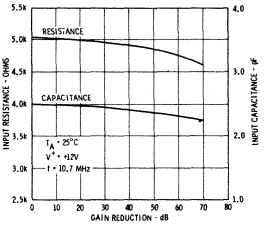
SECTION 1 FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



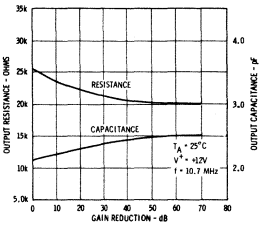
SECTION 2 FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



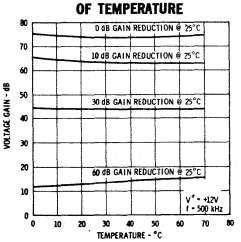
SECTION 1 AND 2 INPUT RESISTANCE AND CAPACITANCE AS A FUNCTION OF GAIN REDUCTION



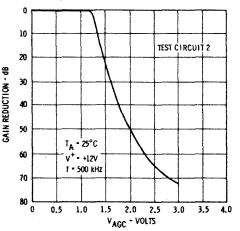
SECTION 2 OUTPUT RESISTANCE AND CAPACITANCE AS A FUNCTION OF GAIN REDUCTION



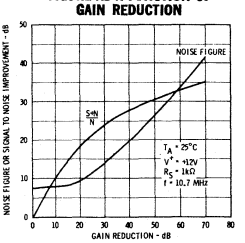
VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



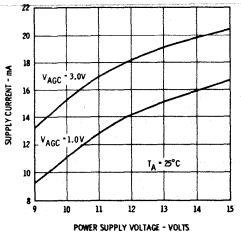
GAIN REDUCTION AS A FUNCTION OF GAIN CONTROL VOLTAGE



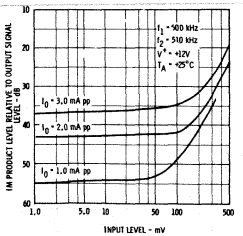
SIGNAL TO NOISE RATIO IMPROVEMENT AND NOISE FIGURE AS A FUNCTION OF GAIN REDUCTION



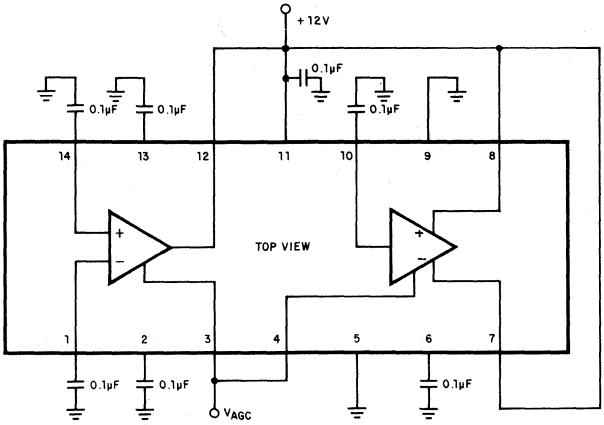
POWER SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



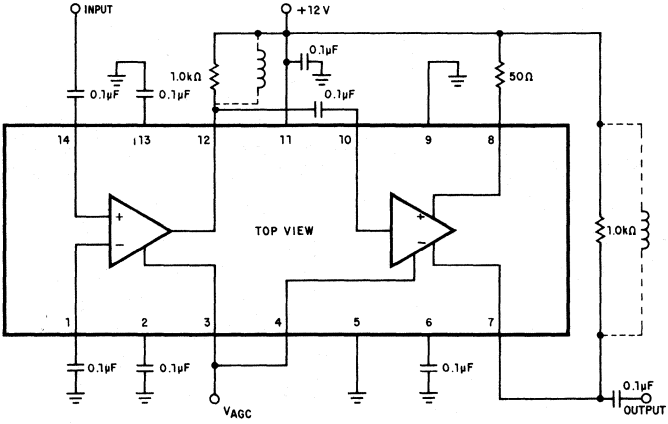
TWO TONE IM DISTORTION PRODUCTS AS A FUNCTION OF INPUT SIGNAL LEVEL



TEST CIRCUIT 1



TEST CIRCUIT 2



NOTE:
For 10.7 MHz measurements, interstage capacitance and Section 2 output capacitance are tuned out.

FOR INFORMATION ON OTHER FAIRCHILD COMMUNICATIONS INTEGRATED CIRCUITS, SEE THE FOLLOWING DATA SHEETS:

RF/IF LIMITING AMP — μA703C
RF/IF LIMITING AMP — μA703D
FIXED GAIN, LOW DISTORTION AMP — μA716C
HIGH FREQUENCY COMMUNICATIONS SYSTEM μA719C
FM STEREO MULTIPLEX DECODER μA729, μA732
DUAL LOW NOISE HIGH GAIN OP-AMP μA739C
DUAL AC AMP μA745
COLOR TV CHROMA DEMODULATOR μA746
DUAL OPERATIONAL AMPLIFIER μA749D
TV/FM SOUND SYSTEM μA754C
BALANCED MODULATOR-DEMODULATOR μA796C

μA760

HIGH SPEED DIFFERENTIAL COMPARATOR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA760 is a differential voltage comparator offering considerable speed improvement over the μA710 family and operation from symmetric supplies of from ±4.5 volts to ±6.5 volts. Complementary outputs are TTL compatible with a minimum sink capability of two gate loads.

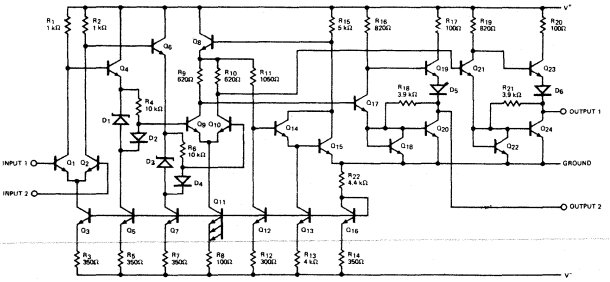
FEATURES

- **GUARANTEED HIGH SPEED**
- **GUARANTEED DELAY MATCHING ON BOTH OUTPUTS**
- **COMPLEMENTARY TTL COMPATIBLE OUTPUTS**
- **HIGH SENSITIVITY**
- **USES STANDARD SUPPLY VOLTAGES**

ABSOLUTE MAXIMUM RATINGS

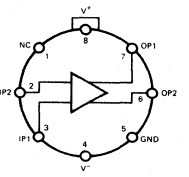
Positive Supply Voltage		+8 V
Negative Supply Voltage		−8 V
Peak Output Current		10 mA
Differential Input Voltage		±5 V
Input Voltage		$\pm V_S$
Internal Power Dissipation (Note 1)	Metal Can	500 mW
	Ceramic DIP	600 mW
	Mini DIP	350 mW
Operating Temperature Range		
Military (312 Grade)		−55°C to 125°C
Commercial (393 Grade)		0°C to 70°C
Storage Temperature Range		
Metal Can and DIP		−65°C to 150°C
Mini DIP		−55°C to 125°C

EQUIVALENT CIRCUIT



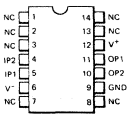
Notes: See Page 3.

CONNECTION DIAGRAM
8 LEAD METAL CAN
(TOP VIEW)



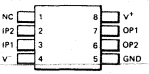
ORDER PART NOS.: PRODUCT CODE
U5B7760312
U5B7760393

14 LEAD DIP
(TOP VIEW)



ORDER PART NOS.: PRODUCT CODE
U6A7760312
U6A7760393

MINI DIP
(TOP VIEW)



ORDER PART NO.: PRODUCT CODE
U9T7760393

FAIRCHILD SEMICONDUCTOR

312 GRADE

ELECTRICAL CHARACTERISTICS (V_S = ±4.5V to ±6.5V, T_A = –55°C to +125°C, T_A = 25°C for typical figures unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 200\Omega$		1.0	6.0	mV
Input Offset Current			0.5	7.5	μA
Input Bias Current			8.0	60	μA
Output Resistance	$V_{OUT} = V_{OH}$		100		Ω
Response Time	Note 2, T_A = 25°C		18	30	ns
	Note 3, T_A = 25°C			25	ns
	Note 4		16		ns
Response Time Difference between outputs					
$t_{pd+1} - t_{pd-2}$	Note 2, T_A = 25°C			5.0	ns
$t_{pd+2} - t_{pd-1}$	Note 2, T_A = 25°C			5.0	ns
$t_{pd+1} - t_{pd+2}$	Note 2, T_A = 25°C			7.5	ns
$t_{pd-1} - t_{pd-2}$	Note 2, T_A = 25°C			7.5	ns
Input Resistance	f = 1 MHz		12		kΩ
Input Capacitance	f = 1 MHz		8.0		pF
Average Temperature Coefficient of Input Offset Voltage	R_S = 50Ω, T_A = –55°C to T_A = +125°C		3.0		μV/°C
Average Temperature Coefficient of Input Offset Current	T_A = 25°C to T_A = +125°C T_A = 25°C to T_A = –55°C		2.0 7.0		nA/°C nA/°C
Input Voltage Range	V_S = ±6.5V	±4.0	±4.5		V
Differential Input Voltage Range			±5.0		V
Positive Output Level	$0 \leq I_{OUT} \leq 5.0$ mA				
	V_S = ±5.0V	2.4	3.2		V
	I_{OUT} = 80 μA, V_S = ±4.5V	2.4	3.0		V
Negative Output Level	I_{SINK} = 3.2 mA		0.25	0.4	V
Positive Supply Current	V_S = ±6.5V		18	32	mA
Negative Supply Current	V_S = ±6.5V		9.0	16	mA

393 GRADE

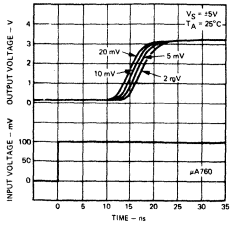
ELECTRICAL CHARACTERISTICS (V_S = ±4.5V to ±6.5V, T_A = 0°C to +70°C, T_A = 25°C for typical figures unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 200\Omega$		1.0	6.0	mV
Input Offset Current			0.5	7.5	μA
Input Bias Current			8.0	60	μA
Output Resistance	$V_{OUT} = V_{OH}$		100		Ω
Response Time	Note 2, T_A = 25°C		18	30	ns
	Note 3, T_A = 25°C			25	ns
	Note 4		16		ns
Response Time Difference between outputs					
$t_{pd+1} - t_{pd-2}$	Note 2, T_A = 25°C			5.0	ns
$t_{pd+2} - t_{pd-1}$	Note 2, T_A = 25°C			5.0	ns
$t_{pd+1} - t_{pd+2}$	Note 2, T_A = 25°C			10	ns
$t_{pd-1} - t_{pd-2}$	Note 2, T_A = 25°C			10	ns
Input Resistance	f = 1 MHz		12		kΩ
Input Capacitance	f = 1 MHz		8.0		pF
Average Temperature Coefficient of Input Offset Voltage	R_S = 50Ω, T_A = −55°C to T_A = +125°C		3.0		μV/°C
Average Temperature Coefficient of Input Offset Current	T_A = 25°C to T_A = +70°C		5.0		nA/°C
	T_A = 25°C to T_A = 0°C		10		nA/°C
Input Voltage Range	V_S = ±6.5V	±4.0	±4.5		V
Differential Input Voltage Range			±5.0		V
Positive Output Level	$0 \leq I_{OUT} \leq 5.0$ mA				
	V_S = ±5.0V	2.4	3.2		V
	I_{OUT} = 80 μA, V_S = ±4.5V	2.5	3.0		V
Negative Output Level	I_{SINK} = 3.2 mA		0.25	0.4	V
Positive Supply Current	V_S = ±6.5V		18	34	mA
Negative Supply Current	V_S = ±6.5V		9.0	16	mA

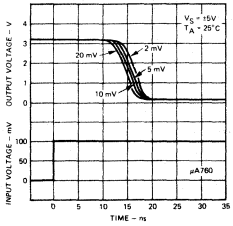
NOTES:
(1) Military ratings (312 grade) apply for case temperature to 125°C; derate linearly at 5.6 mW/°C for ambient temperatures above +75°C. Commercial ratings (393 grade) apply for case temperatures to +70°C.
(2) Response time measured from the 50% point of a 30 mVp-p 10 MHz sinusoidal input to the 50% point of the output.
(3) Response time measured from the 50% point of a 2 Vp-p 10 MHz sinusoidal input to the 50% point of the output.
(4) Response time measured from the start of a 100 mV input step with 5 mV overdrive to the time when the output crosses the logic threshold.

TYPICAL PERFORMANCE CURVES

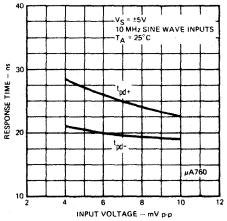
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



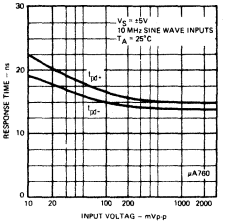
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



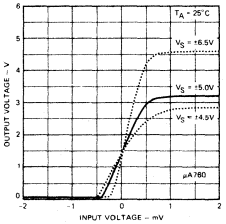
RESPONSE TIME AS A FUNCTION OF INPUT VOLTAGE



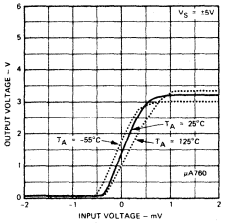
RESPONSE TIME AS A FUNCTION OF INPUT VOLTAGE



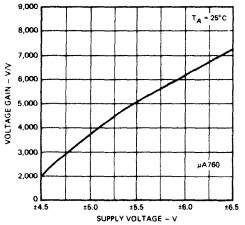
VOLTAGE TRANSFER CHARACTERISTIC



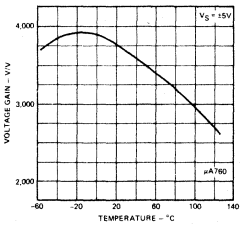
VOLTAGE TRANSFER CHARACTERISTIC



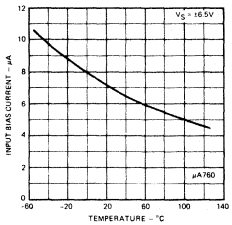
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



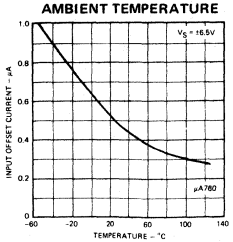
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



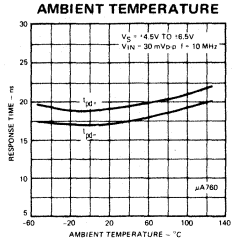
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



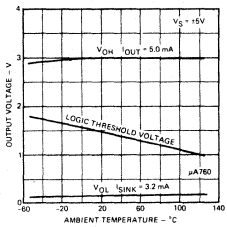
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



RESPONSE TIME AS A FUNCTION OF AMBIENT TEMPERATURE

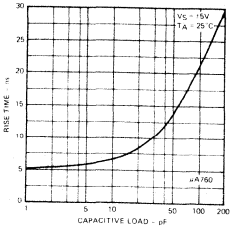


OUTPUT VOLTAGE LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE

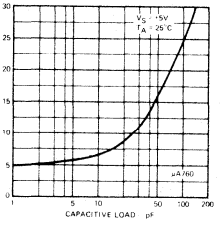


TYPICAL PERFORMANCE CURVES (Cont.)

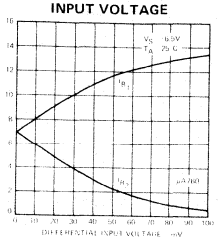
RISE TIME AS A FUNCTION OF CAPACITIVE LOAD



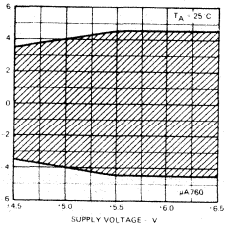
FALL TIME AS A FUNCTION OF CAPACITIVE LOAD



INPUT BIAS CURRENT AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE



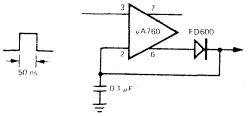
COMMON MODE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



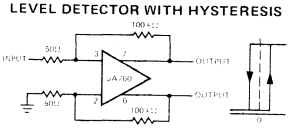
APPLICATIONS

Pin numbers shown are only for Metal Can and Mini DIP.

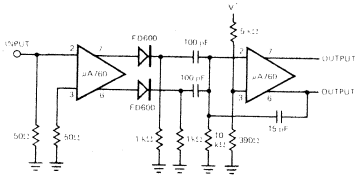
FAST POSITIVE PEAK DETECTOR



LEVEL DETECTOR WITH HYSTERESIS

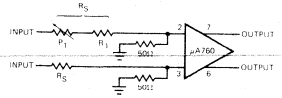


ZERO CROSSING DETECTOR



Total delay = 30 ns
Input frequency = 300 Hz to 3 MHz
Minimum input voltage = 20 mVp-p

LINE RECEIVER WITH HIGH COMMON MODE RANGE



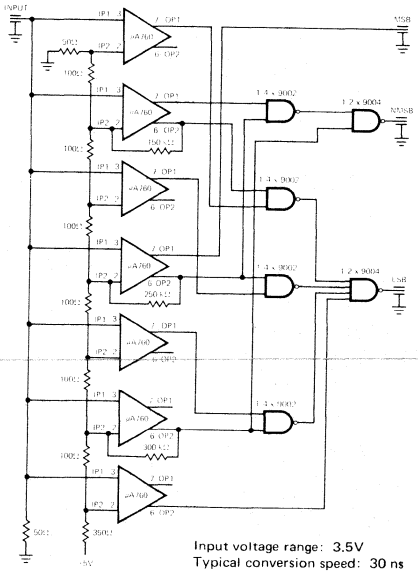
Common mode range = $\pm 4 \times \frac{RS}{50}$ V

Differential Input sensitivity = $5 \times \frac{RS}{50}$ mV

P_1 must be adjusted for optimum common mode rejection.

For $R_S = 200\Omega$
Common mode range = ±16V
Sensitivity = 20 mV

HIGH SPEED 3-BIT A/D CONVERTER



Input voltage range: 3.5V
Typical conversion speed: 30 ns

DEFINITION OF TERMS

INPUT OFFSET VOLTAGE – The minimum differential input voltage at which one output will be at the positive output level while the other is at the negative output level when each output is loaded with two TTL gates.

POSITIVE OUTPUT LEVEL – The DC output voltage in the positive direction with a differential input signal greater than the input offset voltage.

NEGATIVE OUTPUT LEVEL – The DC output voltage in the negative direction with a differential input signal greater than the input offset voltage.

INPUT BIAS CURRENT – The average of the two input currents.

INPUT OFFSET CURRENT – The difference between the two input currents.

INPUT VOLTAGE RANGE – The range of voltage on the input terminals for which the comparator will operate normally.

OUTPUT RESISTANCE – The resistance at either output terminal with a differential input voltage of suitable magnitude and sign to set the output at the positive output level.

RESPONSE TIME – The interval between the application of an input signal and the appearance of a signal at the comparator outputs. See Notes 2, 3 and 4.

INPUT RESISTANCE – The resistance at either input terminal with the other grounded.

INPUT CAPACITANCE – The capacitance at either input terminal with the other grounded.

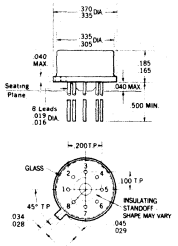
POSITIVE SUPPLY CURRENT – The current required from the positive power supply to operate the device with no load.

NEGATIVE SUPPLY CURRENT – The current required from the negative power supply to operate the device with no load.

PHYSICAL DIMENSIONS

METAL CAN
5B PACKAGE

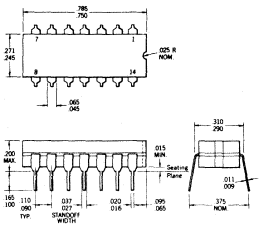
In accordance with JEDEC (TO-99) outline.



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.22 grams

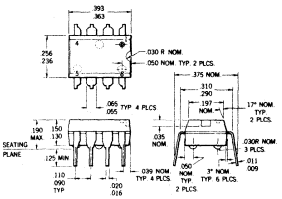
CERAMIC DIP
6A PACKAGE

In accordance with JEDEC (TO-116) outline.



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams

MINI DIP
9T PACKAGE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 0.6 gram
Package material is silicone

FOR INFORMATION ON OTHER FAIRCHILD COMPARATORS AND INTERFACE CIRCUITS SEE THE FOLLOWING DATA SHEETS:

COMPARATORS
- HIGH SPEED – μA710
- DUAL HIGH SPEED – μA711
- DUAL POWER – μA750
- PRECISION – μA734

A/D AND D/A CONVERTERS
- 10-BIT CURRENT SOURCE – μA722
- 4-BIT CURRENT SOURCE – μA9650*
- 10-BIT A/D CONVERTER – SH8091
- 10-BIT D/A CONVERTER – SH8090
- 10-BIT LOW COST D/A – SH1500*

*To be announced

SENSE AMPLIFIERS
- DUAL – μA761, μA7524, μA7525

POWER DRIVERS
- DUAL, GENERAL PURPOSE – μA75450, μA75451
- LAMP AND RELAY DRIVERS – SH2001, SH2002, SH2200

LINE DRIVERS AND RECEIVERS
- DUAL DIFFERENTIAL – μA9614, μA9615
- EIA RS232C TRIPLE – μA9616*, μA9617*

INTERFACE
- MOS/TTμL – μA9624, μA9625
- UNIVERSAL MOS CLOCK DRIVER – SH2011*
- SILICON GATE MOS CLOCK DRIVER – SH2010*

μA761C

TWO CHANNEL CORE MEMORY SENSE AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

- **±2 mV THRESHOLD VARIATION**
- **25 ns PROPAGATION DELAY**
- **DUAL INDEPENDENT STROBES**
- **TTμL COMPATIBLE**

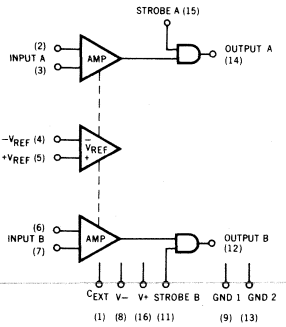
GENERAL DESCRIPTION — The μA761C is a Two Channel Core Memory Sense Amplifier constructed on a single silicon chip using the patented Fairchild Planar* epitaxial process. It can be used for small (1K to 8K words) memories as well as larger memory systems. The device is suitable for small core sizes facilitating very fast memory cycle times. The μA761C features tight threshold accuracy, fast response time, and independent strobe selection. Unit to unit variations are minimized so that individual adjustments of threshold and strobe timing are not necessary.

All logic inputs and outputs are fully TTμL compatible. The μA761C can be combined with Fairchild MSI Quad Latch 9314 to provide complete memory data register capability.

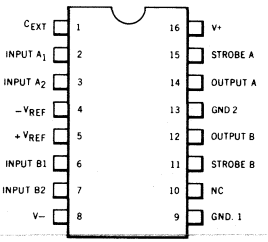
ABSOLUTE MAXIMUM RATINGS

Differential Input Voltage	±5.0 V
Supply Voltage	±7.0 V
Logic Input Voltage	+5.5 V
Power Dissipation (Note 1) 6M Package	400 mW
7B Package	500 mW
Storage Temperature 6M Package	−55°C to +125°C
7B Package	−65°C to +150°C
Operating Temperature	0°C to +70°C
Lead Temperature (6M Package, Soldering 10 seconds)	+260°C
(7B Package, Soldering 60 seconds)	+300°C
Signal Input	±3.0 V
Reference Input	±3.0 V

BLOCK DIAGRAM

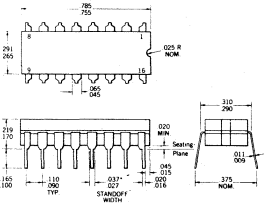


CONNECTION DIAGRAM



PHYSICAL DIMENSIONS

16 Lead Ceramic Dual In-Line



NOTES:

All dimensions in inches

Leads are intended for insertion in hole rows on .300" centers

They are purposely shipped with "positive" misalignment to facilitate insertion

Board-drilling dimensions should equal your practice for .020 inch diameter lead

Leads are tin plated kovar

Package weight is 2.2 grams

The .027 / .037 dimensions does not apply to the corner leads

ORDER PART NO. U7B7761392

Note 1: Rating applies for Ambient Temperature to 70°C.

*Planar is a patented Fairchild process.

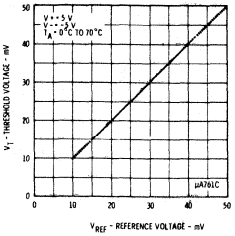
FAIRCHILD SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS ($V^+ = 5.0$ V, $V^- = -5.0$ V, 0°C to +70°C either input unless otherwise specified)

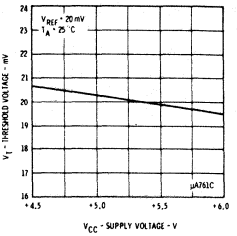
PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Threshold Voltage Range					
Minimum			10		mV
Maximum			50		mV
Threshold Uncertainty			±2.0		mV
Differential Input Threshold Voltage	$V_{ref} = 15$ mV	11		19	mV
	$V_{ref} = 40$ mV	36		44	mV
Differential Input Bias Current	$V_{IND} = 0$ mV		15	75	μA
Differential Input Offset Current	$V_{IND} = 0$ mV		1.0	10	μA
Differential Input Impedance	f = 1.0 kHz		2.5		kΩ
Positive Supply Current	$T_A = 25°C$		25	38	mA
Negative Supply Current	$T_A = 25°C$		10	16	mA
Output Short Circuit Current	$V^+ = 5.25$ V, $V^- = -5.25$ V	2.1		3.5	mA
LOGIC INPUT/OUTPUT CONDITIONS (See Fig. 2)					
Output Voltage Logical "1"	I Load = 400 μA $V_{in(1)}$ STROBE = 2.0 V $V_{in(0)}$ STROBE = 0.8 V $V^+ = 4.75$ V $V^- = -4.75$ V	2.4	3.9		V
Output Voltage Logical "0"	I Sink = 16 mA $V_{in(0)}$ STROBE = 0.8 V $V^+ = 4.75$ V $V^- = -4.75$ V		0.25	0.4	V
Logical "1" Input (Strobe Inputs)	$V_{in(0)}$ STROBE = 0.8 V $V^+ = 4.75$ V $V^- = -4.75$ V	2.0			V
Logical "0" Input (Strobe Inputs)	$V_{in(1)}$ STROBE = 2.0 V $V^+ = 4.75$ V $V^- = -4.75$ V			0.8	V
Logical "0" Input Current (Strobe Inputs)	$V_{in(0)}$ STROBE = 0.4 V $V^+ = 5.25$ V $V^- = -5.25$ V		−1.0	−1.6	mA
Logical "1" Input Current (Strobe Inputs)	$V_{in(1)}$ STROBE = 2.4 V $V^+ = 5.25$ V $V^- = -5.25$ V			40	μA
Logical "1" Input Current (Strobe Inputs)	$V_{in(1)}$ STROBE = V^+ $V^+ = 5.25$ V $V^- = -5.25$ V			1.0	mA
A.C. CHARACTERISTICS (Either amplifier) $T_A = 25°C$					
Minimum "1" Test (See Fig. 3)	$V_{ref} = 15$ mV $V_{IND\ (1)} = 24$ mV	2.0			V
Maximum "0" Test (See Fig. 3)	$V_{ref} = 15$ mV $V_{IND\ (0)} = 10$ mV			1.0	V
Common Mode Input Firing Voltage	$t_r = t_f \leq 15$ ns $t_p = 50$ ns		±3.0		V
Differential Input Overload Recovery Time	$V_{in} + 2.0$ V, $t_r = t_f = 20$ ns		20		ns
Common Mode Input Overload Recovery Time	$V_{inCM} = \pm 2.0$ V, $t_r = t_f = 20$ ns		20		ns
Input to Output Delay (See Figure 1)	t_{pd} (1) D		25	40	ns
	t_{pd} (0) D		35	65	ns
Strobe to Output Delay (See Figure 1)	t_{pd} (1) STROBE		15	30	ns
	t_{pd} (0) STROBE		25	40	ns

TYPICAL PERFORMANCE CURVES

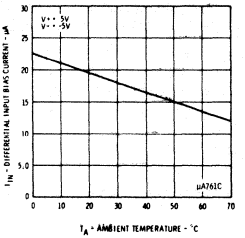
THRESHOLD VOLTAGE VERSUS REFERENCE VOLTAGE



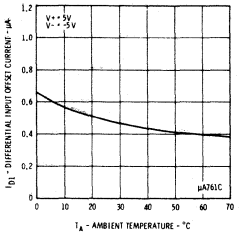
THRESHOLD VOLTAGE VERSUS SUPPLY VOLTAGE



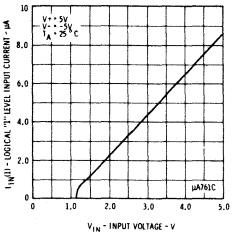
DIFFERENTIAL-INPUT BIAS CURRENT VERSUS AMBIENT TEMPERATURE



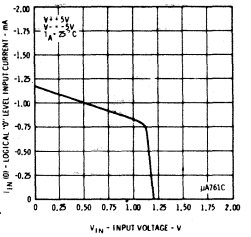
DIFFERENTIAL-INPUT OFFSET CURRENT VERSUS AMBIENT TEMPERATURE



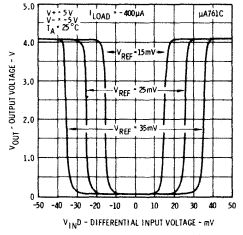
LOGICAL "1" LEVEL INPUT CURRENT VERSUS INPUT VOLTAGE



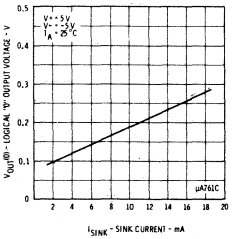
LOGICAL "0" LEVEL INPUT CURRENT VERSUS INPUT VOLTAGE



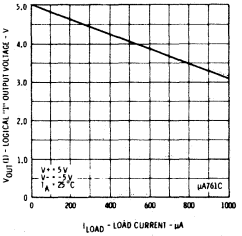
OUTPUT VOLTAGE VERSUS DIFFERENTIAL INPUT VOLTAGE



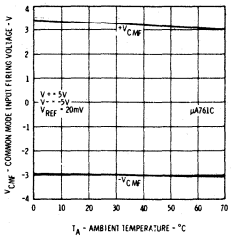
LOGICAL "0" OUTPUT VOLTAGE VERSUS SINK CURRENT



LOGICAL "1" OUTPUT VOLTAGE VERSUS LOAD CURRENT



COMMON-MODE FIRING VOLTAGE VERSUS AMBIENT TEMPERATURE



DEFINITION OF TERMS:

THRESHOLD VOLTAGE — The typical referred to input voltage which determines whether an input is a "1" or a "0". A signal whose magnitude is greater than the threshold level is sensed as a logic "1" and a signal whose magnitude is less as a "0".

THRESHOLD UNCERTAINTY — With all sense amps sharing the same input threshold setting, all input signals greater than the nominal threshold plus the uncertainty shall be sensed as a "1" and all input signals less than the nominal threshold less the uncertainty as a "0". This includes unit to unit, power supply and temperature variations.

PROPAGATION DELAY — The time delay measured from input threshold to output logic threshold with the strobe enabled.

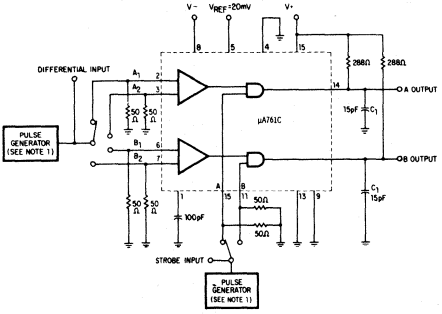
STROBE DELAY — The time delay measured from strobe to output logic threshold with a signal present exceeding the input threshold.

COMMON MODE RECOVERY TIME — The time from the turn off of the CM signal to the analog input threshold of the earliest sense line pulse signal that can be processed normally. Processed normally refers to bi-polar signals greater than or less than the input threshold with a corresponding proper output.

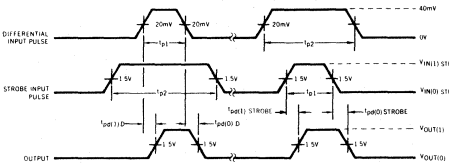
COMMON MODE FIRING VOLTAGE — The CM input voltage that exceeds the dynamic range of the inputs with strobe enabled resulting in the output switching states.

FIG. 1 PROPAGATION DELAY

TEST CIRCUITS

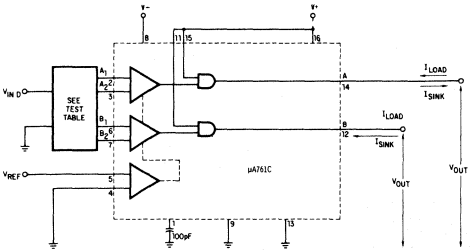


VOLTAGE WAVEFORMS



NOTES: 1. Pulse generators have the following characteristics:
$Z_{out} = 50\ \Omega$, $t_r = t_f = 15\ (\pm 5)$ ns, $t_{p1} = 100$ ns, $t_{p2} = 300$ ns, PRR = 1 MHz.
2. Strobe input pulse is applied to Strobe A when inputs A_1 - A_2 are being tested and to Strobe B when inputs B_1 - B_2 are being tested.
3. C_1 includes probe and jig capacitance.

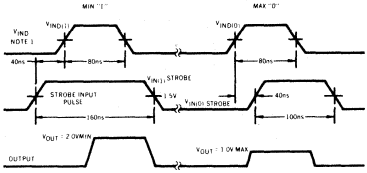
FIG. 2 DC TEST



TEST TABLE

TYPE	INPUTS	V_{ref}	V_{inD}	OUTPUT		
				V_{out}	I_{sink}	I_{load}
μA761C	A_1 - A_2 or B_1 - B_2	15 mV	< 11 mV	⩽ 0.4 V	16 mA	—
	A_1 - A_2 or B_1 - B_2	15 mV	> 19 mV	⩾ 2.4 V	—	−400 μA
	A_1 - A_2 or B_1 - B_2	40 mV	< 36 mV	⩽ 0.4 V	16 mA	—
	A_1 - A_2 or B_1 - B_2	40 mV	> 44 mV	⩾ 2.4 V	—	−400 μA

FIG. 3 MIN "1", MAX "0" TESTS



Notes: 1. Differential signal is applied to either input, either polarity.
2. Pulse generators have the following characteristics:
$Z_{OUT} = 50\ \Omega$ $t_r = t_f = 20$ ns
3. Strobe input pulse is applied to strobe A when inputs A_1 - A_2 are being tested and to strobe B when inputs B_1 - B_2 are being tested.
4. C_1 includes probe and jig capacitance.

μA761D

TWO CHANNEL CORE MEMORY SENSE AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

- **±2 mV THRESHOLD VARIATION**
- **25 ns PROPAGATION DELAY**
- **DUAL INDEPENDENT STROBES**
- **TTμL COMPATIBLE**

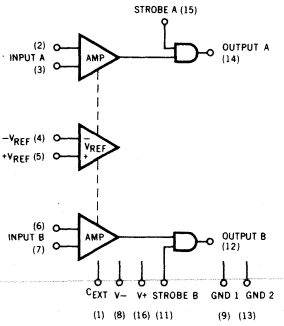
GENERAL DESCRIPTION — The μA761D is a Two Channel Core Memory Sense Amplifier constructed on a single silicon chip using the patented Fairchild Planar* epitaxial process. It can be used for small (1K to 8K words) memories as well as larger memory systems. The device is suitable for small core sizes facilitating very fast memory cycle times. The μA761D features tight threshold accuracy, fast response time, and independent strobe selection. Unit to unit variations are minimized so that individual adjustments of threshold and strobe timing are not necessary.

All logic inputs and outputs are fully TTμL compatible. The μA761D can be combined with Fairchild MSI Quad Latch 9314 to provide complete memory data register capability. For improved performance see μA761C data sheet.

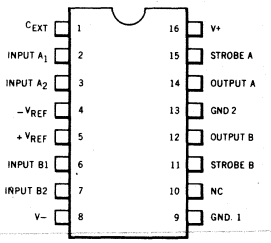
ABSOLUTE MAXIMUM RATINGS

Differential Input Voltage	±5.0 V
Supply Voltage	±7.0 V
Logic Input Voltage	+5.5 V
Power Dissipation (Note 1) 6M Package	400 mW
7B Package	500 mW
Storage Temperature 6M Package	−55°C to +125°C
7B Package	−65°C to +150°C
Operating Temperature	0°C to +70°C
Lead Temperature (6M Package, Soldering 10 seconds)	+260°C
(7B Package, Soldering 60 seconds)	+300°C
Signal Input	±3.0 V
Reference Input	±3.0 V

BLOCK DIAGRAM

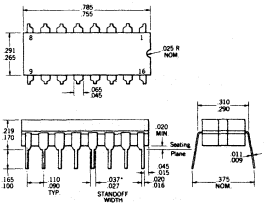


CONNECTION DIAGRAM



PHYSICAL DIMENSIONS

16 Lead Ceramic Dual In-Line



NOTES:

All dimensions in inches

Leads are intended for insertion in hole rows on .300" centers

They are purposely shipped with "positive" misalignment to facilitate insertion

Board-drilling dimensions should equal your practice for 0.20 inch diameter lead

Leads are tin plated kovar

Package weight is 2.2 grams

The .027/.037 dimensions does not apply to the corner leads

ORDER PART NO. U7B7761393

Note 1: Rating applies for Ambient Temperature to 70°C.

*Planar is a patented Fairchild process.

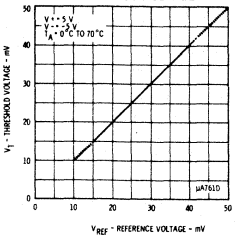
FAIRCHILD SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS ($V^+ = 5.0V$, $V^- = -5.0$ V; 0°C to +70°C either input unless otherwise specified)

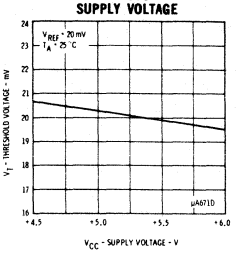
PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Threshold Voltage Range					
Minimum			10		mV
Maximum			50		mV
Threshold Uncertainty			±2.0		mV
Differential Input Threshold Voltage	V_{ref} = 15 mV	8.0		22	mV
	V_{ref} = 40 mV	33		47	mV
Differential Input Bias Current	V_{IND} = 0 mV		15	75	μA
Differential Input Offset Current	V_{IND} = 0 mV		1.0	10	μA
Differential Input Impedance	f = 1.0 kHz		2.5		kΩ
Positive Supply Current	T_A = 25°C		25	38	mA
Negative Supply Current	T_A = 25°C		10	16	mA
Output Short Circuit Current	V^- = 5.25 V, V^- = −5.25 V	2.1		3.5	mA
LOGIC INPUT/OUTPUT CONDITIONS (See Fig. 2)					
Output Voltage Logical "1"	I Load = 400 μA $V_{in(1)}$ STROBE = 2.0 V $V_{in(0)}$ STROBE = 0.8 V V^+ = 4.75 V V^- = −4.75 V	2.4	3.9		V
Output Voltage Logical "0"	I Sink = 16 mA $V_{in(0)}$ STROBE = 0.8 V V^+ = 4.75 V V^- = −4.75 V		0.25	0.4	V
Logical "1" Input (Strobe Inputs)	$V_{in(0)}$ STROBE = 0.8 V V^+ = 4.75 V V^- = −4.75 V	2.0			V
Logical "0" Input (Strobe Inputs)	$V_{in(1)}$ STROBE = 2.0 V V^+ = 4.75 V V^- = −4.75 V			0.8	V
Logical "0" Input Current (Strobe Inputs)	$V_{in(0)}$ STROBE = 0.4 V V^+ = 5.25 V V^- = −5.25 V		−1.0	−1.6	mA
Logical "1" Input Current (Strobe Inputs)	$V_{in(1)}$ STROBE = 2.4 V V^+ = 5.25 V V^- = −5.25 V			40	μA
Logical "1" Input Current (Strobe Inputs)	$V_{in(1)}$ STROBE = V^+ V^+ = 5.25 V V^- = −5.25 V			1.0	mA
A.C. CHARACTERISTICS (Either amplifier) T_A = 25°C					
Minimum "1" Test (See Fig. 3)	V_{ref} = 15 mV $V_{IND\ (1)}$ = 27 mV	2.0			V
Maximum "0" Test (See Fig. 3)	V_{ref} = 15 mV $V_{IND\ (0)}$ = 7 mV			1.0	V
Common Mode Input Firing Voltage	$t_r = t_f \leq 15$ ns t_p = 50 ns		±3.0		V
Differential Input Overload Recovery Time	V_{in} + 2.0 V, $t_r = t_f$ = 20 ns		20		ns
Common Mode Input Overload Recovery Time	V_{inCM} = ±2.0 V, $t_r = t_f$ = 20 ns		20		ns
Input to Output Delay	t_{pd} (1) D		25	40	ns
(See Figure 1)	t_{pd} (0) D		35	65	ns
Strobe to Output Delay	t_{pd} (1) STROBE		15	30	ns
(See Figure 1)	t_{pd} (0) STROBE		25	40	ns

TYPICAL PERFORMANCE CURVES

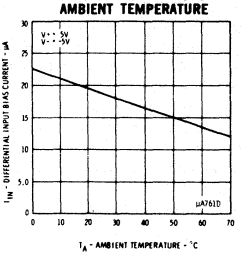
THRESHOLD VOLTAGE VERSUS REFERENCE VOLTAGE



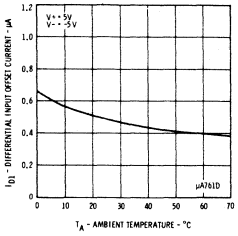
THRESHOLD VOLTAGE VERSUS SUPPLY VOLTAGE



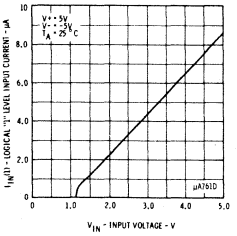
DIFFERENTIAL-INPUT BIAS CURRENT VERSUS AMBIENT TEMPERATURE



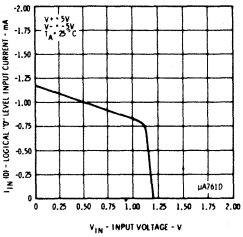
DIFFERENTIAL-INPUT OFFSET CURRENT VERSUS AMBIENT TEMPERATURE



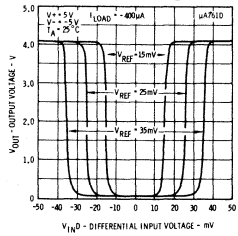
LOGICAL "1" LEVEL INPUT CURRENT VERSUS INPUT VOLTAGE



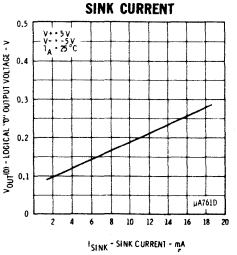
LOGICAL "0" LEVEL INPUT CURRENT VERSUS INPUT VOLTAGE



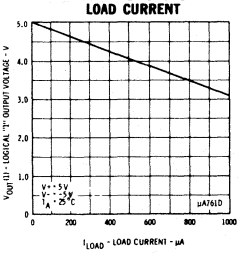
OUTPUT VOLTAGE VERSUS DIFFERENTIAL INPUT VOLTAGE



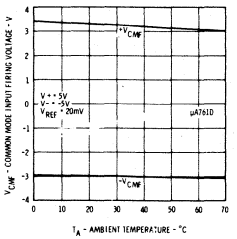
LOGICAL "0" OUTPUT VOLTAGE VERSUS SINK CURRENT



LOGICAL "1" OUTPUT VOLTAGE VERSUS LOAD CURRENT



COMMON-MODE FIRING VOLTAGE VERSUS AMBIENT TEMPERATURE



DEFINITION OF TERMS:

THRESHOLD VOLTAGE — The typical referred to input voltage which determines whether an input is a "1" or a "0". A signal whose magnitude is greater than the threshold level is sensed as a logic "1" and a signal whose magnitude is less as a "0".

THRESHOLD UNCERTAINTY — With all sense amps sharing the same input threshold setting, all input signals greater than the nominal threshold plus the uncertainty shall be sensed as a "1" and all input signals less than the nominal threshold less the uncertainty as a "0". This includes unit to unit, power supply and temperature variations.

PROPAGATION DELAY — The time delay measured from input threshold to output logic threshold with the strobe enabled.

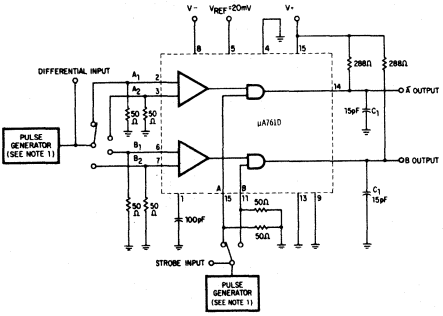
STROBE DELAY — The time delay measured from strobe to output logic threshold with a signal present exceeding the input threshold.

COMMON MODE RECOVERY TIME — The time from the turn off of the CM signal to the analog input threshold of the earliest sense line pulse signal that can be processed normally. Processed normally refers to bi-polar signals greater than or less than the input threshold with a corresponding proper output.

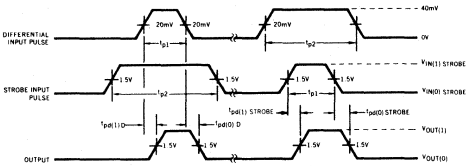
COMMON MODE FIRING VOLTAGE — The CM input voltage that exceeds the dynamic range of the inputs with strobe enabled resulting in the output switching states.

FIG. 1 PROPAGATION DELAY

TEST CIRCUITS

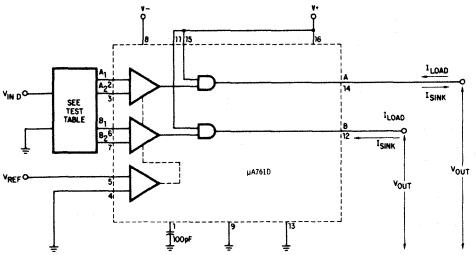


VOLTAGE WAVEFORMS



NOTES: 1. Pulse generators have the following characteristics:
$Z_{out} = 50\ \Omega$, $t_r = t_f = 15\ (\pm 5)$ ns, $t_{p1} = 100$ ns, $t_{p2} = 300$ ns, PRR = 1 MHz.
2. Strobe input pulse is applied to Strobe A when inputs A_1 - A_2 are being tested and to Strobe B when inputs B_1 - B_2 are being tested.
3. C_1 includes probe and jig capacitance.

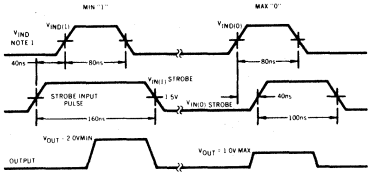
FIG. 2 DC TEST



TEST TABLE

TYPE	INPUTS	V_{ref}	V_{inD}	OUTPUT		
				V_{out}	I_{sink}	I_{load}
μA761D	A_1 - A_2 or B_1 - B_2	15 mV	< 8 mV	⩽ 0.4 V	16 mA	—
	A_1 - A_2 or B_1 - B_2	15 mV	> 22 mV	⩾ 2.4 V	—	−400 μA
	A_1 - A_2 or B_1 - B_2	40 mV	< 33 mV	⩽ 0.4 V	16 mA	—
	A_1 - A_2 or B_1 - B_2	40 mV	> 47 mV	⩾ 2.4 V	—	−400 μA

FIG. 3 MIN "1", MAX "0" TESTS



Notes: 1. Differential signal is applied to either input, either polarity.
2. Pulse generators have the following characteristics:
$Z_{OUT} = 50\ \Omega$ $t_r = t_f = 20$ ns
3. Strobe input pulse is applied to strobe A when inputs A_1 - A_2 are being tested and to strobe B when inputs B_1 - B_2 are being tested.
4. C_1 includes probe and jig capacitance.

μA767
FM STEREO MULTIPLEX DECODER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

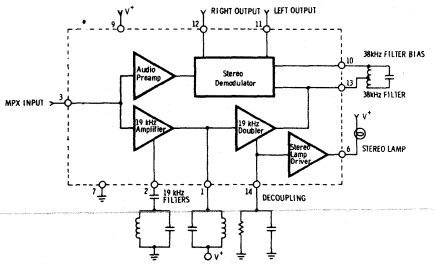
- **45 dB CHANNEL SEPARATION**
- **55 dB STORECAST REJECTION WITHOUT SCA FILTERS**
- **HIGH-CURRENT STEREO INDICATOR LAMP DRIVER**
- **OPERATION WITH 8 V TO 14 V SUPPLIES**

GENERAL DESCRIPTION—The μA767 is a monolithic FM Stereo Multiplex Decoder System constructed on a single silicon chip using the Fairchild Planar* Epitaxial Process. This integrated circuit accomplishes the demodulation of a Stereo Multiplex Signal into the Right and Left audio channels while inherently suppressing SCA frequency components. Internal provision is made for driving an external stereo mode indicator lamp. The excellent performance, wide supply range and low external parts requirement makes the μA767 suitable for all line-operated and automotive FM Stereo Multiplex applications. For Stereo Decoding including interstation audio muting and stereo/mode switching, see the μA729 and μA732 data sheets. See Note 1.

ABSOLUTE MAXIMUM RATINGS

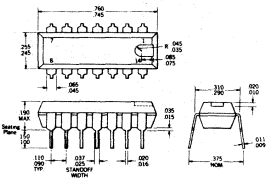
Supply Voltage (Note 2)		+15 V
Voltage at Stereo Lamp Driver Terminal		+22 V
Current into Stereo Lamp Driver Terminal (Note 3)		100 mA
Internal Power Dissipation		500 mW
Operating Temperature Range		0°C to + 70°C
Storage Temperature Range	9A Package	-55°C to + 125°C
	6A Package	-65°C to + 150°C
Lead Temperature (Soldering, 10 seconds)	9A Package	+ 260°C
(Soldering, 60 seconds)	6A Package	+ 300°C

BLOCK DIAGRAM



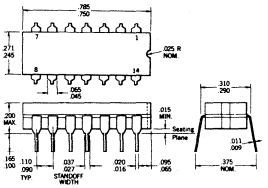
PHYSICAL DIMENSIONS

In accordance with JEDEC (TO-116) outline
14 LEAD SILICONE DUAL IN-LINE



ORDER PART NO. U9A7767394

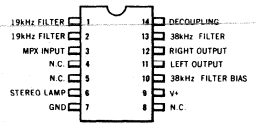
In accordance with JEDEC (TO-116) outline
14 LEAD CERAMIC DUAL IN-LINE



ORDER PART NO. U6A7767394

NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 0.9 gram for 9A
2.0 gram for 6A package

CONNECTION DIAGRAM
(TOP VIEW)



Notes on Page 2.

*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V^+ = + 12 V, 200 mV RMS Standard Stereo Multiplex signal applied to Input, unless otherwise specified (Note 4). Refer to Test Circuit of Figure 1.)

PARAMETER	MIN.	TYP.	MAX.	UNITS
Supply Current		12	18	mA
Input Resistance	12	20		kΩ
Stereo Separation				
f = 100 Hz		40		dB
f = 1 kHz	30	45		dB
f = 10 kHz	20	40		dB
Channel Balance (Monaural Input)		0.2		dB
Total Harmonic Distortion		0.5	1.0	%
Voltage Gain		1.0		V/V
67 kHz Storecast Rejection (Note 5)		55		dB
19 kHz Pilot Level Required at Input for:				
Stereo Indicator Lamp on		12	22	mV RMS
Stereo Indicator Lamp off	4.0	8.0		mV RMS
High Frequency Audio Components in Left and Right Outputs (dB below 1 kHz output)				
19 kHz		30		dB
38 kHz		25		dB

NOTES:

(1) The μA767 is a plug-in replacement for the MC1307. For μA767 applications information, and other Fairchild Communications Integrated circuits see listing on last page.

(2) Power supply transients up to 22V are permissible for periods of 15 seconds. However, extended operation at voltages greater than 15V should be avoided as the maximum allowable internal power dissipation for this device may be exceeded.

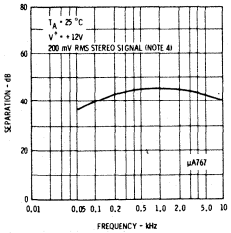
(3) Rating applies to steady state current. Maximum permissible surge current during turn-on of the Stereo Indicator Lamp is 500 mA.

(4) "Standard Stereo Multiplex Signal" here refers to a 200mV RMS (0.56V p-p) composite stereo signal including 10% pilot with L=1 and R = 1 as described in the FCC Rules on FM Broadcasting.

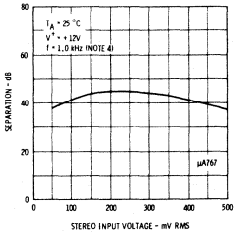
(5) Measured with a stereo composite signal consisting of 80% stereo, 10% pilot and 10% SCA as defined in the FCC Rules on FM Broadcasting.

TYPICAL PERFORMANCE CURVES

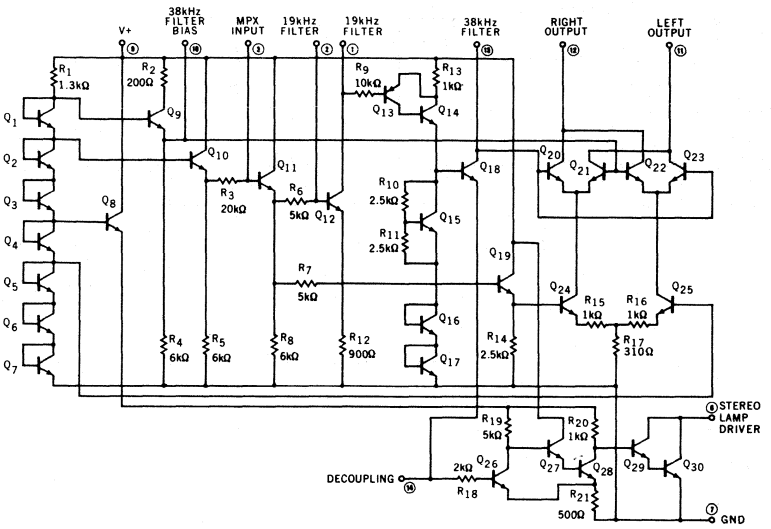
SEPARATION VERSUS AUDIO FREQUENCY



1 kHz SEPARATION VERSUS COMPOSITE INPUT VOLTAGE

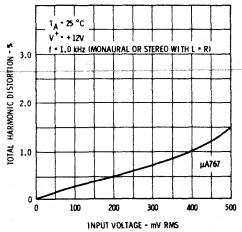


μA767 FM STEREO MULTIPLEX DECODER EQUIVALENT CIRCUIT

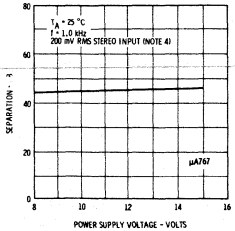


TYPICAL PERFORMANCE CURVES

1 kHz DISTORTION VERSUS INPUT VOLTAGE



1 kHz SEPARATION VERSUS POWER SUPPLY VOLTAGE



μA767 FM STEREO MULTIPLEX DECODER TEST CIRCUIT AND TYPICAL APPLICATION

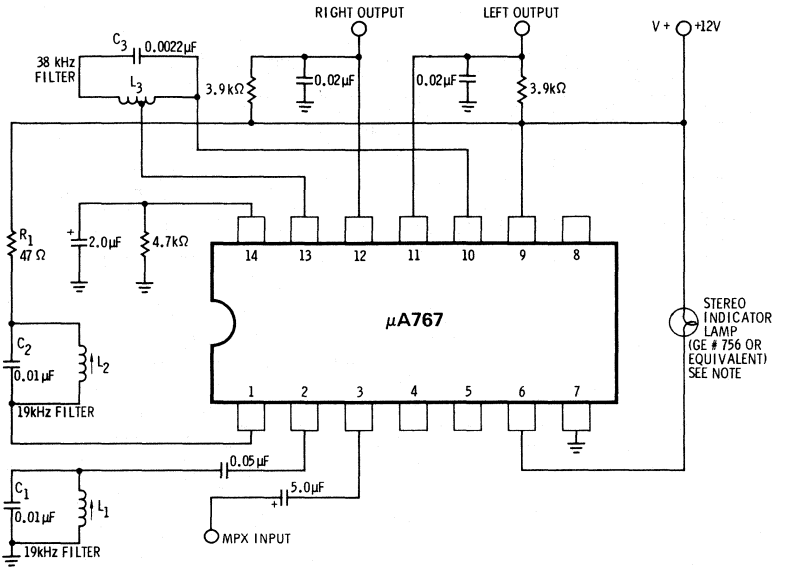


Fig. 1

NOTES:
(1) Capacitors C_1, C_2, and C_3 should be polystyrene or mylar.
(2) Coils L_1 and L_2 are 7.0 mH nominal with Q_{U_L} = 60 (Miller #1361 or equivalent).
(3) Coil L_3 is 8.0 mH nominal with Q_{U_L} = 80, tapped at 10:1 turns ratio. (Miller #1362 or equivalent).
(4) Resistor R_1 can be increased (or decreased) in value to increase (or decrease) the 19kHz sensitivity.

μA767 APPLICATIONS INFORMATION:

APP BRIEF 150—The μA729, μA732 and μA767 Integrated Circuit Stereo Multiplex Decoders.

FOR INFORMATION ON OTHER FAIRCHILD COMMUNICATIONS INTEGRATED CIRCUITS, SEE THE FOLLOWING DATA SHEETS:

RF/IF LIMITING AMP – μA703, μA703C, μA703D
AUDIO AMP – μA716C
TV/FM SOUND IF – μA719, μA719C, μA754, μA754C, μA784, μA3065
VIDEO AMPLIFIER – μA733, μA733C, μA715C
STEREO MULTIPLEX DECODER – μA729, μA732
STEREO AUDIO PREAMP – μA739C, μA749, μA749C, μA749D
DUAL AC AMPLIFIER/OSCILLATOR – μA745
COLOR TV CHROMA PROCESSING – μA706, μA707, μA746, μA780, μA781, μA786
AGC IF AMPLIFIER – μA757, μA757C
TV SIGNAL PROCESSING – μA708, μA785
AUTOMATIC FINE TUNING CIRCUITS – μA3064
BALANCED MODULATOR-DEMODULATOR – μA796, μA796C
GAIN CONTROLLED IF AMPLIFIER – μA781
TRANSISTOR AND DIODE ARRAYS – μA3018, μA3018A, μA3019, μA3026, μA3036, μA3045, μA3046, μA3054
VOLTAGE REGULATOR – μA723, μA723C

μA776
MULTI-PURPOSE PROGRAMMABLE OPERATIONAL AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

FEATURES:

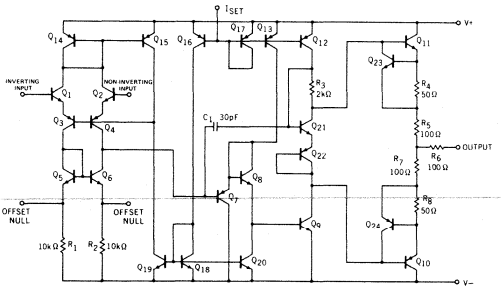
- **MICROPOWER CONSUMPTION**
- **±1.2V to ±18V OPERATION**
- **NO FREQUENCY COMPENSATION REQUIRED**
- **LOW INPUT BIAS CURRENTS**
- **WIDE PROGRAMMING RANGE**
- **HIGH SLEW RATE**
- **LOW NOISE**
- **SHORT CIRCUIT PROTECTION**
- **OFFSET NULL CAPABILITY**
- **NO LATCH UP**

DESCRIPTION – The μA776 Programmable Operational Amplifier is constructed on a single silicon chip using the Fairchild Planar* epitaxial process. High input impedance, low supply currents, and low input noise over a wide range of operating supply voltages coupled with programmable electrical characteristics result in an extremely versatile amplifier for use in high accuracy, low power consumption analog applications. Input voltage and current noise, power consumption, and input current can be optimized by a single resistor or current source that sets the chip quiescent current for nano-watt power consumption or for characteristics similar to the μA741. Internal frequency compensation, absence of latch up high slew rate and short circuit current protection assure ease of use in long time integrators, active filters, and sample and hold circuits. For information on other Fairchild Linear Operational Amplifiers see last page.

ABSOLUTE MAXIMUM RATINGS

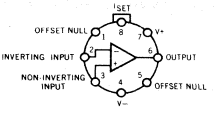
Supply Voltage	±18 V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Voltage Between Offset Null and V–	±0.5 V
I_{SET} (Maximum Current at I_{SET})	200 μA
V_{SET} (Maximum Voltage to Ground at I_{SET})	$(V^+ - 1.0\ V) \leqslant V_{SET} \leqslant V^+$
Storage Temperature Range	
Metal Can, Ceramic DIP	–65°C to +150°C
Mini DIP and Silicone DIP	–55°C to +125°C
Operating Temperature Range	
Military (312 Grade)	–55°C to +125°C
Commercial (393 Grade)	0°C to +70°C
Lead Temperature (Soldering, 60 seconds)	
Metal Can, Ceramic DIP	300°C
Mini DIP and Silicone DIP	260°C
Output Short-Circuit Duration (Note 3)	Indefinite

EQUIVALENT CIRCUIT



CONNECTION DIAGRAMS
8 LEAD METAL CAN

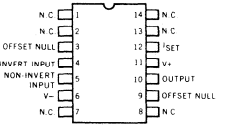
(TOP VIEW)



ORDER PART NOS: **PRODUCT CODE**
U5B7776312
U5B7776393

14 LEAD DIP

(TOP VIEW)

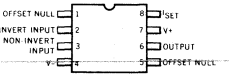


ORDER PART NOS:
FOR CERAMIC DIP : PRODUCT CODE
U6A7776312
U6A7776393

FOR SILICONE DIP : PRODUCT CODE
U9A7776393

MINI DIP

(TOP VIEW)



PRODUCT CODE:
ORDER PART NO.: **U9T7776393**

*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR

±3 VOLT OPERATION FOR 312 GRADE

ELECTRICAL CHARACTERISTICS (T_A = 25°C, Unless Otherwise Specified)

		I_{SET} = 1.5μA			I_{SET} = 15μA			
PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10k\Omega$		2.0	5.0		2.0	5.0	mV
Input Offset Current			0.7	3.0		4.0	15	nA
Input Bias Current			2.0	7.5		15	50	nA
Input Resistance			50			5.0		MΩ
Input Capacitance			2.0			2.0		pF
Offset Voltage Adjustment Range			9.0			18		mV
Large Signal Voltage Gain	$R_L \geq 75k\Omega$, V_{OUT}=±1V	50k	200k					V/V
	$R_L \geq 5k\Omega$, V_{OUT}=±1V				50k	200k		V/V
Output Resistance			5k			1k		Ω
Output Short-Circuit Current			2.0			5.0		mA
Supply Current			13	20		100	120	μA
Power Consumption			78	120		600	720	μW
Transient Response (unity gain)	V_{IN} = 20mV, $R_L \geq 5k\Omega$, C_L=100pF							
Risetime			3.0			0.6		μs
Overshoot			0			5		%
Slew Rate	$R_L \geq 5k\Omega$		0.03			0.35		V/μs
The following specifications apply for $-55°C \leq T_A \leq 125°C$								
Input Offset Voltage	$R_S \leq 10k\Omega$			6.0			6.0	mV
Input Offset Current	T_A = +125°C			5.0			15	nA
	T_A = −55°C			10			40	nA
Input Bias Current	T_A = +125°C			7.5			50	nA
	T_A = −55°C			20			120	nA
Input Voltage Range		±1.0			±1.0			V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	86		70	86		dB
Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$		25	150		25	150	μV/V
Large-Signal Voltage Gain	$R_L \geq 75k\Omega$, V_{OUT}=±1V	25k						V/V
	$R_L \geq 5k\Omega$, V_{OUT}=±1V				25k			V/V
Output Voltage Swing	$R_L \geq 75k\Omega$	±2.0	±2.4					V
	$R_L \geq 5k\Omega$				±1.9	±2.1		V
Supply Current				25			125	μA
Power Consumption				150			750	μW

NOTES:

1. Military ratings (312 grade) apply for case temperatures to 125° C; Derate linearly at 6.5 mW/° C for ambient temperatures above +75° C. Commercial ratings (393 grade) apply for case temperatures to +70° C.
2. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125° C case temperature or +75° C ambient temperature for $I_{SET} \leq 30$ μA.

±15 VOLT OPERATION FOR 312 GRADE

ELECTRICAL CHARACTERISTICS (T_A = 25°C, Unless Otherwise Specified)

		I_{SET} = 1.5μA			I_{SET} = 15μA			
PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10k\Omega$		2.0	5.0		2.0	5.0	mV
Input Offset Current	$R_S \leq 10k\Omega$		0.7	3.0		4.0	15	nA
Input Bias Current			2.0	7.5		15	50	nA
Input Resistance			50			5.0		MΩ
Input Capacitance			2.0			2.0		pF
Offset Voltage Adjustment Range			9.0			18		mV
Large-Signal Voltage Gain	$R_L \geq 75k\Omega$, V_{OUT} = ±10V	200k	400k					V/V
	$R_L \geq 5k\Omega$, V_{OUT} = ±10V				100k	400k		V/V
Output Resistance			5.0k			1.0k		Ω
Output Short-Circuit Current			2.0			10		mA
Supply Current			20	25		125	150	μA
Power Consumption				0.75			4.5	mW
Transient Response (unity gain)	V_{IN}=20mV, $R_L \geq 5k\Omega$, $C_L \leq 100pF$							
Risetime			1.6			0.35		μs
Overshoot			0			10		%
Slew Rate	$R_L \geq 5k\Omega$		0.1			0.8		V/μs
Output Voltage Swing	$R_L \geq 75k\Omega$	±12	±14					V
	$R_L \geq 5k\Omega$				±10	±13		V
The following specifications apply	$-55°C \leq T_A \leq +125°C$							
Input Offset Voltage	$R_S \leq 10k\Omega$			6.0			6.0	mV
Input Offset Current	T_A = +125°C			5.0			15	nA
	T_A = −55°C			10			40	nA
Input Bias Current	T_A = +125°C			7.5			50	nA
	T_A = −55°C			20			120	nA
Input Voltage Range		±10			±10			V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$		25	150		25	150	μV/V
Large-Signal Voltage Gain	$R_L \geq 75k\Omega$, V_{OUT}=±10V	100k			75k			V/V
Output Voltage Swing	$R_L \geq 75k\Omega$	±10			±10			V
Supply Current				30			170	μA
Power Consumption				0.9			5.1	mW

±3 VOLT OPERATION FOR 393 GRADE

ELECTRICAL CHARACTERISTICS (T_A = 25°C, Unless Otherwise Specified)

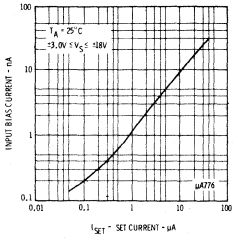
		I_{SET} = 1.5μA			I_{SET} = 15μA			
PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10k\Omega$		2.0	6.0		2.0	6.0	mV
Input Offset Current			0.7	6.0		4.0	25	nA
Input Bias Current			2.0	10		15	50	nA
Input Resistance			50			5.0		MΩ
Input Capacitance			2.0			2.0		pF
Offset Voltage Adjustment Range			9.0			18		mV
Large-Signal Voltage Gain	$R_L \geq 75k\Omega$, V_{OUT}=±1V	25k	200k					V/V
	$R_L \geq 5k\Omega$, V_{OUT}=±1V				25 k	200k		V/V
Output Resistance			5.0			1.0		kΩ
Output Short-Circuit Current			2.0			5.0		mA
Supply Current			13	20		100	120	μA
Power Consumption			78	120		600	720	μW
Transient Response (unity gain)	V_{IN} = 20mV, $R_L \geq 5k\Omega$, C_L = 100pF							
Risetime			3.0			0.6		μs
Overshoot			0			5		%
Slew Rate	$R_L \geq 5k\Omega$		0.03			0.35		V/μs
The following specifications apply for $0°C \leq T_A \leq +70°C$								
Input Offset Voltage	$R_S \leq 10k\Omega$			7.5			7.5	mV
Input Offset Current	T_A = +70°C			6.0			25	nA
	T_A = 0°C			10			40	nA
Input Bias Current	T_A = +70°C			10			50	nA
	T_A = 0°C			20			100	nA
Input Voltage Range		±1.0			±1.0			V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	86		70	86		dB
Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$		25	200		25	200	μV/V
Large-Signal Voltage Gain	$R_L \geq 75k\Omega$, V_{OUT}=±1V	25k						V/V
	$R_L \geq 5k\Omega$, V_{OUT}=±1V				25k			V/V
Output Voltage Swing	$R_L \geq 75k\Omega$	±2.0	±2.4					V
	$R_L \geq 5k\Omega$				±2.0	±2.1		V
Supply Current				25			125	μA
Power Consumption				150			750	μW

±15 VOLT OPERATION FOR 393 GRADE

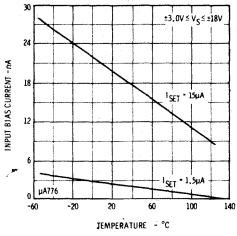
ELECTRICAL CHARACTERISTICS (T_A = 25°C, Unless Otherwise Specified)

		I_{SET} = 1.5μA			I_{SET} = 15μA			
PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10k\Omega$		2.0	6.0		2.0	6.0	mV
Input Offset Current			0.7	6.0		4.0	25	nA
Input Bias Current			2.0	10		15	50	nA
Input Resistance			50			5.0		MΩ
Input Capacitance			2.0			2.0		pF
Offset Voltage Adjustment Range			9.0			18		mV
Large-Signal Voltage Gain	$R_L \geq 75k\Omega$, V_{OUT}=±10V	50k	400k					V/V
	$R_L \geq 5k\Omega$, V_{OUT}=±10V				50k	400k		V/V
Output Resistance			5.0			1.0		kΩ
Output Short-Circuit Current			2.0			10		mA
Supply Current			20	30		125	160	μA
Power Consumption				0.9			4.8	mW
Transient Response (unity gain)	V_{IN} = 20mV, $R_L \geq 5k\Omega$, $C_L \leq 100pF$							
Risetime			1.6			0.35		μs
Overshoot			0			10		%
Slew Rate	$R_L \geq 5k\Omega$		0.1			0.8		V/μs
Output Voltage Swing	$R_L \geq 75k\Omega$	±12	±14					V
	$R_L \geq 5k\Omega$				±10	±13		V
The following specifications apply to $0°C \leq T_A \leq +70°C$								
Input Offset Voltage	$R_S \leq 10k\Omega$			7.5			7.5	mV
Input Offset Current	T_A = +70°C			6.0			25	nA
	T_A = 0°C			10			40	nA
Input Bias Current	T_A = +70°C			10			50	nA
	T_A = 0°C			20			100	nA
Input Voltage Range		±10			±10			V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$		25	200		25	200	μV/V
Large-Signal Voltage Gain	$R_L \geq 75k\Omega$, V_{OUT}=±10V	50k			50k			V/V
Output Voltage Swing	$R_L \geq 75k\Omega$	±10			±10			V
Supply Current				35			170	μA
Power Consumption				1.05			5.10	mW

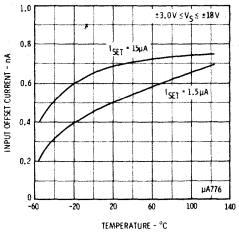
INPUT BIAS CURRENT AS A FUNCTION OF SET CURRENT



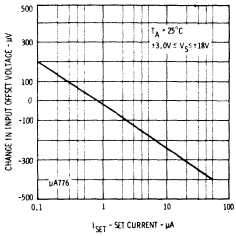
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



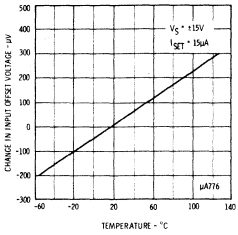
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



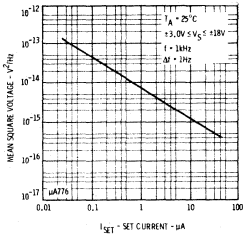
CHANGE IN INPUT OFFSET VOLTAGE AS A FUNCTION OF SET CURRENT



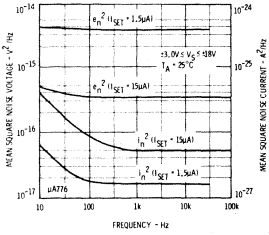
CHANGE IN INPUT OFFSET VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE (UNNULLED)



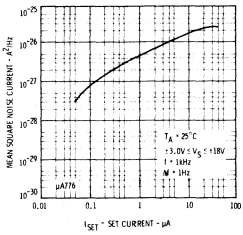
INPUT NOISE VOLTAGE AS A FUNCTION OF SET CURRENT



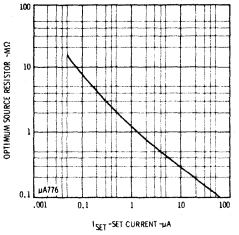
INPUT NOISE VOLTAGE AND CURRENT AS A FUNCTION OF FREQUENCY



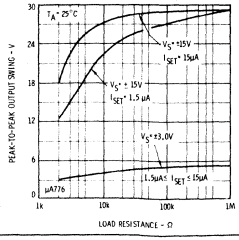
INPUT NOISE CURRENT AS A FUNCTION OF SET CURRENT



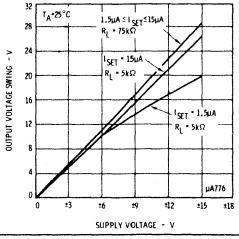
OPTIMUM SOURCE RESISTOR FOR MINIMUM NOISE AS A FUNCTION OF SET CURRENT



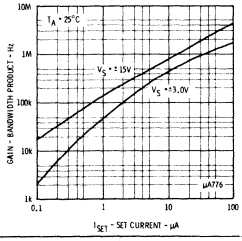
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



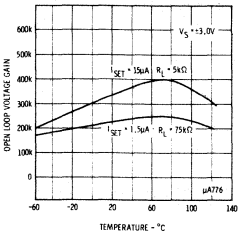
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



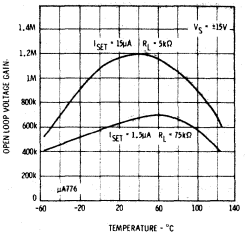
GAIN-BANDWIDTH PRODUCT AS A FUNCTION OF SET CURRENT



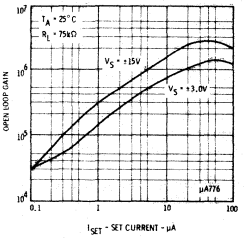
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



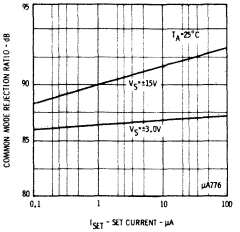
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



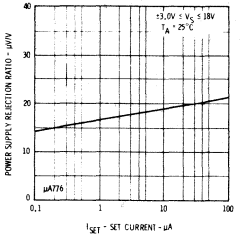
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SET CURRENT



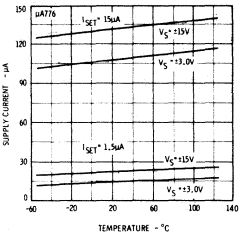
COMMON MODE REJECTION RATIO AS A FUNCTION OF SET CURRENT



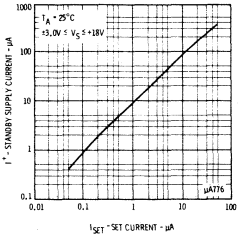
POWER SUPPLY REJECTION RATIO AS A FUNCTION OF SET CURRENT



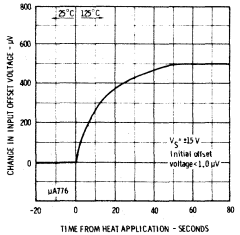
SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



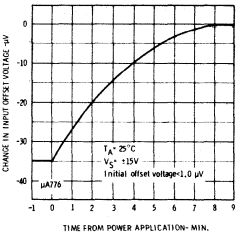
STANDBY SUPPLY CURRENT AS A FUNCTION OF SET CURRENT



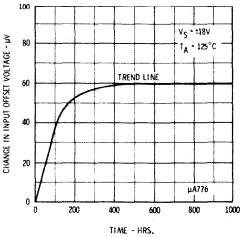
THERMAL RESPONSE OF INPUT OFFSET VOLTAGE TO STEP CHANGE OF CASE TEMPERATURE



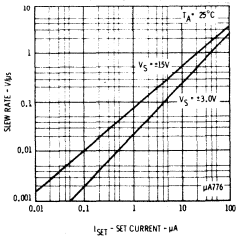
STABILIZATION TIME OF INPUT OFFSET VOLTAGE FROM POWER ON



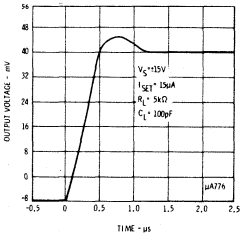
INPUT OFFSET VOLTAGE DRIFT AS A FUNCTION OF TIME



SLEW RATE AS A FUNCTION OF SET CURRENT



VOLTAGE FOLLOWER TRANSIENT RESPONSE (UNITY GAIN)



DEFINITION OF TERMS

UNITY GAIN BANDWIDTH PRODUCT – The frequency at which the open loop gain of the amplifier is unity.

INPUT OFFSET VOLTAGE – That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT – The difference in the currents into the two input terminals with the output at zero volts.

INPUT BIAS CURRENT – The average of the two input currents.

INPUT RESISTANCE – The resistance looking into either input terminal with the other grounded.

INPUT CAPACITANCE – The capacitance looking into either input terminal with the other grounded.

LARGE-SIGNAL VOLTAGE GAIN – The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT RESISTANCE – The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

OUTPUT SHORT-CIRCUIT CURRENT – The maximum output current available from the amplifier with the output shorted to ground or to either supply.

SUPPLY CURRENT – The DC current from the supplies required to operate the amplifier with the output at zero and with no load current.

POWER CONSUMPTION – The DC power required to operate the amplifier with the output at zero and with no load current.

TRANSIENT RESPONSE – The closed-loop step-function response of the amplifier under small-signal conditions.

INPUT VOLTAGE RANGE – The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

INPUT COMMON MODE REJECTION RATIO – The ratio of the input voltage range to the maximum change in input offset voltage over this range.

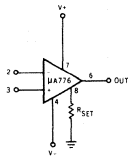
SUPPLY VOLTAGE REJECTION RATIO – The ratio of the change in input offset voltage to the change in supply voltage producing it.

OUTPUT VOLTAGE SWING – The peak output swing, referred to zero, that can be obtained without clipping.

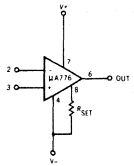
QUIESCENT SET CURRENT – The current out of the quiescent current set terminal which sets the current levels for the current sources in the amplifier.

BIASING CIRCUITS

RESISTOR BIASING



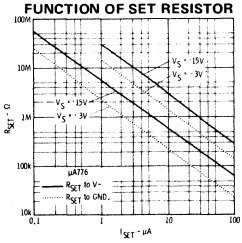
R_{SET} CONNECTED TO GROUND



R_{SET} CONNECTED TO V^-*

*Recommended for supply voltages less than ±6V.

SET CURRENT AS A FUNCTION OF SET RESISTOR

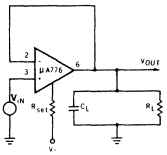


QUIESCENT CURRENT SETTING RESISTOR (I_{SET} TO V^-)

V_S	I_{SET}	
	1.5μA	15μA
±1.5 V	1.7MΩ	170kΩ
±3.0 V	3.6MΩ	360kΩ
±6.0 V	7.5MΩ	750kΩ
±15 V	20MΩ	2.0MΩ

Note: The μA776 may be operated with R_{set} connected to ground or V^-

TRANSIENT RESPONSE TEST CIRCUIT



I_{SET} EQUATIONS:

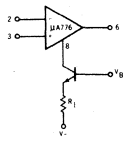
$$I_{SET} = \frac{V^+ - 0.7 - V^-}{R_{SET}}$$

where R_{SET} is connected to V^-

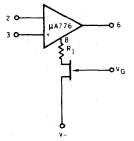
$$I_{SET} = \frac{V^+ - 0.7}{R_{SET}}$$

where R_{SET} is connected to ground.

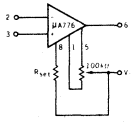
TRANSISTOR CURRENT SOURCE BIASING



FET CURRENT SOURCE BIASING

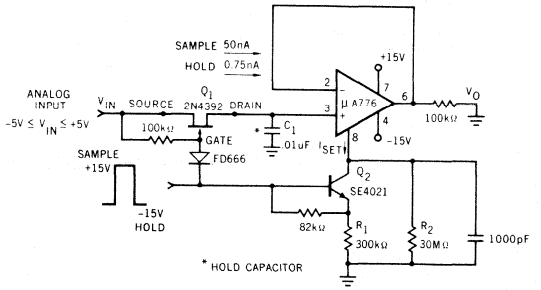


VOLTAGE OFFSET NULL CIRCUIT

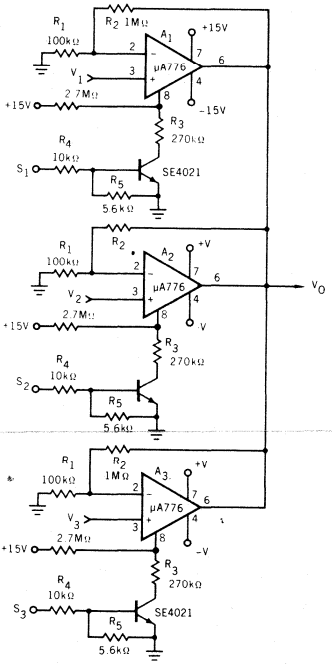


TYPICAL APPLICATIONS

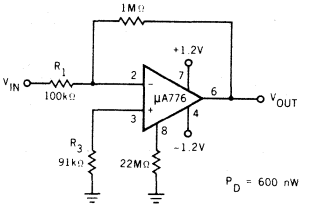
HIGH ACCURACY SAMPLE AND HOLD



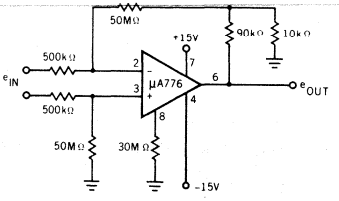
MULTIPLEXING AND SIGNAL CONDITIONING WITHOUT FET'S



NANO-WATT AMPLIFIER



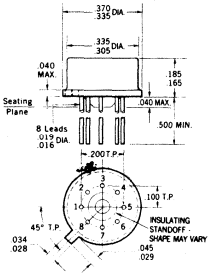
HIGH INPUT IMPEDANCE AMPLIFIER



PHYSICAL DIMENSIONS

METAL CAN
5B PACKAGE

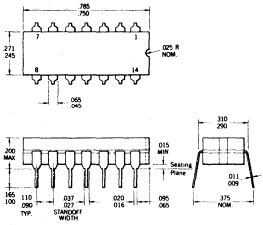
in accordance with JEDEC (TO-99) outline



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.22 grams

CERAMIC DIP
6A PACKAGE

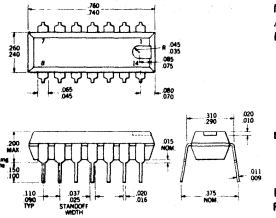
in accordance with JEDEC (TO-116) outline



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams

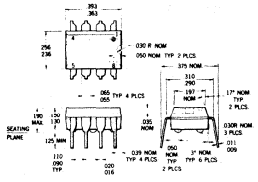
SILICONE DIP
9A PACKAGE

In accordance with JEDEC (TO-116) outline



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for .020 inch diameter lead.
Leads are tin-plated kovar
Package weight is 0,9 gram

MINI DIP
9T PACKAGE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 0.6 gram
Package material is silicone

FOR INFORMATION ON OTHER FAIRCHILD OPERATIONAL AMPLIFIERS, SEE THE FOLLOWING DATA SHEETS:

HIGH SPEED – μA715
INSTRUMENTATION – μA725
TEMPERATURE STABLE PREAMPS – μA727
MICROPOWER – μA735
FET INPUT – μA740
FREQUENCY COMPENSATED – μA741
DUALS – μA739, μA747, μA749
HIGH PERFORMANCE – μA101, μA201, μA748
PRECISION – μA777, μA108A, μA208A, μA308A
GENERAL PURPOSE – μA101A, μA201A, μA301A

μA777 . μA777C
PRECISION OPERATIONAL AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

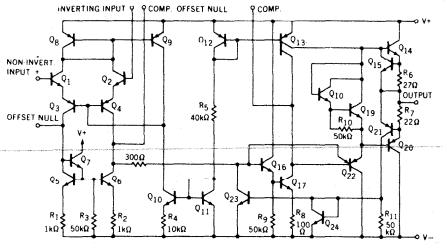
- **LOW OFFSET VOLTAGE AND OFFSET CURRENT**
- **LOW OFFSET VOLTAGE AND CURRENT DRIFT**
- **LOW INPUT BIAS CURRENT**
- **LOW INPUT NOISE VOLTAGE**
- **LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES**

GENERAL DESCRIPTION – The μA777 is a precision operational amplifier constructed on a single silicon chip, using a low noise Fairchild Planar* epitaxial process. It is an excellent choice when performance versus cost trade-offs are possible between super beta or FET input operational amplifiers and low cost general purpose operational amplifiers. Low offset and bias currents improve system accuracy when used in applications such as long term integrators, sample and hold circuits and high source impedance summing amplifiers. Even though the input bias current is extremely low, the μA777 maintains full ± 30 V differential voltage range. The internal construction utilizes isothermal layout and special electrical design to maintain system performance despite variations in temperature or output load. High common mode input voltage range, latch-up protection, short circuit protection and simple frequency compensation make the device versatile and essentially foolproof. (See last page for information on other Fairchild operational amplifiers.)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	± 22 V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	± 30 V
Input Voltage (Note 2)	± 15 V
Storage Temperature Range	
Metal Can, Ceramic DIP, and Flatpak	-65°C to + 150°C
Mini DIP and Silicone DIP	-55°C to + 125°C
Operating Temperature Range	
Military (312 and 313 grades)	-55°C to + 125°C
Commercial (393 grade)	0°C to + 70°C
Lead Temperature (Soldering, 60 Seconds)	
Metal Can, Ceramic DIP and Flatpak	300°C
Mini DIP and Silicone DIP	260°C
Output Short Circuit Duration (Note 3)	Indefinite

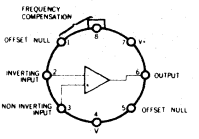
EQUIVALENT CIRCUIT



Notes: See Page 3.

CONNECTION DIAGRAMS

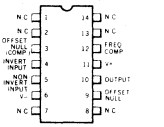
8 LEAD METAL CAN
(TOP VIEW)



NOTE: Pin 4 connected to case

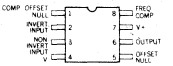
ORDER PART NOS: U5B7777312
U5B7777393

14 LEAD DIP
(TOP VIEW)



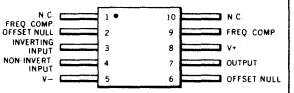
ORDER PART NOS: U6A7777312
U6A7777393
U9A7777393

MINI DIP
(TOP VIEW)



ORDER PART NO: U9T7777393

10 LEAD FLAT PACK ‡
(TOP VIEW)



‡Available on special request

ORDER PART NO: U3F7777312
U3F7777313

*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS FOR μA777 (312 GRADE) (V_S = ± 15 V, T_A = 25°C, C_C = 30 pF unless otherwise specified)

PARAMETERS (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 50\ k\Omega$		.5	2.0	mV
Input Offset Current			.25	3.0	nA
Input Bias Current			8.0	25	nA
Input Resistance		2.0	10.0		MΩ
Input Capacitance			3.0		pF
Offset Voltage Adjustment Range			± 25		mV
Large-Signal Voltage Gain	$R_L \geq 2\ k\Omega$, V_{OUT} = ± 10V	50,000	250,000		
Output Resistance			100		Ω
Output Short-Circuit Current			± 25		mA
Supply Current			1.9	2.8	mA
Power Consumption			60	85	mW
Transient Response	V_{IN} = 20 mV, C_C = 30 pF,				
(Voltage Follower, Gain of 1)	R_L = 2 kΩ, $C_L \leq$ 100 pF				
Risetime			.3		μs
Overshoot			5.0		%
Slew Rate	$R_L \geq 2k\Omega$		.5		V/μs
(Voltage Follower, Gain of 1)					
Transient Response	V_{IN} = 20 mV, C_C = 3.5 pF,				
(Voltage Follower, Gain of 10)	R_L = 2 kΩ, $C_L \leq$ 100 pF				
Risetime			.2		μs
Overshoot			5.0		%
Slew Rate	$R_L \geq 2\ k\Omega$, C_C = 3.5 pF		5.5		V/μs
(Voltage Follower, Gain of 10)					
The following specifications apply for	-55°C ≤ T_A ≤ + 125°C:				
Input Offset Voltage	$R_S \leq 50\ k\Omega$		0.5	3.0	mV
Average Input Offset Voltage Drift	$R_S \leq 50\ k\Omega$		2.5	15	μV/°C
Input Offset Current				10	nA
Average Input Offset Current Drift	25°C ≤ T_A ≤ 125°C		2.5	30	pA/°C
	-55°C ≤ T_A ≤ 25°C		6.5	150	pA/°C
Input Bias Current				75	nA
Input Voltage Range		± 12	± 13		V
Common Mode Rejection Ratio	$R_S \leq 50\ k\Omega$	80	95		dB
Supply Voltage Rejection Ratio	$R_S \leq 50\ k\Omega$		13	100	μV/V
Large-Signal Voltage Gain	$R_L \geq 2\ k\Omega$, V_{OUT} = ± 10 V	25,000			
Output Voltage Swing	$R_L \geq 10\ k\Omega$	± 12	± 14		V
	$R_L \geq 2\ k\Omega$	± 10	± 13		V
Supply Current	T_A = + 125°C		1.5	2.5	mA
	T_A = -55°C		2.0	3.3	mA
Power Consumption	T_A = + 125°C		40	75	mW
	T_A = -55°C		60	100	mW

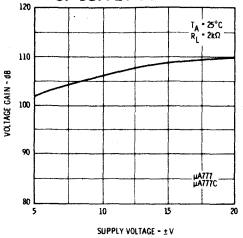
ELECTRICAL CHARACTERISTICS FOR μA777C (393 and 313 GRADE) ($V_S = \pm 15$ V, $T_A = 25°C$, $C_C = 30$ pF unless otherwise specified)

PARAMETERS (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 50\ k\Omega$		0.7	5.0	mV
Input Offset Current			0.7	20.0	nA
Input Bias Current			25	100	nA
Input Resistance		1.0	2.0		MΩ
Input Capacitance			3.0		pF
Offset Voltage Adjustment Range			± 25		mV
Large-Signal Voltage Gain	$R_L \geq 2\ k\Omega$, $V_{OUT} = \pm 10V$	25,000	250,000		
Output Resistance			100		Ω
Output Short-Circuit Current			± 25		mA
Supply Current			1.9	2.8	mA
Power Consumption			60	85	mW
Transient Response	$V_{IN} = 20$ mV, $C_C = 30$ pF,				
(Voltage Follower, Gain of 1)	$R_L = 2\ k\Omega$, $C_L \leq 100$ pF				
Risetime			.3		μs
Overshoot			5.0		%
Slew Rate	$R_L \geq 2\ k\Omega$		.5		V/μ
(Voltage Follower, Gain of 1)					
Transient Response	$V_{IN} = 20$ mV, $C_C = 3.5$ pF,				
(Voltage Follower, Gain of 10)	$R_L = 2\ k\Omega$, $C_L \leq 100$ pF				
Risetime			.2		μs
Overshoot			5.0		%
Slew Rate	$R_L \geq 2\ k\Omega$		5.5		V/μs
(Voltage Follower, Gain of 10)					
The following specifications apply for $0°C \leq T_A \leq +70°C$ (Note 4):					
Input Offset Voltage	$R_S \leq 50\ k\Omega$		0.8	5.0	mV
Average Input Offset Voltage Drift	$R_S \leq 50\ k\Omega$		4	30	μV/°C
Input Offset Current				40	nA
Average Input Offset Current Drift	$25°C \leq T_A \leq 70°C$		.01	0.3	nA/°C
	$0°C \leq T_A \leq 25°C$		.02	0.6	nA/°C
Input Bias Current				200	nA
Input Voltage Range		± 12	± 13		V
Common Mode Rejection Ratio	$R_S \leq 50\ k\Omega$	70	95		dB
Supply Voltage Rejection Ratio	$R_S \leq 50\ k\Omega$		15	150	μV/V
Large-Signal Voltage Gain	$R_L \geq 2\ k\Omega$, $V_{OUT} = \pm 10$ V	15,000			
Output Voltage Swing	$R_L \geq 10\ k\Omega$	± 12	± 14		V
	$R_L \geq 2\ k\Omega$	± 10	± 13		V
Power Consumption			60	100	mW

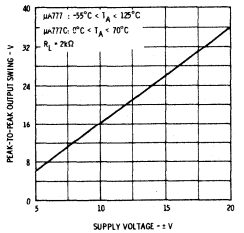
NOTES:
(1) Military ratings (312 and 313 grades) apply for case temperatures to 125°C; Derate linearly at 6.5 mW/°C for ambient temperatures above + 75°C. Commercial ratings (393 grade) apply for case temperatures to + 70°C. Flatpack maximum dissipation is 300 mW.
(2) For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.
(3) Short circuit may be to ground or either supply. Rating applies to + 125°C case temperature or + 75°C ambient temperature.
(4) 313 grade specifications apply for $-55°C \leq T_A \leq 125°C$.

TYPICAL PERFORMANCE CURVES

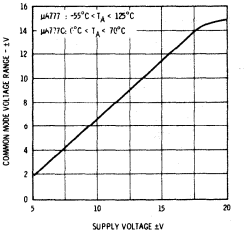
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



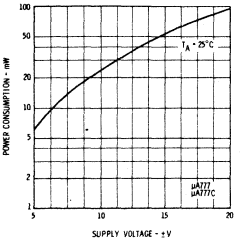
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



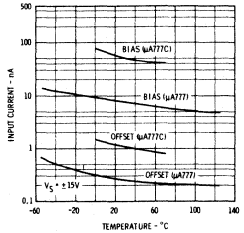
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



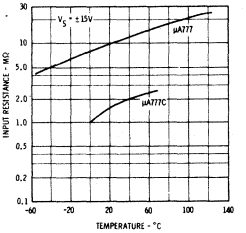
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



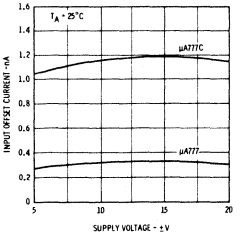
INPUT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



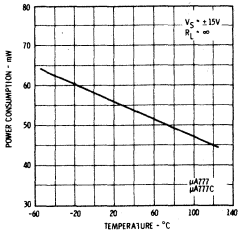
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



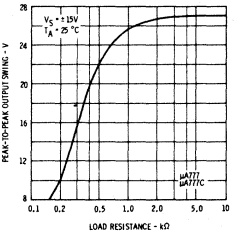
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



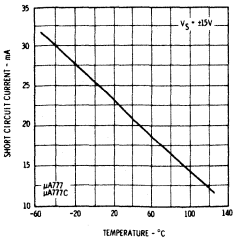
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



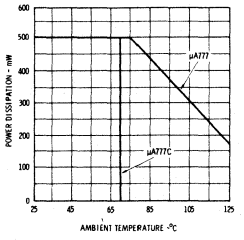
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



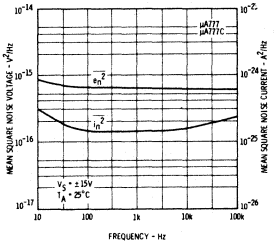
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE

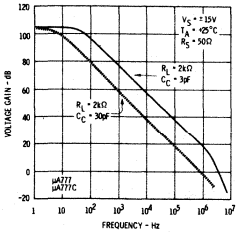


INPUT NOISE VOLTAGE AND CURRENT AS A FUNCTION OF FREQUENCY

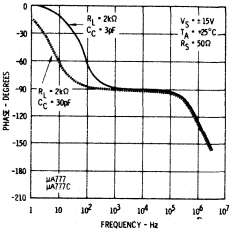


TYPICAL PERFORMANCE CURVES

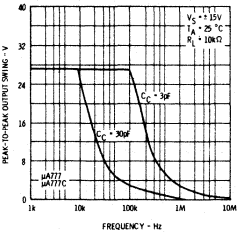
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



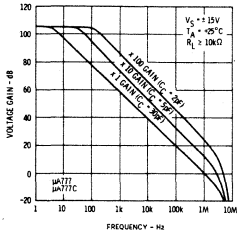
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



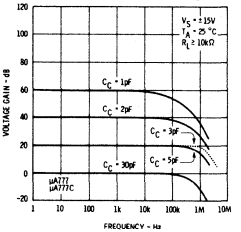
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



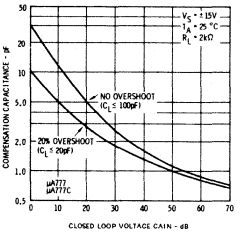
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY FOR VARIOUS GAIN/COMPENSATION OPTIONS



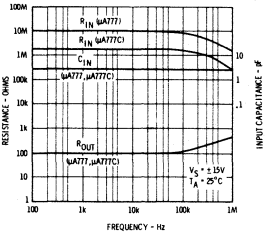
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS



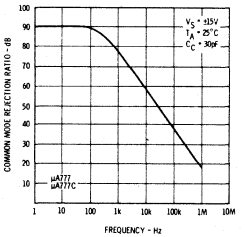
COMPENSATION CAPACITANCE AS A FUNCTION OF CLOSED LOOP VOLTAGE GAIN



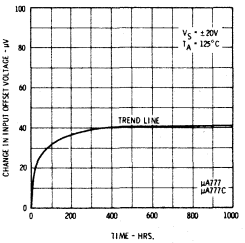
INPUT RESISTANCE, OUTPUT RESISTANCE, AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY



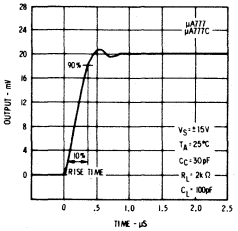
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



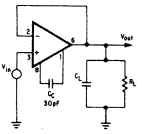
INPUT OFFSET VOLTAGE DRIFT AS A FUNCTION OF TIME



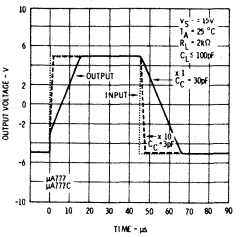
VOLTAGE FOLLOWER TRANSIENT RESPONSE (GAIN OF 1)



TRANSIENT RESPONSE TEST CIRCUIT

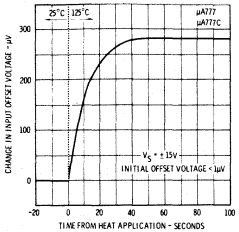


VOLTAGE FOLLOWER LARGE-SIGNAL PULSE RESPONSE

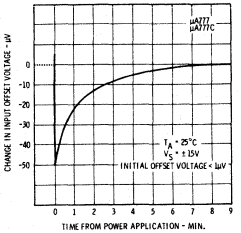


TYPICAL PERFORMANCE CURVES (CONT'D)

THERMAL RESPONSE OF INPUT OFFSET VOLTAGE TO STEP CHANGE OF CASE TEMPERATURE

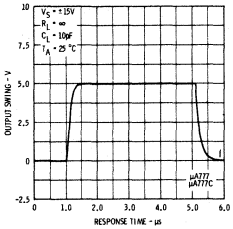


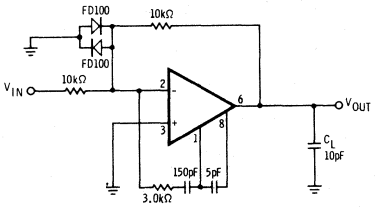
STABILIZATION TIME OF INPUT OFFSET VOLTAGE FROM POWER TURN-ON



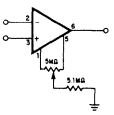
FEED-FORWARD COMPENSATION

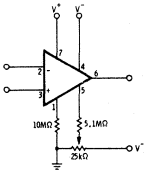
LARGE SIGNAL FEEDFORWARD TRANSIENT RESPONSE



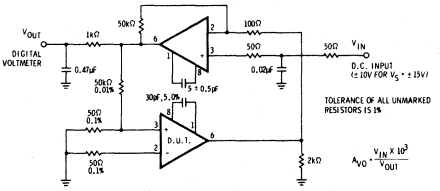


VOLTAGE OFFSET NULL CIRCUIT





GAIN TEST CIRCUIT



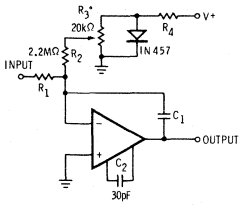
SUGGESTED **ALTERNATE**

DEFINITION OF TERMS

INPUT OFFSET VOLTAGE – That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.
INPUT OFFSET CURRENT – The difference in the currents into the two input terminals with the output at zero volts.
INPUT BIAS CURRENT – The average of the two input currents.
INPUT RESISTANCE – The resistance looking into either input terminal with the other grounded.
INPUT CAPACITANCE – The capacitance looking into either input terminal with the other grounded.
LARGE-SIGNAL VOLTAGE GAIN – The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.
OUTPUT RESISTANCE – The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.
OUTPUT SHORT-CIRCUIT CURRENT – The maximum output current available from the amplifier with the output shorted to ground or to either supply.
SUPPLY CURRENT – The DC current from the supplies required to operate the amplifier with the output at zero and with no load current.
POWER CONSUMPTION – The DC power required to operate the amplifier with the output at zero and with no load current.
TRANSIENT RESPONSE – The closed-loop step-function response of the amplifier under small-signal conditions.
INPUT VOLTAGE RANGE – The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.
INPUT COMMON MODE REJECTION RATIO – The ratio of the input voltage range to the maximum change in input offset voltage over this range.
SUPPLY VOLTAGE REJECTION RATIO – The ratio of the change in input offset voltage to the change in supply voltage producing it.
OUTPUT VOLTAGE SWING – The peak output swing, referred to zero, that can be obtained without clipping.

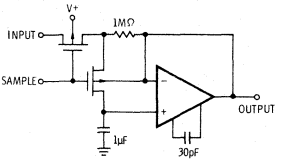
TYPICAL APPLICATIONS

BIAS COMPENSATED LONG TIME INTEGRATOR

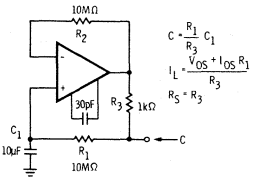


*Adjust R_3 for minimum integrator drift

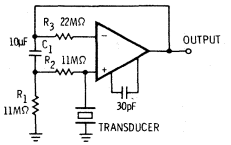
SAMPLE AND HOLD



CAPACITANCE MULTIPLIER

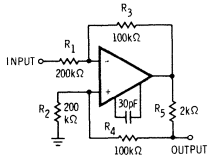


AMPLIFIER FOR CAPACITANCE TRANSDUCERS



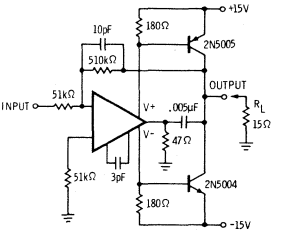
Low Frequency Cutoff $R_1 \times C_1$

BILATERAL CURRENT SOURCE

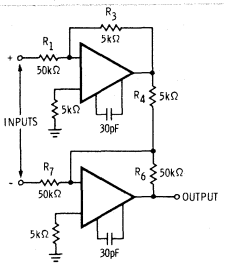


$$I_{OUT} = \frac{R_3 V_{IN}}{R_1 R_5} \; ; \; R_1 = R_2; R_3 = R_4 + R_5$$

HIGH SLEW RATE POWER AMPLIFIER



± 100 V COMMON MODE RANGE INSTRUMENTATION AMPLIFIER



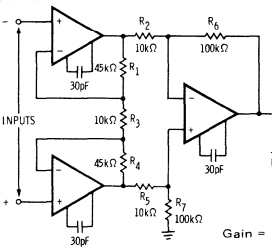
$\frac{R_1}{R_7} \equiv \frac{R_3}{R_4}$ for best CMRR

$R_3 = R_4$

$R_1 = R_6 = 10R_3$

$\text{Gain} = \frac{R_7}{R_6}$

INSTRUMENTATION AMPLIFIER WITH HIGH COMMON MODE REJECTION



$\frac{R_2}{R_5} \equiv \frac{R_6}{R_7}$ for best CMRR

$R_1 = R_4$

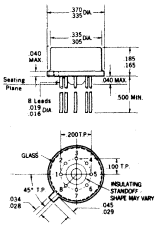
$R_2 = R_5$

$\text{Gain} = \frac{R_6}{R_2}\left(1 + \frac{2R_1}{R_3}\right)$

PHYSICAL DIMENSIONS

METAL CAN
5B PACKAGE

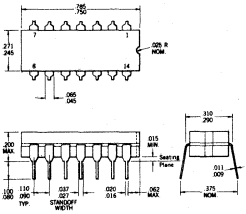
in accordance with JEDEC (TO-99) outline



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.22 grams

CERAMIC DIP
6A PACKAGE

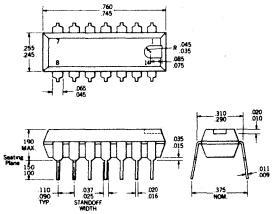
in accordance with JEDEC (TO-116) outline



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams

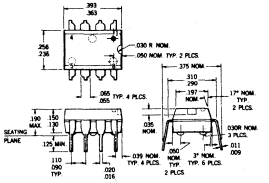
SILICONE DIP
9A PACKAGE

in accordance with JEDEC (TO-116) outline



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for .020 inch diameter lead.
Leads are tin-plated kovar
Package weight is 0.9 gram

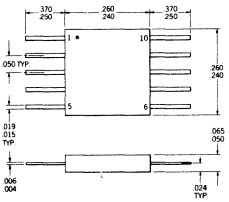
MINI DIP
9T PACKAGE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 0.6 gram
Package material is silicone

FLATPACK
3F PACKAGE

in accordance with JEDEC (TO-91) outline



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.26 gram
Package material is ceramic
Available on special request

FOR INFORMATION ON OTHER FAIRCHILD OPERATIONAL AMPLIFIERS, SEE THE FOLLOWING DATA SHEETS:

HIGH SPEED – μA715, μA715C.
INSTRUMENTATION – μA725, μA725B, μA725C.
TEMPERATURE STABLE PREAMPS – μA727, μA727B.
MICROPOWER – μA735, μA735B, μA735C.
PROGRAMMABLE – μA776, μA776C

FET INPUT – μA740, μA740C.
FREQUENCY COMPENSATED – μA741, μA741C.
DUALS – μA739C, μA749, μA749C, μA747, μA747C.
HIGH PERFORMANCE – μA101, μA201, μA748, μA748C.
PRECISION – μA101A, μA201A, μA301A.

μA780
PHASE LOCKED LOOP
FAIRCHILD LINEAR INTEGRATED CIRCUITS

- **COMPLETE COLOR TV SUBCARRIER REGENERATOR**
- **AUTOMATIC PHASE CONTROL LOOP**
- **DC TINT CONTROL**
- **SYNCHRONOUS ACC/KILLER DETECTOR**
- **COLOR BURST GATING AND BLANKING**
- **INTERNALLY REGULATED SUPPLY**

GENERAL DESCRIPTION – The μA780 is a Phase Locked Loop designed for use as a Color TV Subcarrier Regenerator and is constructed on a single silicon chip using the Fairchild Planar* epitaxial process. This integrated circuit, which uses an Automatic Phase Control (APC) loop, accepts the composite NTSC color video signal, extracts the color subcarrier reference and generates a CW signal suitable for use as a chroma demodulation reference. Other features include control of the CW phase (tint) by a DC voltage, blanking of the CW output during burst time and synchronous generation of an Automatic Color Control (ACC) voltage.

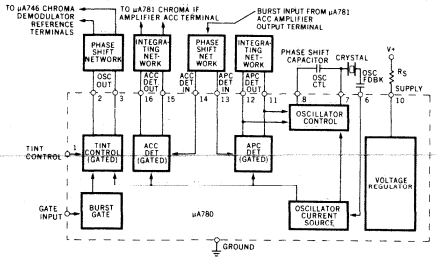
The μA780 in combination with the μA781 Chroma IF Amplifier and the μA746 Chroma Demodulator form a complete low cost, high quality chroma processing system for color TV receivers.

The μA780 is also useful as a communications phase locked loop system to select, amplify and demodulate AM, FM, FSK and SSB signals. For information on μA780 applications and other Fairchild Communications circuits, see listing on last page.

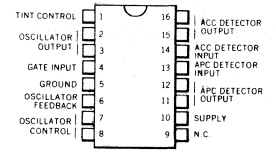
ABSOLUTE MAXIMUM RATINGS

Supply Current	40 mA
Current into Gate Input Terminal	5 mA
Peak-to-Peak Voltage at either APC or ACC Detector Input Terminals	5 V
Internal Power Dissipation	
Ceramic DIP	600 mW
Silicone DIP	500 mW
Storage Temperature Range	
Ceramic DIP	-65°C to + 150°C
Silicone DIP	-55°C to + 125°C
Operating Temperature Range	0°C to + 70°C
Lead Temperature	
Ceramic DIP (Soldering -60 seconds)	300°C
Silicone DIP (Soldering -10 seconds)	260°C

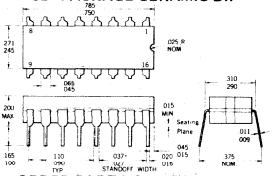
BLOCK DIAGRAM



CONNECTION DIAGRAM
(TOP VIEW)

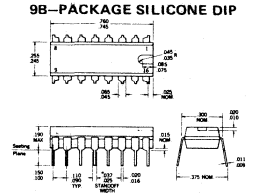


PHYSICAL DIMENSIONS
6B—PACKAGE CERAMIC DIP



ORDER PART NO. U6B7780394

9B—PACKAGE SILICONE DIP



ORDER PART NO. U9B7780394

NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar

Package weight is 2.0 grams for 6B Package and 0.9 for 9B Package

*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR

STATIC ELECTRICAL CHARACTERISTICS (T_A = 25°C, Gate "ON," Test Circuit 1 unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current			26		mA
Voltage at Supply Terminal		11.3	12.0	12.6	V
Supply Regulation	V^+ = 21 V to V^+ = 27 V		40		mV
Total Current into Oscillator Output Terminals	Gate "OFF," 50 k Ω resistor connected between Pin 10 and Pin 6, Pin 2 shorted to Pin 3	4.2	5.8	7.6	mA
Current into either APC Detector Output Terminal	12 k Ω resistor connected between Pin 6 and Ground		12	40	μA
Offset Voltage between ACC Detector Output Terminals (V_{15} -V_{16})	50 k Ω resistor connected between Pin 10 and Pin 6	-330	-70	+300	mV
Offset Voltage between APC Detector Output Terminals (V_{11} -V_{12})	50 k Ω resistor connected between Pin 10 and Pin 6	-315	-50	+315	mV
Offset Voltage between Oscillator Control Terminals (V_7 -V_8)	12 k Ω resistor connected between Pin 6 and Ground, V_{11} = V_{12} = 9.5 V	-330	-20	+330	mV
Offset Voltage between Oscillator Output Terminals (V_2 -V_3)	Gate "OFF"	-200	+300	+800	mV
Voltage at Oscillator Feedback Terminal			2.8		V
Voltage at ACC Detector Input Terminal		6.0	6.5	7.0	V
Voltage at APC Detector Input Terminal		6.0	6.5	7.0	V
Voltage at Tint Control Terminal			200	300	mV
Voltage at Tint Control Terminal	Gate "OFF"	7.3	7.6	8.2	V
Internal Power Dissipation			310	400	mV

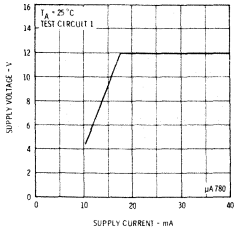
DYNAMIC ELECTRICAL CHARACTERISTICS (T_A = 25°C, peak-to-peak burst level at APC Detector Input Terminal = 200 mV. Standard NTSC Signal, f_o=3.579545 MHz, Test Circuit 2 unless otherwise specified.)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Oscillator Pull-in Range	$f_{free\ run} > f_o$		+510		Hz
	$f_{free\ run} < f_o$		-750		Hz
Oscillator Static Phase Error	$f_{free\ run} = f_o$ + 120 Hz		+2.2		Degree
	$f_{free\ run} = f_o$ - 120 Hz		-2.2		Degree
Oscillator Control Sensitivity			12		Hz/mV
Input Resistance at Oscillator Feedback Terminal			2.2		k Ω
Input Capacitance at Oscillator Feedback Terminal			4.5		pF
Peak-to-Peak Current at Oscillator Output Terminal (Pin 3)	Tint Control Wiper at Ground		6.8		mA
ACC Detector Input Resistance			2.2		k Ω
ACC Detector Input Capacitance			4.5		pF
ACC Detector Sensitivity	100 mV p-p burst level at ACC Detector Input Terminal, Oscillator Locked		+2.2		mV DC/mV p-p
APC Detector Input Resistance			2.2		k Ω
APC Detector Input Capacitance			4.5		pF
APC Detector Sensitivity			5		mV/Degree

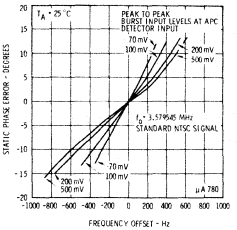
TYPICAL PERFORMANCE CURVES

(Test Circuit 2 unless otherwise specified)

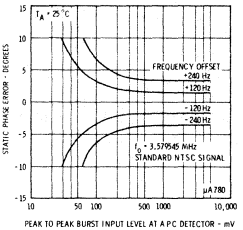
SUPPLY VOLTAGE AS A FUNCTION OF SUPPLY CURRENT



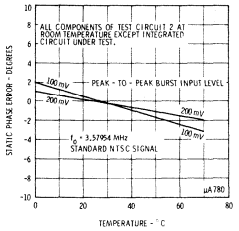
STATIC PHASE ERROR AS A FUNCTION OF FREQUENCY OFFSET



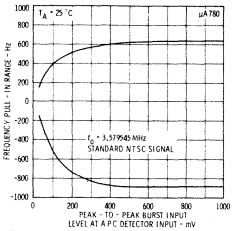
STATIC PHASE ERROR AS A FUNCTION OF BURST INPUT LEVEL



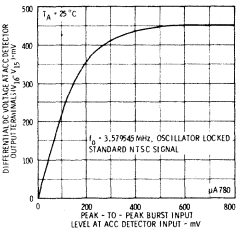
STATIC PHASE ERROR AS A FUNCTION OF TEMPERATURE



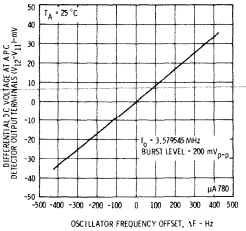
FREQUENCY PULL-IN RANGE AS A FUNCTION OF BURST INPUT LEVEL



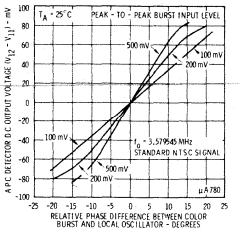
DIFFERENTIAL DC VOLTAGE AT ACC DETECTOR OUTPUT AS A FUNCTION OF BURST INPUT LEVEL



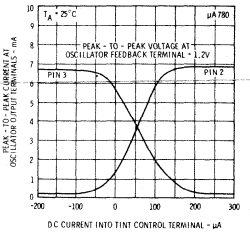
DIFFERENTIAL DC VOLTAGE AT APC DETECTOR OUTPUT TERMINALS AS A FUNCTION OF OSCILLATOR FREQUENCY OFFSET



APC DETECTOR OUTPUT AS A FUNCTION OF RELATIVE PHASE DIFFERENCE

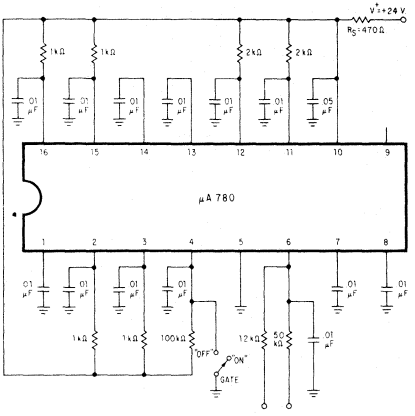


OSCILLATOR OUTPUT AS A FUNCTION OF TINT CONTROL CURRENT

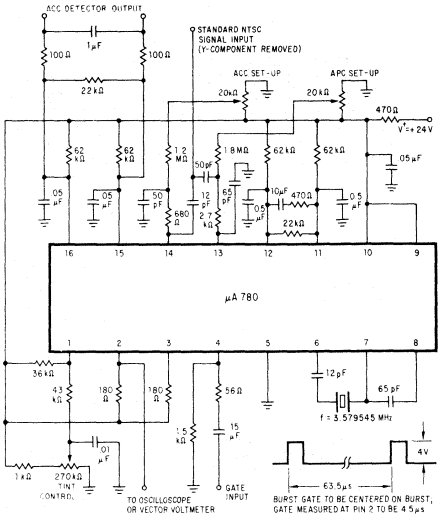


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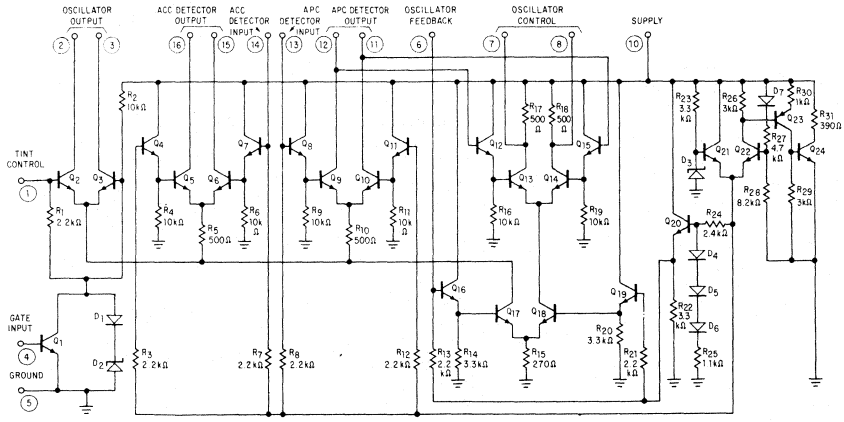
TEST CIRCUIT 1



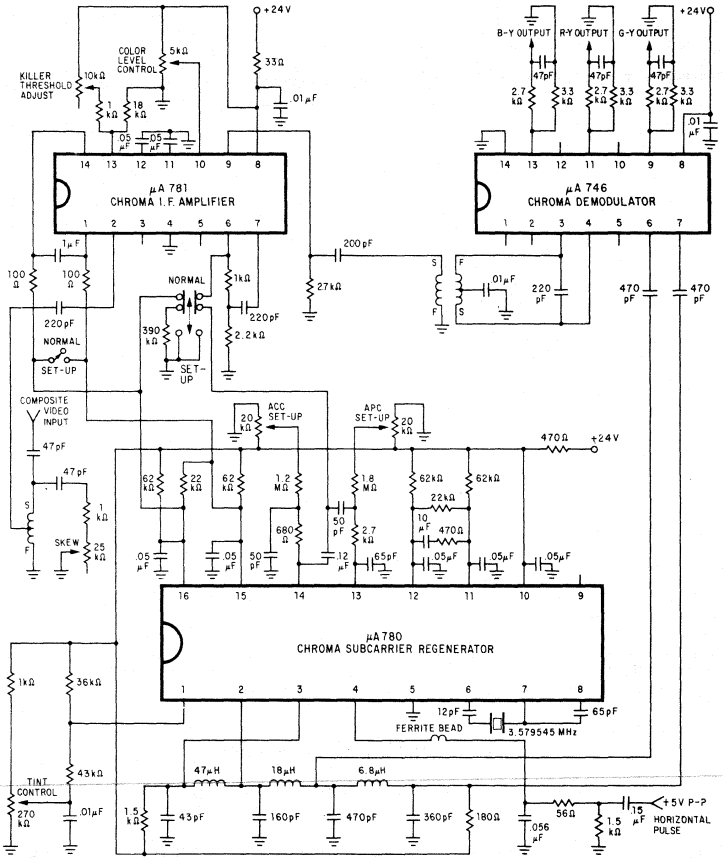
TEST CIRCUIT 2



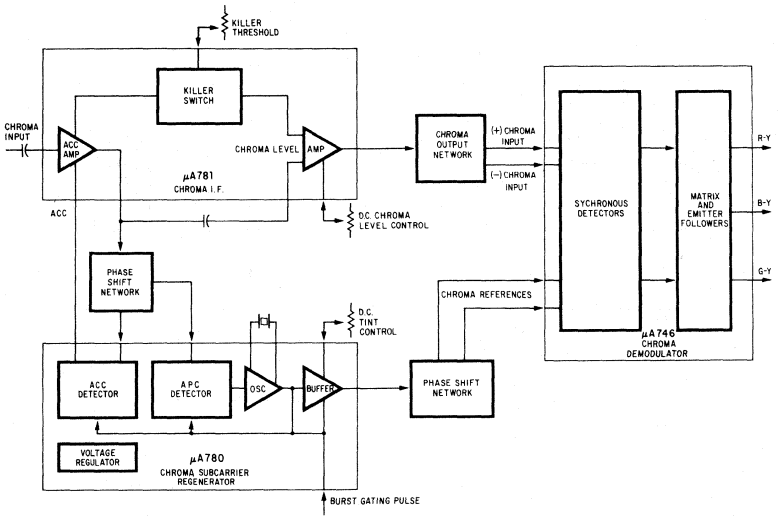
EQUIVALENT CIRCUIT



INTEGRATED CIRCUIT COLOR TV CHROMA PROCESSING SYSTEM
(COMPLETE SCHEMATIC)



INTEGRATED CIRCUIT COLOR TV CHROMA PROCESSING SYSTEM
(BLOCK DIAGRAM)



DEFINITION OF TERMS

SUPPLY REGULATION – The change in voltage at the Supply Terminal for a specified change in the V^+ voltage.

OSCILLATOR CONTROL SENSITIVITY – The ratio of the incremental change in oscillator free running frequency to the incremental change in the differential DC voltage at the APC Detector Output Terminals.

ACC DETECTOR SENSITIVITY – The ratio of the incremental differential DC voltage change at the ACC Detector Output Terminals to the incremental change in peak-to-peak voltage at the ACC Detector Input Terminal for a specified burst input level, with the local oscillator locked.

APC DETECTOR SENSITIVITY – The ratio of the incremental differential DC voltage change at the APC Detector Output Terminals to the incremental change in relative phase at the APC Detector Input Terminal for a specified burst input level.

μA780 APPLICATION INFORMATION

APP210 – THE μA746, μA780, AND μA781 TV CHROMA PROCESSING SYSTEM
AB156 – APPLICATIONS OF THE μA746, μA780, AND μA781 TV CHROMA PROCESSING SYSTEM

FOR INFORMATION ON OTHER FAIRCHILD COMMUNICATIONS CIRCUITS SEE THE FOLLOWING DATA SHEETS:

RF/IF LIMITING AMP – μA703, μA703C, μA703D
AUDIO AMP – μA716C
TV/FM SOUND IF – μA719, μA719C, μA754, μA754C, μA784, μA3065
VIDEO AMPLIFIER – μA733, μA733C, μA751C
STEREO MULTIPLEX DECODER – μA729, μA732, μA767
STEREO AUDIO PREAMP – μA739C, μA749, μA749C, μA749D
DUAL AC AMPLIFIER/OSCILLATOR – μA745
COLOR TV CHROMA PROCESSING –, μA746, μA786
AGC IF AMPLIFIER – μA757, μA757C
TV SIGNAL PROCESSING – μA785
AUTOMATIC FINE TUNING CIRCUIT – μA3064
BALANCED MODULATOR-DEMODULATOR – μA796, μA796C
GAIN CONTROLLED IF AMPLIFIER – μA781
TRANSISTOR AND DIODE ARRAYS – μA3018, μA3018A, μA3019, μA3026, μA3036, μA3045, μA3046, μA3054
VOLTAGE REGULATOR – μA723, μA723C

μA781
GAIN CONTROLLED IF AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUIT

- **COMPLETE COLOR TV CHROMA IF AMP**
- **10 MHz BANDWIDTH**
- **AUTOMATIC COLOR CONTROL (ACC) AMPLIFIER**
- **DC CHROMA LEVEL CONTROL**
- **ADJUSTABLE COLOR KILLER**
- **OUTPUT SHORT CIRCUIT PROTECTION**

GENERAL DESCRIPTION – The μA781 is a dual gain controlled IF amplifier designed for use as a Color TV Chroma IF Amplifier and constructed on a single silicon chip using the Fairchild Planar* epitaxial process. The first section is a gain controlled chroma signal amplifier whose output is used to drive a subcarrier regenerator circuit. The gain of the second section is controlled by means of an external DC voltage to set chroma level. In addition, the second stage may be gated off to provide "color killing" action in the absence of a color signal with the trip point of the gate adjusted externally.

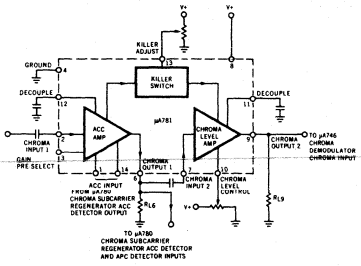
The μA781 in combination with the μA780 Phase Locked Loop Subcarrier Regenerator and the μA746 Chroma Demodulator forms a complete low cost, high quality chroma processing system for color TV receivers.

The μA781 is also useful as a gain-controlled, intermediate-frequency amplifier in AM and FM communication circuits. For information on μA781 applications and other Fairchild Communications circuits, see listing on last page.

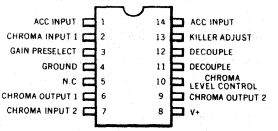
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	30 V
Internal Power Dissipation	600 mW
Storage Temperature Range	
Ceramic DIP	-65°C to + 150°C
Silicone DIP	-55°C to + 125°C
Operating Temperature Range	0°C to + 70°C
Lead Temperature	
Ceramic DIP (Soldering -60 seconds)	300°C
Silicone DIP (Soldering -10 seconds)	260°C
Output Short Circuit Duration	30 seconds

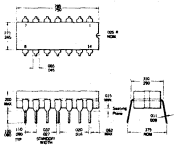
BLOCK DIAGRAM



CONNECTION DIAGRAM

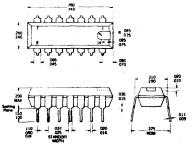


PHYSICAL DIMENSIONS
6A PACKAGE - CERAMIC DIP



ORDER PART NO. U6A7781394

9A PACKAGE - SILICONE DIP



ORDER PART NO. U9A7781394

NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar

Package weight is 2.0 grams for 6A Package, and 0.9 grams for 9A Package

*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR

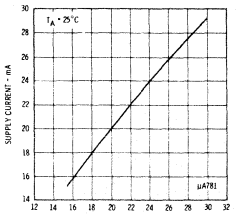
ELECTRICAL CHARACTERISTICS (NOTE 1)

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
Supply Current	$R_{L6} = R_{L9} = 1\ M\Omega$	8	13	18	mA
Supply Current		17	24	31	mA
Internal Power Dissipation			400	550	mW
Short Circuit Load Current, Chroma Output 1	$R_{L6} = 0\ \Omega$	20	42		mA
Short Circuit Load Current, Chroma Output 2	$R_{L9} = 0\ \Omega$	20	36		mA
DC Voltage at Chroma Output 1 Terminal		15.5	17.5	20.0	V
DC Voltage at Chroma Output 2 Terminal		17.5	18.0	18.5	V
Gain, ACC Amplifier Stage		14	17	19	dB
Gain Reduction ACC Amplifier Stage	$V_{ACC} = V_1 - V_{14} = 0$ mV to $V_1 - V_{14} = -75$ mV	12	14	16	dB
Maximum Gain, Chroma Level Amplifier Stage		12	15.8	17	dB
DC Voltage at Chroma Level Control Terminal for 90% Maximum Output Level, Chroma Level Amplifier Stage	Chroma Level Control set for 90% Maximum Output	2.3	3.5	4.8	V
DC Voltage at Chroma Level Control Terminal for 10% Maximum Output Level, Chroma Level Amplifier Stage	Chroma Level Control Wiper set for 10% of Maximum Output	17	19.5	21.7	V
Killer "ON" Threshold			16.6	17.0	V
Killer "OFF" Threshold		16.0	16.3		V
DC Voltage at Decouple Terminal, Pin 11		15	15.5	16	V
DC Voltage at Decouple Terminal, Pin 12		14.5	15.3	16	V
DC Voltage at Gain Preselect Terminal		0.7	1.0	1.2	V
DC Voltage at Chroma Input 1 Terminal			1.7		V
DC Voltage at Chroma Input 2 Terminal			1.4		V
Gain Change with V^+, Chroma Level Amplifier Stage	$V^+ = 24$ V to $V^+ = 21$ V	-1.9	-0.4	1.6	dB
	$V^+ = 24$ V to $V^+ = 27$ V Adjust Input Level at Chroma Input 2 for Output Level = 1.0 V RMS at Maximum Gain. Set Chroma Level Control Wiper for Output Level = 100 mV RMS	-1.9	0.8	1.6	dB
Gain Change with Temperature, Chroma Level Amplifier Stage	$T_A = 25°C$ to $T_A = 70°C$ Adjust Input Level at Chroma Input 2 for Output Level = 1.0 V RMS at Maximum Gain. Set Chroma Level Control Wiper for Output Level = 100 mV RMS		0.7		dB
Chroma Input 1 Resistance			2.4		k Ω
Chroma Input 1 Capacitance			6.2		pF
Chroma Input 2 Resistance			2.4		k Ω
Chroma Input 2 Capacitance			4.2		pF

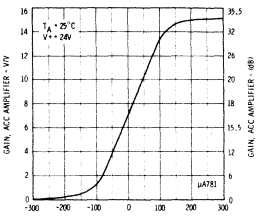
NOTE (1)

$T_A = 25°C$, $V^+ = 24$ V, $R_{L6} = 3.3$ k Ω, $R_{L9} = 2.7$ k Ω, Chroma Level Control Wiper at Ground, Voltage at ACC Input Terminals = 10 V, zero Differential Voltage between ACC Input Terminals, f = 3.58 MHz, Peak-to-peak Input at Chroma Input 1 = 200 mV, Peak-to-peak Input at Chroma Input 2 = 400 mV, unless otherwise specified. Refer to Test Circuit 1.

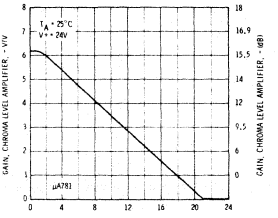
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



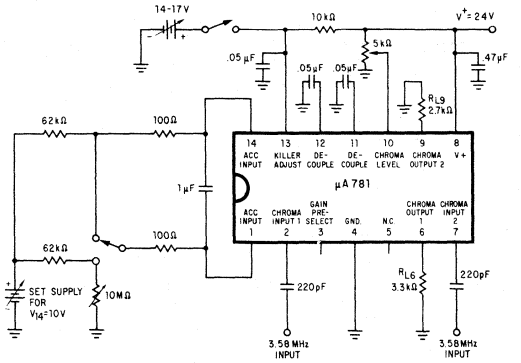
ACC AMPLIFIER GAIN AS A FUNCTION OF DIFFERENTIAL DC VOLTAGE AT ACC INPUT TERMINALS



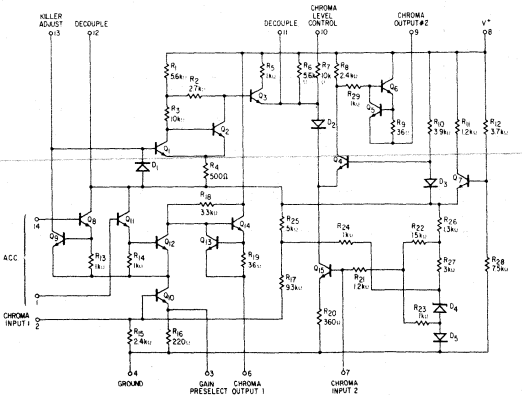
CHROMA LEVEL AMPLIFIER GAIN AS A FUNCTION OF DC VOLTAGE AT CHROMA LEVEL CONTROL TERMINAL



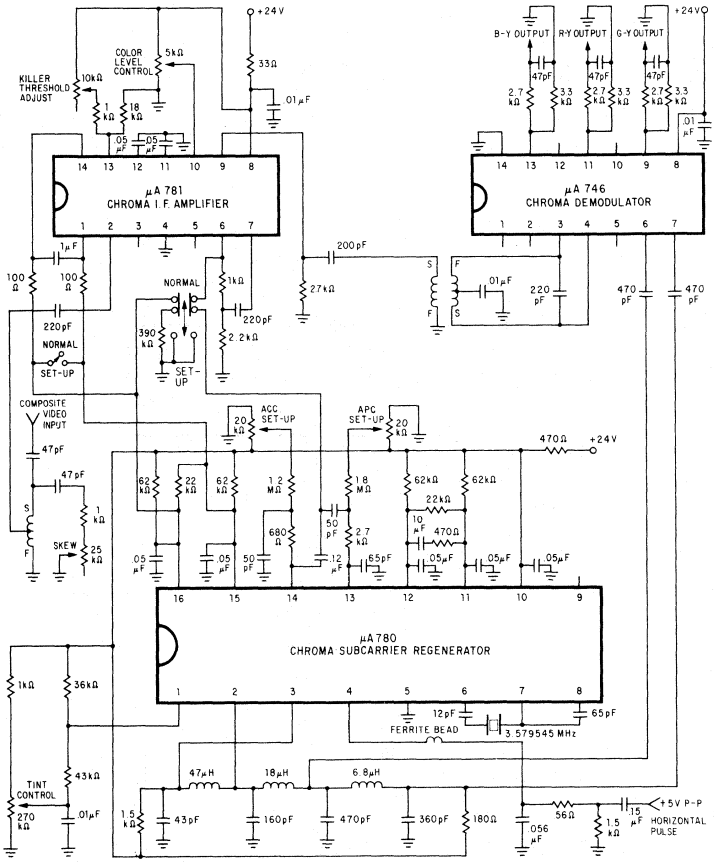
TEST CIRCUIT



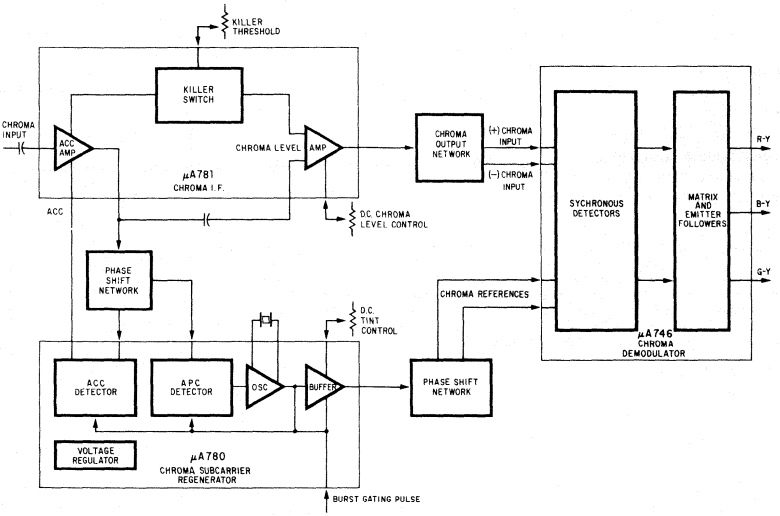
EQUIVALENT CIRCUIT



INTEGRATED CIRCUIT COLOR TV CHROMA PROCESSING SYSTEM



INTEGRATED CIRCUIT COLOR TV CHROMA PROCESSING SYSTEM (BLOCK DIAGRAM)



DEFINITION OF TERMS

SUPPLY REGULATION – The change in voltage at the Supply Terminal for a specified change in the V^+ voltage.

OSCILLATOR CONTROL SENSITIVITY – The ratio of the incremental change in oscillator free running frequency to the incremental change in the differential DC voltage at the APC Detector Output Terminals.

ACC DETECTOR SENSITIVITY – The ratio of the incremental differential DC voltage change at the ACC Detector Output Terminals to the incremental change in peak-to-peak voltage at the ACC Detector Input Terminal for a specified burst input level, with the local oscillator locked.

APC DETECTOR SENSITIVITY – The ratio of the incremental differential DC voltage change at the APC Detector Output Terminals to the incremental change in relative phase at the APC Detector Input Terminal for a specified burst input level.

μA781 APPLICATION INFORMATION

APP210 – THE μA746, μA780, AND μA781 TV CHROMA PROCESSING SYSTEM

AB156 – APPLICATIONS OF THE μA746, μA780, AND μA781 TV CHROMA PROCESSING

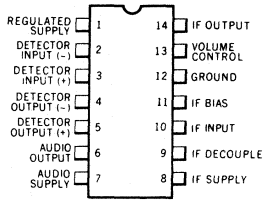
FOR INFORMATION ON OTHER FAIRCHILD COMMUNICATIONS INTEGRATED CIRCUITS, SEE THE FOLLOWING DATA SHEETS:

RF/IF LIMITING AMP – μA703, μA703C, μA703D
AUDIO AMP – μA716C
TV/FM SOUND IF – μA719, μA719C, μA754, μA754C, μA784, μA3065
VIDEO AMPLIFIER – μA733, μA733C, μA751C
STEREO MULTIPLEX DECODER – μA729, μA732, μA767
STEREO AUDIO PREAMP – μA739C, μA749, μA749C, μA749D
DUAL AC AMPLIFIER/OSCILLATOR – μA745
COLOR TV CHROMA PROCESSING – μA746, μA780, μA786
AGC IF AMPLIFIER – μA757, μA757C
TV SIGNAL PROCESSING – μA785
AUTOMATIC FINE TUNING CIRCUIT – μA3064
BALANCED MODULATOR-DEMODULATOR – μA796, μA796C
PHASE LOCKED LOOP – μA780
TRANSISTOR AND DIODE ARRAYS – μA3018, μA3018A, μA3019, μA3026, μA3036, μA3045, μA3046, μA3054
VOLTAGE REGULATOR – μA723, μA723C

μA784
TV/FM SOUND SYSTEM
FAIRCHILD LINEAR INTEGRATED CIRCUITS

- **100 μV SENSITIVITY**
- **44 dB AM REJECTION**
- **DC VOLUME CONTROL**
- **INTERNALLY REGULATED SUPPLY**
- **SINGLE COIL SLOPE DETECTOR**
- **LOW EXTERNAL COMPONENT COUNT**
- **PIN-FOR-PIN REPLACEMENT FOR TAA640**

CONNECTION DIAGRAM
(TOP VIEW)



GENERAL DESCRIPTION

The μA784 is a monolithic TV/FM sound system constructed on a single silicon chip using the Fairchild Planar* epitaxial process. The device consists of a four stage limiting IF amplifier, modified FM slope detector, and an audio preamplifier. The circuit incorporates a dc volume control and may be remotely controlled over a 60 dB range. Excellent sensitivity, high AM rejection, an internally regulated power supply, coupled with low external component count, make the μA784 an ideal choice for TV sound channels and line operated or automobile FM radios. For information on other Fairchild Communications Integrated Circuits, see listing on last pages.

ABSOLUTE MAXIMUM RATINGS

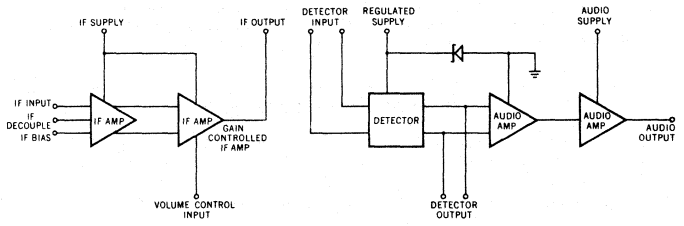
Supply Voltages (Note 1)	V_7	32 V
	V_8	9 V
Supply Currents (Note 1)	$I_1+I_7+I_8$	40 mA
	I_1	28 mA
Internal Power Dissipation (Note 2)		500 mW
Operating Temperature Range		−40°C to +85°C
Storage Temperature Range		
Ceramic DIP		−65°C to +150°C
Silicone DIP		−55°C to +125°C
Lead Temperature (Soldering)		
Ceramic DIP (60 seconds)		300°C
Silicone DIP (10 seconds)		260°C

ORDERING INFORMATION

Ceramic Dual In-Line – U6A784354
Silicone Dual In-Line – U9A784354
Ceramic Quad In-Line – U7F7784354*
Silicone Quad In-Line – U9C7784354*

*Available from factory on special request. See Package dimensions on last page.

BLOCK DIAGRAM



*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS $T_A = 25°C$. See note 3.

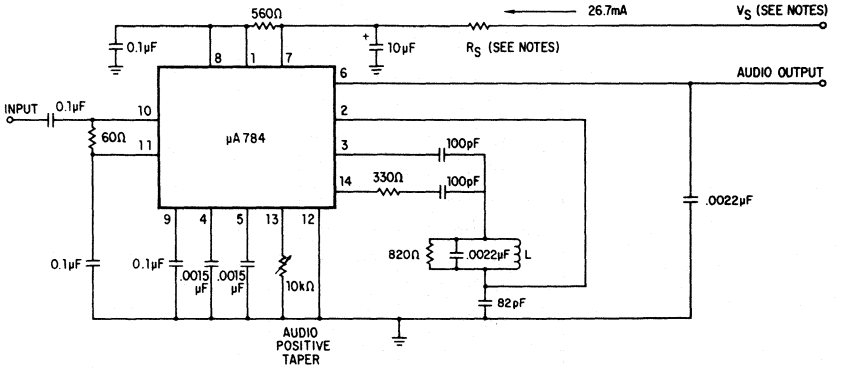
Parameter	Condition	MIN	TYP	MAX	UNITS
Zener Voltage, V_1			7.4	8.5	V
Voltage at Pin 7			22		V
Current at Pin 7			0.7		mA
IF Input Voltage for 3 dB Limiting			100		μV
IF Amplifier Voltage Gain		70	76		dB
IF Output Voltage			1.7		V_{p-p}
AM Rejection	30% AM		44		dB
Audio Output Voltage	Δf = ±50 kHz		1.6		V_{rms}
Total Distortion	Δf = ±15 kHz		1.6		%
	Δf = ±50 kHz			5.0	%
Remote Volume Control Range		60			dB

NOTES:

1. Rating permissible during warmup.
2. Rating applies to +85°C for Ceramic Package. For Silicone Package, rating applies to +45°C. For ambient temperatures above +45°C, derate linearly at 6.2 mW/°C.
3. Test Circuit 1 applicable. Adjust $I_1 + I_7 + I_8$ to equal =26.7 mA. IF input = 5.5 MHz; modulation = ±15 kHz at 1 kHz unless otherwise specified.

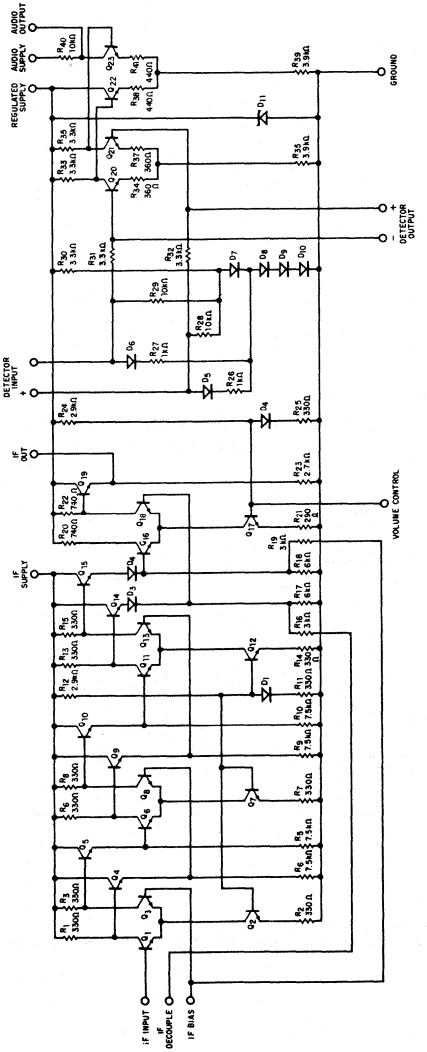
TEST CIRCUIT AND TYPICAL APPLICATION

TV SOUND SYSTEM



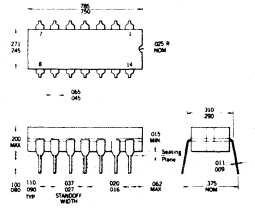
Notes:
1. Adjust V_s and R_s so that I_s = 26.7 mA.
2. Detector coil for 5.5 MHz operation: 6.5 turns 0.5 mm wire; Coil Former: Ferroxcube AP 3016/02 less frame; Can: AP 3015/02; Core: 3122 104 93040.

EQUIVALENT CIRCUIT



PHYSICAL DIMENSIONS

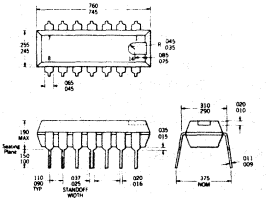
CERAMIC DIP
6A - 14 LEAD DUAL IN-LINE
in accordance with JEDEC (TO-116) outline



NOTES: All dimensions in inches.
Leads are intended for insertion in hole rows on .300" centers.
They are purposely shipped with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for .020 inch diameter lead.
Leads are tin-plated kovar.
Package weight is 2.0 grams.

ORDER PART NO. U6A7784354

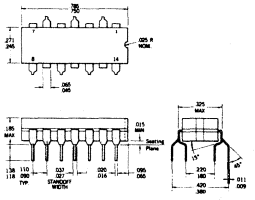
SILICONE DIP
9A - 14 LEAD DUAL IN-LINE
in accordance with JEDEC (TO-116) outline



NOTES: All dimensions in inches.
Leads are intended for insertion in hole rows on .300" centers.
They are purposely shipped with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for .020 inch diameter lead.
Leads are tin-plated kovar.
Package weight is 0.9 grams.

ORDER PART NO. U9A7784354

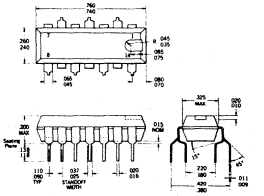
CERAMIC QUIL
7F – 14 LEAD QUAD IN-LINE



NOTES: All dimensions in inches.
This is a "6A" package with leads formed in assembly.
Board-drilling dimensions should equal your practice for .020 inch diameter lead.
Leads are tin-plated kovar.
Package weight is 2.0 grams.

ORDER PART NO. U7F7784354*
*Available from factory on special request

SILICONE QUIL
9C – 14 LEAD QUAD IN-LINE



NOTES: All dimensions in inches.
This is a "9A" package with leads formed in assembly.
Board-drilling dimensions should equal your practice for .020 inch diameter lead.
Leads are gold-plated kovar.
Package weight is 0.9 gram.

ORDER PART NO. U9C7784354*
*Available from factory on special request.

FOR INFORMATION ON OTHER FAIRCHILD COMMUNICATIONS INTEGRATED CIRCUITS, SEE THE FOLLOWING DATA SHEETS:

RF/IF LIMITING AMP – μA703, μA703C, μA703D
AUDIO AMP – μA716C
TV/FM SOUND IF – μA719, μA719C, μA754, μA754C, μA3065
VIDEO AMPLIFIER – μA733, μA733C, μA751C
STEREO MULTIPLEX DECODER – μA729, μA732, μA767
STEREO AUDIO PREAMP – μA739C, μA749, μA749C, μA749D
DUAL AC AMPLIFIER/OSCILLATOR – μA745
COLOR TV CHROMA PROCESSING – μA746, μA781, μA786
AGC IF AMPLIFIER – μA757, μA757C
TV SIGNAL PROCESSING – μA785
AUTOMATIC FINE TUNING CIRCUIT – μA3064
BALANCED MODULATOR-DEMODULATOR – μA796, μA796C
GAIN CONTROLLED IF AMPLIFIER – μA781
TRANSISTOR AND DIODE ARRAYS – μA3018, μA3018A, μA3019, μA3026, μA3036, μA3045, μA3046, μA3054
VOLTAGE REGULATOR – μA723, μA723C

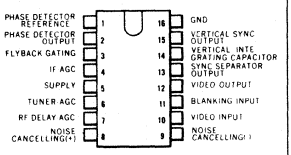
μA785
TV SIGNAL PROCESSING CIRCUIT
FAIRCHILD LINEAR INTEGRATED CIRCUITS

- **VIDEO PREAMPLIFIER WITH EMITTER FOLLOWER OUTPUT**
- **GATED AGC DETECTOR SUPPLYING CONTROL VOLTAGES FOR VIDEO I.F. AGC AND TUNER DELAYED AGC**
- **AUTOMATIC FREQUENCY CONTROL VOLTAGE FOR HORIZONTAL OSCILLATOR**
- **VERTICAL SYNC PULSE SEPARATOR**
- **VIDEO BLANKING FACILITY**
- **NOISE CANCELLATION IN AGC AND SYNC CIRCUITS**
- **PIN FOR PIN REPLACEMENT FOR TAA700**

GENERAL DESCRIPTION – The μA785 is a TV Signal Processing Circuit constructed on a single silicon chip using the Fairchild Planar* Epitaxial process. This device serves as a central processing and distribution circuit for the video, AGC, noise, and synchronization signals for both monochrome and color TV systems including receivers, monitors and cameras. Other applications are in raster-scan alpha-numeric displays, video tape recorders and studio and broadcast equipment. For μA785 applications information, and other Fairchild Communications Integrated circuits, see listing on last page.

CONNECTION DIAGRAM

(TOP VIEW)



ORDERING INFORMATION

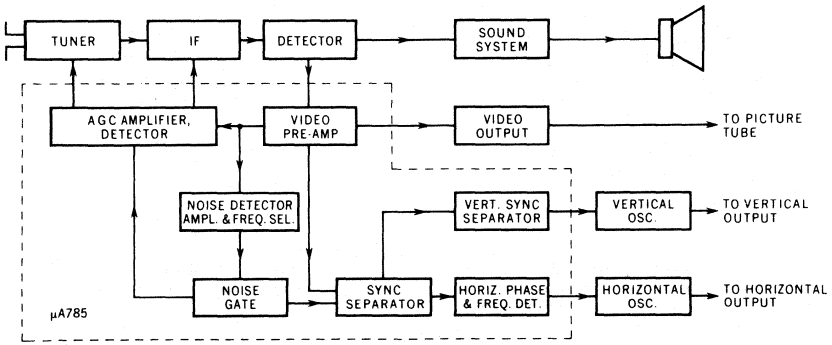
Ceramic Dual-in-line	**U6B7785394**
Silicone Dual-in-line	**U9B7785394**
Ceramic Quad-in-line	**U7H7785394***
Silicone Quad-in-line	**U9D7785394***

*Available on special request.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 1)		16 V
Power Dissipation (Note 2)		600 mW
Operating Temperature Range		-25°C to + 125°C
Storage Temperature Range	Ceramic Dip	-65°C to + 150°C
	Silicone Dip	-55°C to + 125°C
Lead Temperature (Soldering)	Ceramic Dip - 60 Seconds	300°C
	Silicone Dip - 10 Seconds	260°C

BLOCK DIAGRAM



See notes on Page 2

*Planar is a patented Fairchild process.

FAIRCHILD SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_S = + 12 V, Test Circuit 1, unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, I_5	$R_L = \infty$, $V_{10} = 0$		19	25	mA
	R_L = 1 kΩ, $V_{10} = 0$		30		mA
VIDEO PREAMPLIFIER					
Voltage Gain			3.0		V/V
Input Resistance, R_{10}			2.7		kΩ
Input Capacitance, C_{10}				1.0	pF
Bandwidth	-3dB	5.0	14		MHz
Black Level at Video Output	$V_{10} = 2\,V_{P-P}$, Direct Coupled		5.0		V
Video DC Output Voltage, V_{12}	$V_{10} = 0$	8.5	9.8	10.6	V
Tracking of Video Output Voltage with Supply Variation, $\frac{\Delta V_{12}}{\Delta V_5}$	$V_{10} = 0$		0.7		V/V
Peak Video Output Current	(Note 3)		14		mA
Required Video Blanking Input Voltage Pulse, V_{11}	(Note 4)	1.0			V
Required Video Blanking Input Current Pulse, I_{11}	(Note 4)	1.0			mA
Required Flyback Gating Voltage Pulse, V_3	(Note 4)	1.0			V
Required Flyback Gating Current Pulse, I_3	(Note 4)	1.0			mA
AGC CIRCUIT					
Control Voltage at IF AGC Terminal, V_4	$V_{10} = 0V$		0		V
	$V_{10} = -2.5\,V_{DC}$		8.0		V
Control Voltage at Tuner AGC Terminal, V_6	$V_{10} = 0V$		0		V
	$V_{10} = -2.5V_{DC}$		7.0		V
SYNCHRONIZATION CIRCUIT					
AFC Operating Reference Voltage, V_2	$V_1 = 3V_{DC}$, $V_2 = 7\,V_{P-P}$, (Note 5)		7.0		V_{DC}
Vertical Sync Pulse Output, V_{15}		10	11.5		V_{P-P}
Vertical Sync Output Resistance			2.0		kΩ
Slicing Level (Percentage Below Top of Sync Pulse)	(Note 6)		30		%
NOISE GATE					
Amplitude of Noise Pulses Above Sync Tips to Activate Noise Gate	(Note 7)		0.9		V
Minimum Frequency of Noise Pulses to Activate Noise Gate	(Note 7)		3.5		MH_z
Video Input Level to reduce V_8 to 10 V			3.3		V_{PEAK}

NOTES:

(1) Rating permissible during warm-up: however, continuous maximum supply voltage is 14 volts.

(2) Derate linearly at 6.0mW/°C for ambient temperatures above 25°C.

(3) Operation with R_L less than 430 Ω is not recommended.

(4) The μA785 may be operated ungated if pin 3 is connected to the positive supply line via a resistor of a suitable value (e.g. 10 kΩ). However, the following precaution should be taken:
The decoupling capacitors at the i.f. and tuner control points must be larger to prevent ripple voltages due to the vertical sync pulses. As a consequence the AGC will not follow fast input signal fluctuations (airplane flutter). Since the horizontal phase detector is designed to be gated, ungated operation will result in the phase detector not operating as a frequency detector when the horizontal oscillator is out of sync. This considerably decreases the pull-in range.

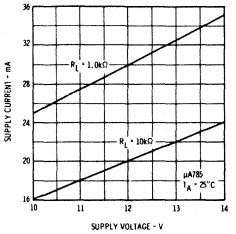
(5) These values apply for an oscillator-reactance stage having a control sensitivity of 400Hz/V. This yields a hold-in range of about ± 1000Hz. If the phase detector is gated a pull-in range of about ± 700Hz is obtained without affecting the noise immunity.

(6) The slicing level is independent of the video input level.

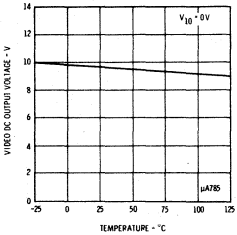
(7) The noise detector of the μA785 is frequency and amplitude selective, i.e., frequencies and noise levels above the values given will turn off the sync and AGC detectors.

TYPICAL PERFORMANCE CURVES
(TEST CIRCUIT 1 UNLESS OTHERWISE SPECIFIED)

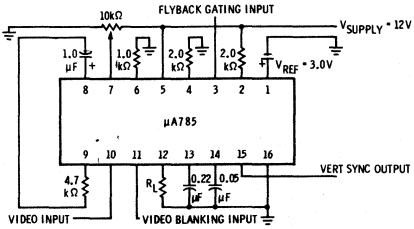
SUPPLY CURRENT VS. SUPPLY VOLTAGE



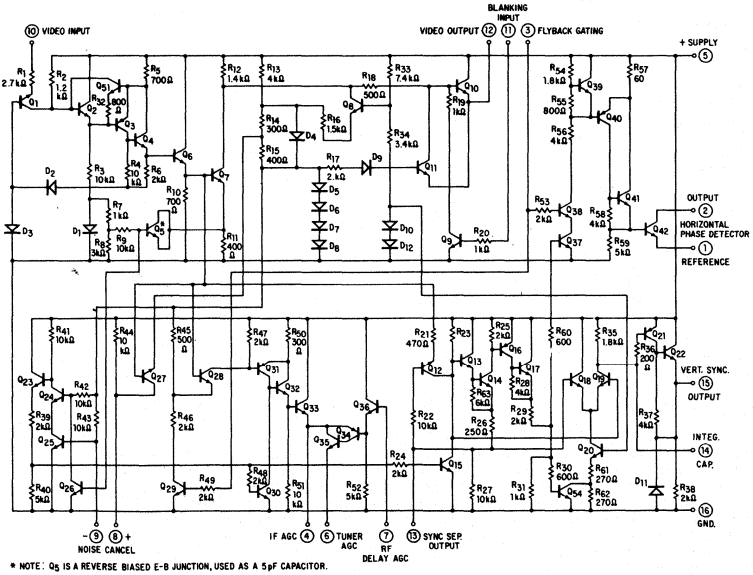
VIDEO DC OUTPUT VOLTAGE VS. TEMPERATURE



TEST CIRCUIT 1

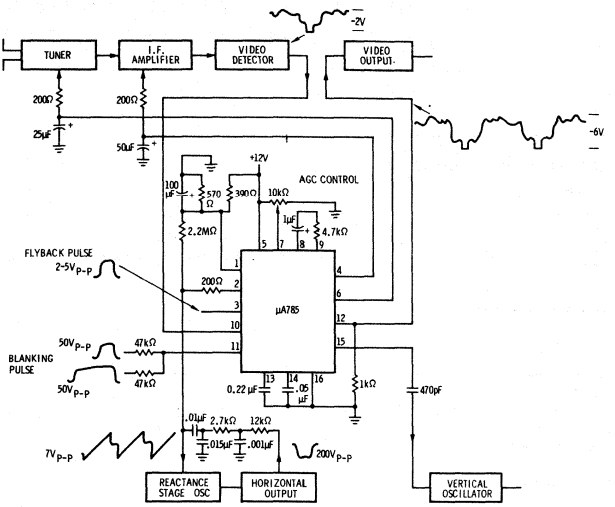


EQUIVALENT CIRCUIT



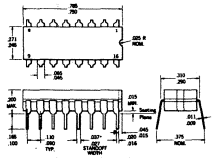
* NOTE: Q_5 IS A REVERSE BIASED E-B JUNCTION, USED AS A 5pF CAPACITOR.

TYPICAL TV RECEIVER APPLICATION



PHYSICAL DIMENSIONS

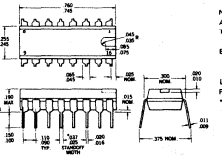
CERAMIC DIP 6B - PACKAGE
16 Lead Dual In-Line



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams
*The .037/.027 dimension does not apply to the corner leads

ORDER NO. U6B7785394

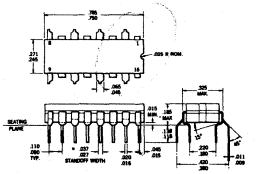
SILICONE DIP 9B - PACKAGE
16 Lead Plastic Dual In-Line



NOTES:
All dimensions in inches
This is a "9B" package with leads formed in assembly
Board-drilling dimensions should equal your practice for a .020 diameter lead
Leads are tin-plated kovar
Package weight is 0.9 gram.
*The .037/.027 dimension does not apply to the corner leads

ORDER NO. U9B7785394

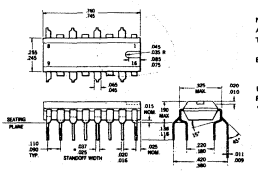
CERAMIC QUIL 7H - PACKAGE
16 Lead Quad In-Line



NOTES:
All dimensions in inches
This is a "9B" package with leads formed in assembly
Board-drilling dimensions should equal your practice for a .020 diameter lead
Leads are tin-plated kovar
Package weight is 0.9 gram.
*The .037/.027 dimension does not apply to the corner leads

ORDER NO. U7H7785394

SILICONE QUIL 9D - PACKAGE
16 Lead Silicone Quad In-Line



NOTES:
All dimensions in inches
This is a "9B" package with leads formed in assembly
Board-drilling dimensions should equal your practice for a .020 diameter lead
Leads are tin-plated kovar
Package weight is 0.9 grams
*The .037/.027 dimension does not apply to the corner leads

ORDER NO. U9D7785394

μA785 APPLICATIONS INFORMATION

AB 170 APPLICATIONS OF THE μA785 TV SIGNAL PROCESSING CIRCUIT

FOR INFORMATION ON OTHER FAIRCHILD COMMUNICATIONS INTEGRATED CIRCUITS, SEE THE FOLLOWING DATA SHEETS:

RF/IF LIMITING AMP—μA703, μA703C. μA703D
AUDIO AMP—μA716C
TV/FM SOUND IF—μA719, μA719C, μA754, μA754C, μA784, μA3065
VIDEO AMPLIFIER—μA733, μA733C, μA751C
STEREO MULTIPLEX DECODER—μA729, μA732, μA767
STEREO AUDIO PREAMP—μA739C, μA749, μA749C, μA749D
DUAL AC AMPLIFIER/OSCILLATOR—μA745
COLOR TV CHROMA PROCESSING—μA746, μA780, μA781, μA786
AGC IF AMPLIFIER—μA757, μA757C
AUTOMATIC FINE TUNING CIRCUIT—μA3064
BALANCED MODULATOR-DEMODULATOR—μA796, μA796C
GAIN CONTROLLED IF AMPLIFIER—μA781
PHASE LOCKED LOOP—μA780
TRANSISTOR AND DIODE ARRAYS—μA3018, μA3018A, μA3019, μA3026, μA3036, μA3045, μA3046, μA3054
VOLTAGE REGULATOR—μA723, μA723C

μA786
PAL COLOR TV CHROMA DEMODULATOR
FAIRCHILD LINEAR INTEGRATED CIRCUIT

- **DOUBLE-BALANCED SYNCHRONOUS DEMODULATOR**
- **INTERNAL DECODING MATRIX**
- **EMITTER FOLLOWER OUTPUTS**
- **INTERNAL PAL SWITCH**
- **INTERNAL COLOR KILLER**
- **PROVISION FOR OUTPUT DC LEVEL MATCHING**
- **PIN-FOR-PIN REPLACEMENT FOR TAA630**

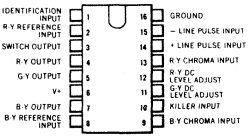
GENERAL DESCRIPTION

The μA786 is a synchronous demodulator for direct drive of color video output stages constructed on a single silicon chip using the Fairchild Planar* epitaxial process. It is designed for use in color television receivers operating on the Phase Alternate Line (PAL) system. The circuit consists of two synchronous demodulators, a decoding matrix, a PAL switch with internal multivibrator, and a color killer switch. For other Fairchild Communications Integrated Circuits, see listing on last page.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 1)	13.2V
Internal Power Dissipation (Note 2)	550mW
Color Difference Output Currents	5 mA
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	
Ceramic DIP	-65°C to +150°C
Silicone DIP	-55°C to +125°C
Lead Temperature (Soldering)	
Ceramic, 60 seconds	300°C
Silicone, 10 seconds	260°C

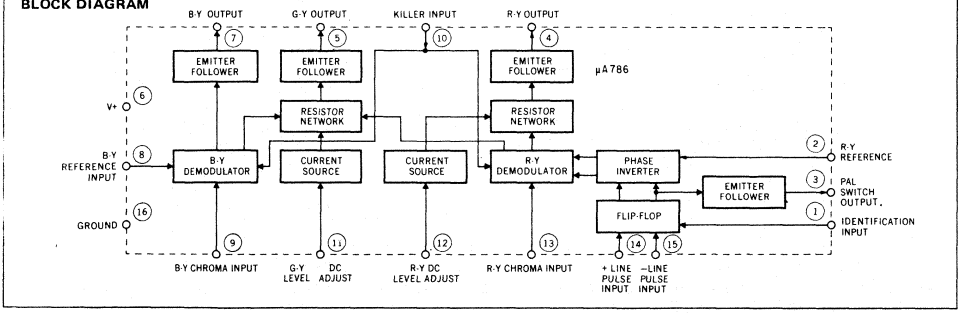
CONNECTION DIAGRAM
(TOP VIEW)



ORDERING INFORMATION

Ceramic Dual In-Line	**U6B7786354**
Silicone Dual In-Line	**U9B7786354**

BLOCK DIAGRAM



*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V+ = 12V, Test Circuit 1, unless otherwise specified. See Note 3)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current (I_6)			33	40	mA
DC Voltage at B-Y Output	(NOTE 4)	6.8	7.4	7.8	V
Output Resistance at Color Difference Terminals (R_4, R_5, R_7)				100	Ω
Color Difference Gain					
R-Y Channel			7.0		V/V
B-Y Channel			12.5		V/V
G-Y Channel			(NOTE 5)		
Maximum Color Difference Output Voltage	(NOTE 6)				
R-Y Output (V_4)			3.2		Vp-p
B-Y Output (V_7)			4.0		Vp-p
G-Y Output (V_5)			1.8		Vp-p
Input Resistance of Chroma Inputs (R_9, R_{13})			1000		Ω
Input Capacitance of Chroma Inputs (C_9, C_{13})			10		pF
DC Voltage at Chroma Inputs (V_9, V_{13})			3.2		V
Input Resistance of Reference Input (R_2, R_8)			900		Ω
DC Voltage at Reference Inputs (V_2, V_8)			2.2		V
Color Killer Voltage Threshold (V_{10})					
Color "ON"				0.9	V
Color "OFF"		0.3			V
Peak-To-Peak PAL Switch Output Voltage (V_3)		2.0	3.0		Vp-p

NOTES:

1.) 16 volts is permissible during warmup.

2.) Rating applies for ambient temperatures to +85°C. For silicone DIP, rating applies for ambient temperatures to +35°C. Derate linearly at 6.2 mW/°C above +35°C. 800 mW dissipation is permissible for either package during warmup.

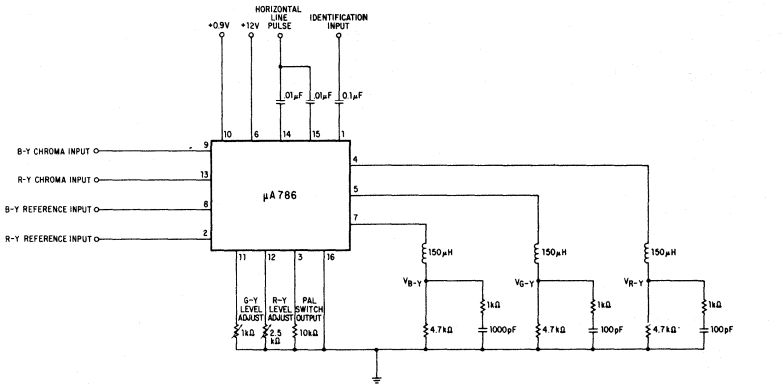
3.) Killer Voltage, V_{10} = 0.9V; Reference Voltages V_2 and V_8 = 1Vp-p @ 4.4 MHz, V_2 leads by 90°; Line Input Pulses, V_{14} and V_{15} = -2.5V peak; Chroma Input Voltages V_9 and V_{13} = 50 mVp-p; Identification Input Voltage, V_1 = 4Vp-p.

4.) DC Output Levels at R-Y and G-Y outputs are adjustable to B-Y level with a variable voltage ($V \leqslant 1.2V$) or with variable resistors connected between pins 11 and 12 to ground. See typical application.

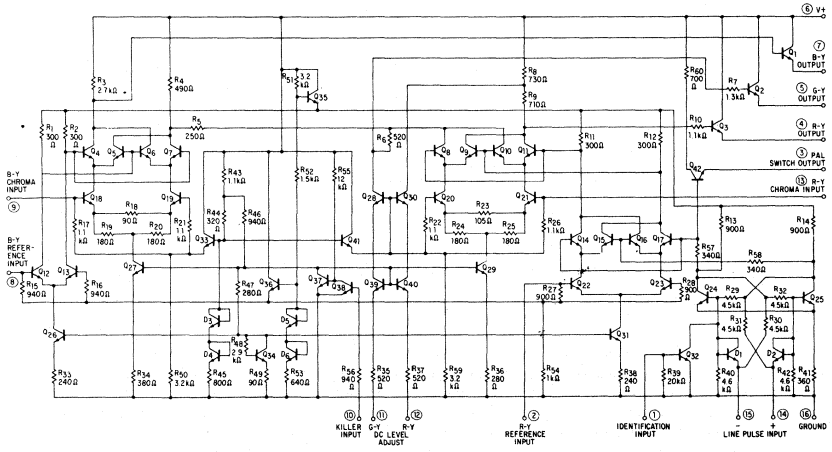
5.) G-Y Output is typically equal to 0.51(R-Y) -0.19(B-Y).

6.) Gain Linearity is greater than 0.7.

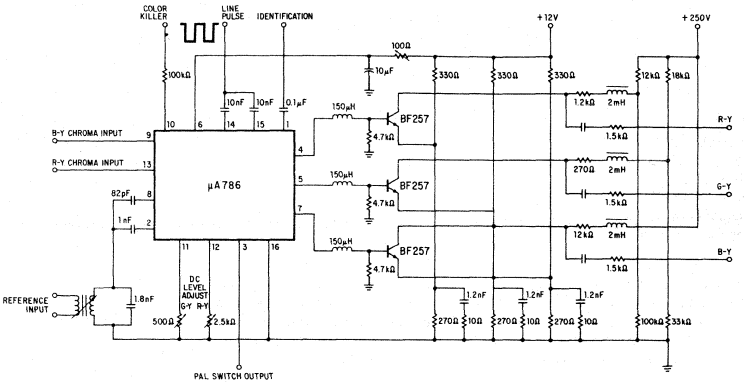
TEST CIRCUIT 1



EQUIVALENT CIRCUIT

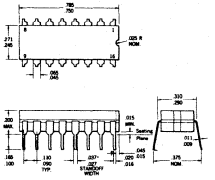


TYPICAL APPLICATION – PAL COLOR TV SYSTEM



PHYSICAL DIMENSIONS

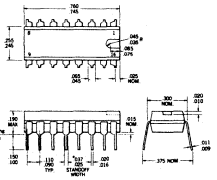
CERAMIC DIP
6B – 16 LEAD DUAL IN-LINE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams
*The .037/.027 dimension does not apply to the corner leads

ORDER PART NO. U6B7786354

SILICON DIP
9B – 16 LEAD DUAL IN-LINE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for .002 inch diameter lead
Leads are tin-plated Kovar
Package weight is 0.9 gram
*The .037/.027 dimension does not apply to the corner leads.

ORDER PART NO. U9B7786354

FOR INFORMATION ON OTHER FAIRCHILD COMMUNICATIONS INTEGRATED CIRCUITS, SEE THE FQLLOWING DATA SHEETS:

RF/LIMITING AMP—μA703, μA703C, μA703D

AUDIO AMP—μA716C

TV/FM SOUND IF—μA719, μA719C, μA754, μA784C, μA3065

VIDEO AMPLIFIER—μA733, μA733C, μA751C

STEREO MULTIPLEX DECODER—μA729, μA732, μA767

STEREO AUDIO PREAMP—μA739C, μA749, μA749C, μA749D

DUAL AC AMPLIFIER/OSCILLATOR—μA745

COLOR TV CHROMA PROCESSING—μA746, μA781

AGC IF AMPLIFIER—μA757, μA757C

TV SIGNAL PROCESSING—μA785

AUTOMATIC FINE TUNING CIRCUIT—μA3064

BALANCED MODULATOR-DEMODULATOR—μA796, μA796C

GAIN CONTROLLED IF AMPLIFIER—μA781

TRANSISTOR AND DIODE ARRAYS—μA3018, μA3018A, μA3019, μA3026, μA3036, μA3045, μA3046, μA3054

VOLTAGE REGULATOR—μA723, μA723C

μA795C
FOUR QUADRANT MULTIPLIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

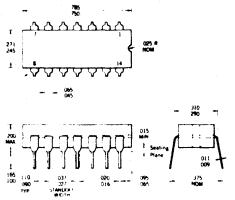
- **EXCELLENT LINEARITY**
- **HIGH INPUT VOLTAGE RANGE**
- **WIDE SUPPLY VOLTAGE OPERATION**
- **WIDE BANDWIDTH**
- **EXCELLENT PHASE MATCHING**
- **ADJUSTABLE GAIN FACTOR**
- **EXCELLENT TEMPERATURE STABILITY**

GENERAL DESCRIPTION — The μA795C is a four Quadrant Analog Multiplier constructed on a single silicon chip using the Fairchild Planar* epitaxial process. The μA795C provides excellent linearity and operates over a wide supply range and input voltage range. The differential output current is the product of two input analog voltages multiplied by a pre-determined scale factor. The μA795C is ideally suited for applications as a multiplier, squarer, divider, phase detector, frequency doubler or balanced modulator.

ABSOLUTE MAXIMUM RATINGS

Applied Voltage (Note 1)	30 V
Differential Input Signal	$V_9 - V_{12} = \pm(6 + I_{13} R_x)$ $V_4 - V_8 = \pm(6 + I_3 R_y)$
Maximum Bias Current	10 mA
Power Dissipation (Note 2)	500 mW
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (soldering, 60 seconds)	300°C

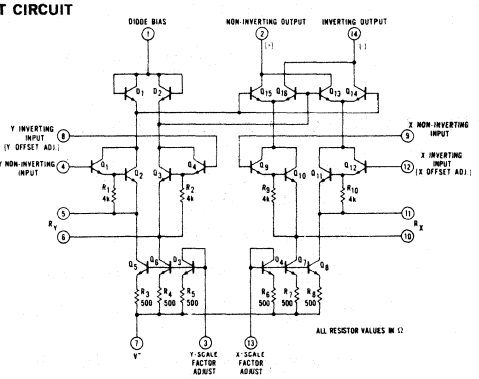
PHYSICAL DIMENSIONS
In accordance with JEDEC (TO-116) outline



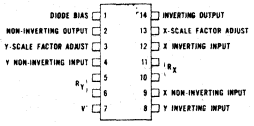
NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for .020 inch diameter lead.
Leads are gold-plated kovar
Package weight is 0.9 gram

ORDER PART NO. U6A7795393

EQUIVALENT CIRCUIT



CONNECTION DIAGRAM



NOTES:
(1) Voltage applied between pins 2-1, 14-1, 1-9, 1-12, 1-4, 1-8, 12-7, 9-7, 8-7, 4-7.
(2) Applies for ambient temperature to 70°C.

*Planar is a patented Fairchild process.

FAIRCHILD SEMICONDUCTOR

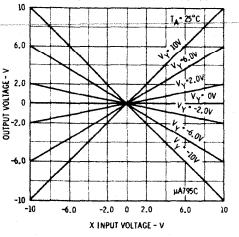
ELECTRICAL CHARACTERISTICS (Note 3; $T_A = 25°C$ unless otherwise specified)

PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Linearity Error in % Of Full Scale	$-10 < V_X < +10$	$V_Y = +10\,V$		1.0	2.0	%
	$-10 < V_X < +10$	$V_Y = -10\,V$		2.0		%
	$-10 < V_Y < +10$	$V_X = +10\,V$		2.0	4.0	%
	$-10 < V_Y < +10$	$V_X = -10\,V$		2.0	4.0	%
Squaring Mode Error				0.75		%
Scale Factor (Adjustable $K = \frac{2\,R_L}{I_3\,R_X\,R_Y}$				0.1		—
Input Resistance	$f = 20$ Hz			20		MΩ
Differential Output Resistance	$f = 20$ Hz			300		kΩ
Input Bias Current				2.0	12	μA
Input Offset Current				0.4	2.0	μA
Frequency Response	−3 dB Bandwidth			3.0		MHz
	3° Relative Phase Shift			750		kHz
	1% Absolute Error Due to Input-Output Phase Shift			30		kHz
Input Voltage Range			±10.5	±12		V
Common Mode Gain			−40	−50		dB
Output Common Mode Voltage				21		V
Differential Output Voltage Swing				±14		V
Positive Supply Voltage Rejection Ratio				5.0		mV/V
Negative Supply Voltage Rejection Ratio				10		mV/V
Negative Supply Current				6.0	7.0	mA
Power Consumption				135	170	mW
The following specifications apply for $0°C \leq T_A \leq +70°C$:						
Linearity Error in % Of Full Scale	$-10 < V_X < +10$	$V_Y = +10\,V$		1.5		%
	$-10 < V_X < +10$	$V_Y = -10\,V$		3.0		%
	$-10 < V_Y < +10$	$V_X = +10\,V$		3.0		%
	$-10 < V_Y < +10$	$V_X = -10\,V$		3.0		%
Squaring Mode Error				1.0		%
Average Temperature Coefficient Of Input Offset Current				2.0		nA/°C

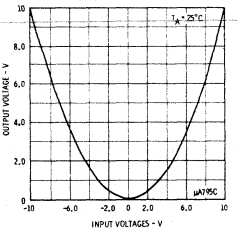
Note 3: Connected as shown in Figure 1, set up 1, with resistor values as shown.

TYPICAL CHARACTERISTICS

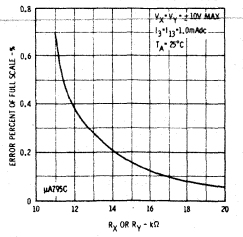
FOUR-QUADRANT MULTIPLIER TRANSFER CHARACTERISTIC



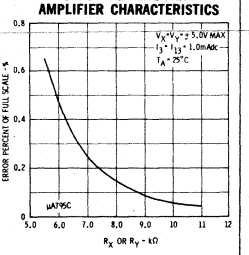
SQUARING MODE TRANSFER CHARACTERISTIC



ERROR CONTRIBUTED BY INPUT DIFFERENTIAL AMPLIFIER CHARACTERISTICS

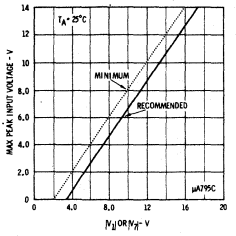


ERROR CONTRIBUTED BY INPUT DIFFERENTIAL AMPLIFIER CHARACTERISTICS

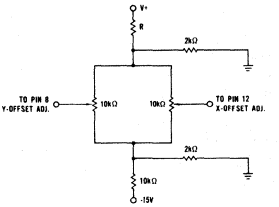


TYPICAL CHARACTERISTICS

MAXIMUM ALLOWABLE INPUT VOLTAGE VERSUS OUTPUT VOLTAGE (PIN 1 OR PIN 7)



OFFSET ADJUSTMENT

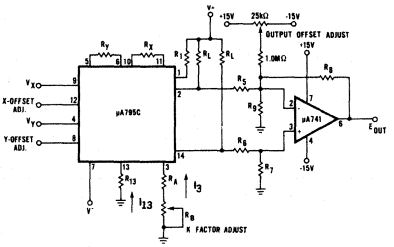


for V+ = 15 V, R = 10 kΩ
V+ = 32 V, R = 22 kΩ

For best output accuracy, use above network; see RECOMMENDED ZERO ADJUST AND SCALE SETTING PROCEDURE on back page.

TYPICAL APPLICATIONS

MULTIPLY WITH OP-AMP LEVEL SHIFT



SET UP	RESISTOR* / TOLERANCE	R_1 5%	R_5 1%	R_6 1%	R_7 1%	R_8 1%	R_9 1%	R_{13} 1%	R_A 5%	R_B 20%	R_L 0.5%	R_X 5%	R_Y 5%
1	V+ = +32 V, V− = −15 V −10 V ≤ V_X ≤ +10 V −10 V ≤ V_Y ≤ +10 V	9.1	121	100	11	121	15	13.7	12	5.0	11	15	15
2	V+ = +15 V, V− = −15 V −5 V ≤ V_X ≤ +5 V −5 V ≤ V_Y ≤ +5 V	3.0	300	100	100	300	∞	13.7	12	5.0	3.4	8.2	8.2
3	V+ = +15 V, V− = −15 V −10 V ≤ V_X ≤ +10 V −10 V ≤ V_Y ≤ +10 V	1.2	121	100	11	910	13.7	13.7	12	5.0	1.5	15	15

*All resistors are k ohms

Figure 1

TYPICAL APPLICATIONS

DIVIDE AND SQUARE ROOT

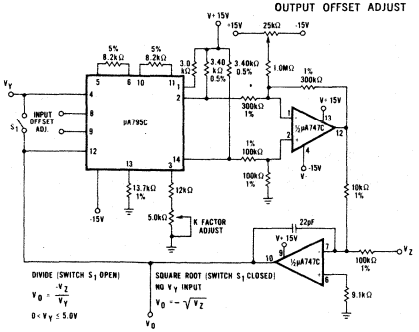


Figure 2

FREQUENCY DOUBLER

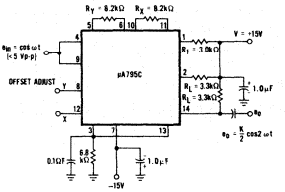


Figure 3

DEFINITIONS

INPUT BIAS CURRENT — The average of the two currents in either pair of grounded inputs.
INPUT OFFSET CURRENT — The difference of the input bias currents in either pair.
INPUT RESISTANCE — The resistance looking into any input terminal with all other inputs grounded.
SCALE FACTOR — An adjustable constant $K = \frac{2 R_L}{I_3 R_X R_Y}$
INPUT VOLTAGE RANGE — A range of voltage, if exceeded on any input terminal, could cause the multiplier to cease functioning properly.
COMMON MODE GAIN — A ratio of the differential output voltage to the change in applied input common mode voltage.
OUTPUT COMMON MODE VOLTAGE — The average voltage at the output terminals with the inputs grounded.
DIFFERENTIAL OUTPUT VOLTAGE SWING — The largest differential voltage that can be obtained.
SUPPLY VOLTAGE REJECTION RATIO — The ratio of the change in input offset voltage to the change in supply voltage producing it.
NEGATIVE SUPPLY CURRENT — The current coming out of the V^- terminal.
POWER CONSUMPTION — The power which is dissipated on the chip.
LINEARITY ERROR — The deviation from the theoretical response.

RECOMMENDED ZERO ADJUST AND SCALE SETTING PROCEDURE

With $V_X = V_Y = 0$ volts adjust the output offset adjustment until the output of the external amplifier reads zero volts. Set $V_X = 5.000$ volts, $V_Y = 0.000$ volt and adjust the Y-input offset control until the output amplifier reads zero volts. Repeat this procedure for $V_X = 0.000$ volt, $V_Y = 5.000$ volts and adjust the X-input offset control until the output amplifier reads zero volts. This procedure should be repeated until complete null is achieved.
Next, set $V_X = V_Y = 5.000$ volts and adjust the K factor potentiometer until the output reads the desired output.
$V_{out} = 2.500V = K V_X V_Y$ for a K factor of .100.
When a high degree of accuracy is unnecessary for small output signals, the above procedure may be simplified by eliminating the output offset adjustment.

SUGGESTIONS AND GENERAL PRECAUTIONS

The high frequency performance of the μA795C is primarily determined by two conditions. One, by the load resistors and the associated stray output capacitance of the multiplier and two, the operational amplifier used at the output. For maximum frequency of operation, low value load resistors and a μA715 wideband high slew rate operational amplifier should be used.

Phase shift at higher frequencies due to load resistors and output stray capacitances and relative phase shift between X and Y channels should be considered for maximum accuracy. As an example if the input to output phase shift is only 0.6°, the output product of two sine waves will exhibit a vector error of 1%. A 3° relative phase shift between the input signals will result in a vector error of 5%.

The normal circuit precautions should be taken to avoid parasitic oscillation. Leads should be as short as possible and the power supplies should be decoupled with a 0.1 μF high frequency capacitor. An RC parasitic suppression network of 510 Ω in series with a 10 pF from each input to ground can be used to reduce the Q_2 of a source-tuned circuit, which may cause the oscillation. As an alternate solution, a 510Ω resistor network can be placed in series with each input of the μA795C.

μA796

DOUBLE-BALANCED MODULATOR/DEMODULATOR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA796 is a monolithic Double-Balanced Modulator/Demodulator constructed on a single silicon chip using the Fairchild Planar® epitaxial process. This circuit produces an output voltage which is the product of an input voltage (signal) and a switching function (carrier). Communications applications include modulation and demodulation of AM, SSB, DSB, FSK, FM and phase encoded signals. Signal conditioning techniques possible include frequency doubling and halving, linear mixing and chopping, with additional uses as phase detectors in phase locked loops and as differentiators in NRZ and phase encoded digital tape and disk memories.

(For μA796 applications information and other Fairchild Communications Integrated Circuits, see listing on last page.)

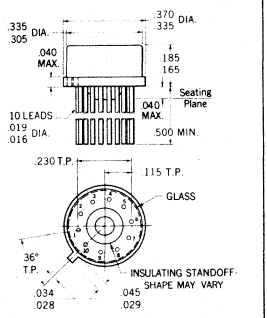
- **EXCELLENT CARRIER SUPPRESSION**
- **LOW OFFSETS AND DRIFT**
- **FULLY BALANCED INPUTS AND OUTPUT**
- **USEFUL TO 100 MHz**
- **WIDE RANGE OF APPLICATION**

ABSOLUTE MAXIMUM RATINGS

Internal Power Dissipation (Note 1)	500 mW
Applied Voltage (Note 2)	30 V
Differential Input Signal ($V_7 - V_8$)	±5.0 V
Differential Input Signal ($V_4 - V_1$)	$\pm(5+I_5R_e)$ V
Input Signal ($V_2 - V_1$, $V_3 - V_4$)	5.0 V
Bias Current (I_5)	12 mA
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	300°C

PHYSICAL DIMENSIONS

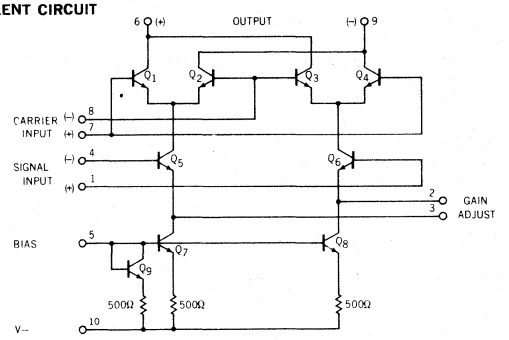
In accordance with JEDEC (TO-100) outline



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.32 grams

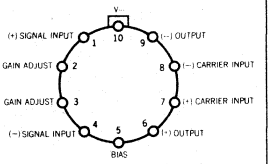
ORDER PART NO. U5E7796312

EQUIVALENT CIRCUIT



CONNECTION DIAGRAM

(TOP VIEW)



Pin 10 electrically connected to case through substrate.

NOTES:
(1) Rating applies to Case Temperatures to +125°C; derate linearly at 6.5 mW/°C for Ambient Temperature above 75°C.
(2) Voltage applied between pins 6-7, 8-1, 9-7, 9-8, 7-4, 7-1, 8-4, 6-8, 2-5, 3-5.

*Planar is a patented Fairchild process.

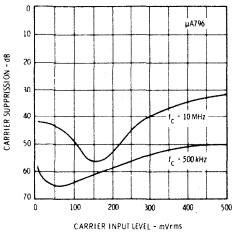
FAIRCHILD SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, Figure 1 unless otherwise specified)

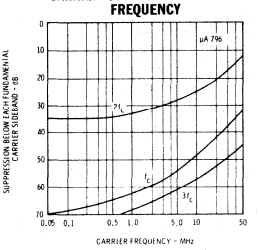
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Carrier Feedthru	$V_C = 60$ mV (rms) sine wave $f_C = 1.0$ kHz, offset adjusted		40		μV (rms)
	$V_C = 60$ mV (rms) sine wave $f_C = 10$ MHz, offset adjusted		140		μV (rms)
	$V_C = 300$ mV_{p-p} square wave $f_C = 1.0$ kHz, offset adjusted		0.04	0.2	mV (rms)
	$V_C = 300$ mV_{p-p} square wave $f_C = 1.0$ kHz, offset not adjusted		20	100	mV (rms)
Carrier Suppression	$f_S = 10$ kHz, 300 mV (rms) $f_C = 500$ kHz, 60 mV (rms) sine wave offset adjusted	50	65		dB
	$f_S = 10$ kHz, 300 mV (rms) $f_C = 10$ MHz, 60 mV (rms) sine wave offset adjusted		50		dB
Transadmittance Bandwidth	$R_L = 50\ \Omega$ Carrier Input Port, $V_C = 60$ mV (rms) sine wave $f_S = 1.0$ kHz, 300 mV (rms) sine wave		300		MHz
	Signal Input Port, $V_S = 300$ mV (rms) sine wave $V_7 - V_8 = 0.5$ V dc		80		MHz
Voltage Gain, Signal Channel	$V_S = 100$ mV (rms), $f = 1.0$ kHz $V_7 - V_8 = 0.5$ V dc	2.5	3.5		V/V
Input Resistance, Signal Port	$f = 5.0$ MHz $V_7 - V_8 = 0.5$ V dc		200		kΩ
Input Capacitance, Signal Port	$f = 5.0$ MHz $V_7 - V_8 = 0.5$ V dc		2.0		pF
Single Ended Output Resistance	$f = 10$ MHz		40		kΩ
Single Ended Output Capacitance	$f = 10$ MHz		5.0		pF
Input Bias Current	$(I_1 + I_4)/2$		12	25	μA
Input Bias Current	$(I_7 + I_8)/2$		12	25	μA
Input Offset Current	$(I_1 - I_4)$		0.7	5.0	μA
Input Offset Current	$(I_7 - I_8)$		0.7	5.0	μA
Average Temperature Coefficient of Input Offset Current	$(-55°C < T_A < +125°C)$		2.0		nA/°C
Output Offset Current	$(I_6 - I_9)$		14	50	μA
Average Temperature Coefficient of Output Offset Current	$(-55°C < T_A < +125°C)$		90		nA/°C
Signal Port Common Mode Input Voltage Range	$f_S = 1.0$ kHz		5.0		V_{p-p}
Signal Port Common Mode Rejection Ratio	$V_7 - V_8 = 0.5$ V dc		−85		dB
Common Mode Quiescent Output Voltage			8.0		Vdc
Differential Output Swing Capability			8.0		V_{p-p}
Positive Supply Current	$(I_6 + I_9)$		2.0	3.0	mA
Negative Supply Current	(I_{10})		3.0	4.0	mA
Power Dissipation			33		mW

TYPICAL PERFORMANCE CURVES

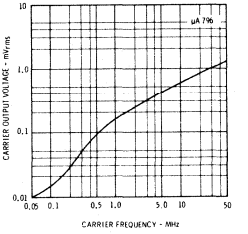
CARRIER SUPPRESSION VERSUS CARRIER INPUT LEVEL



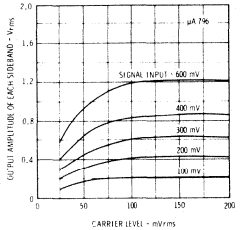
CARRIER SUPPRESSION VERSUS FREQUENCY



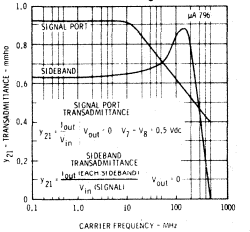
CARRIER FEEDTHROUGH VERSUS FREQUENCY



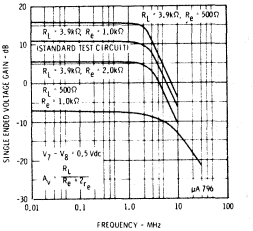
SIDEBAND OUTPUT VERSUS CARRIER LEVELS



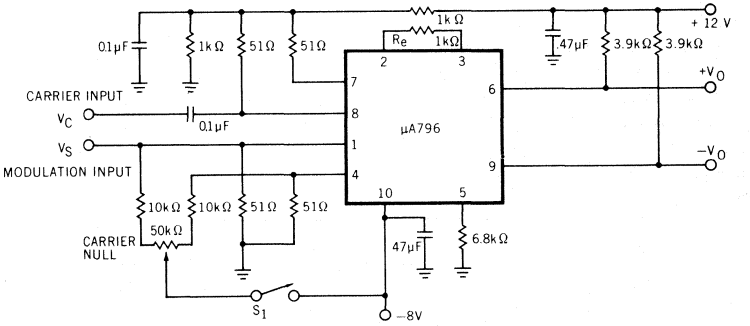
SIDEBAND AND SIGNAL PORT TRANSADMITTANCES VERSUS FREQUENCY



SIGNAL-PORT FREQUENCY RESPONSE



TYPICAL MODULATOR CIRCUIT

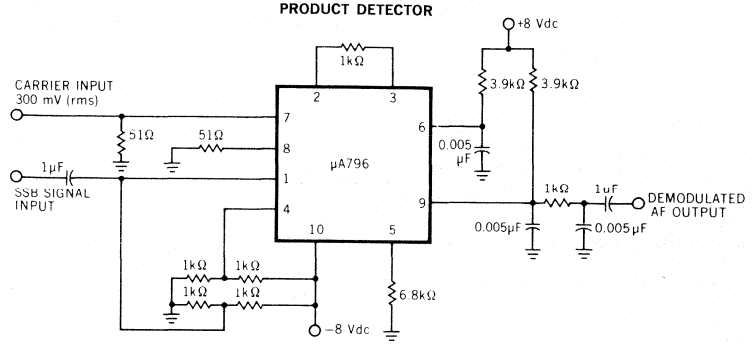


Note: S_1 is closed for "adjusted" measurements.

Fig. 1

TYPICAL APPLICATIONS

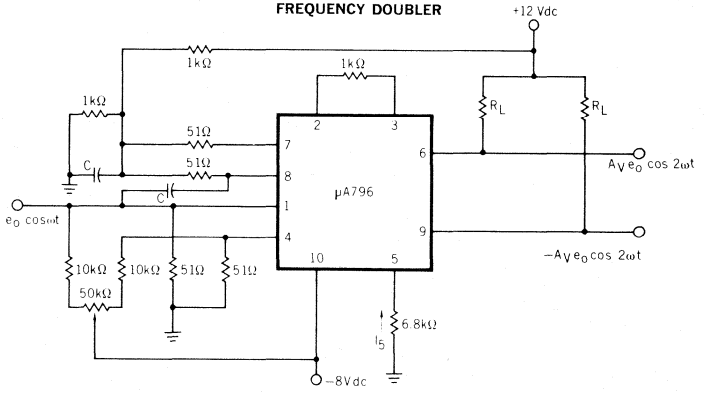
PRODUCT DETECTOR



This figure shows the μA796 used as a single sideband (SSB) suppressed carrier demodulator (product detector). The carrier signal is applied to the carrier input port with sufficient amplitude for switching operation. A carrier input level of 300 mV(rms) is optimum. The composite SSB signal is applied to the signal input port with an amplitude of 5.0 to 500 mV(rms). All output signal components except the desired demodulated audio are filtered out, so that an offset adjustment is not required. This circuit may also be used as an AM detector by applying composite and carrier signals in the same manner as described for product detector operation.

Fig. 2

FREQUENCY DOUBLER



The frequency doubler circuit shown will double low-level signals with low distortion. The value of C should be chosen for low reactance at the operating frequency.

Signal level at the carrier input must be less than 25 mV peak to maintain operation in the linear region of the switching differential amplifier. Levels to 50 mV peak may be used with some distortion of the output waveform. If a larger input signal is available a resistive divider may be used at the carrier input, with full signal applied to the signal input.

Fig. 3

μA796 APPLICATIONS INFORMATION

APP BRIEF 163 — Applications of the μA796 Modulator/Demodulator in Communication Circuits

For information on other Fairchild Communications Integrated Circuits, see the following data sheets:

RF/IF Limiting Amp — μA703
Fixed Gain, Low Distortion Amp — μA716C
High Frequency Communications System — μA719
FM Stereo Multiplex Decoder — μA729
FM Stereo Multiplex Decoder — μA732
Dual Low Noise, High Gain Op-Amp — μA739C
Dual AC Amp — μA745
Color TV Chroma Demodulator — μA746
Dual AC Amp — μA749D
Gain Controlled IF Amp — μA757
TV/FM Sound System — μA754

μA796C
DOUBLE-BALANCED MODULATOR/DEMODULATOR
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA796C is a monolithic Double-Balanced Modulator/Demodulator constructed on a single silicon chip using the Fairchild Planar* epitaxial process. This circuit produces an output voltage which is the product of an input voltage (signal) and a switching function (carrier). Communications applications include modulation and demodulation of AM, SSB, DSB, FSK, FM and phase encoded signals. Signal conditioning techniques possible include frequency doubling and halving, linear mixing and chopping, with additional uses as phase detectors in phase locked loops and as differentiators in NRZ and phase encoded digital tape and disk memories.

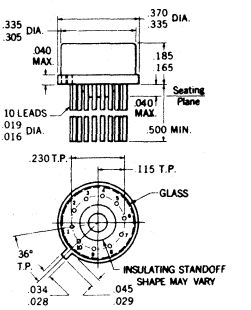
For μA796C applications information and other Fairchild Communications Integrated Circuits, see listing on last page. For full temperature range operation −55°C to +125°C, see μA796 data sheet.

- **EXCELLENT CARRIER 'PRESSION**
- **LOW OFFSETS AND Dkur'**
- **FULLY BALANCED INPUTS AND OUTPUT**
- **USEFUL TO 100 MHz**
- **WIDE RANGE OF APPLICATION**

ABSOLUTE MAXIMUM RATINGS

Internal Power Dissipation (Note 1)	500 mW
Applied Voltage (Note 2)	30 V
Differential Input Signal ($V_7 - V_8$)	±5.0 V
Differential Input Signal ($V_4 - V_1$)	±(5+I_5R_e) V
Input Signal ($V_2 - V_1$, $V_3 - V_4$)	5.0 V
Bias Current (I_5)	12 mA
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	300°C

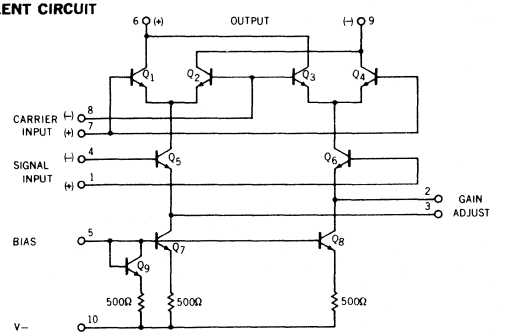
PHYSICAL DIMENSIONS
In accordance with JEDEC (TO-100) outline



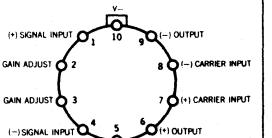
NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.32 grams

ORDER PART NO. U5E7796393

EQUIVALENT CIRCUIT



CONNECTION DIAGRAM
(TOP VIEW)



Pin 10 electrically connected to case through substrate.

NOTES:
(1) Rating applies to Case Temperatures to +70°C.
(2) Voltage applied between pins 6-7, 8-1, 9-7, 9-8, 7-4, 7-1, 8-4, 6-8, 2-5, 3-5.

*Planar is a patented Fairchild process.

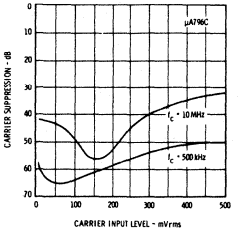
FAIRCHILD SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, Figure 1 unless otherwise specified)

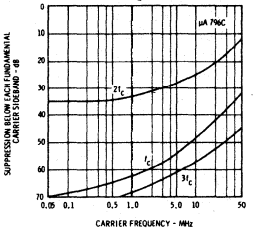
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Carrier Feedthru	V_C = 60 mV (rms) sine wave f_C = 1.0 kHz, offset adjusted		40		μV (rms)
	V_C = 60 mV (rms) sine wave f_C = 10 MHz, offset adjusted		140		μV (rms)
	V_C = 300 mV_{PP} square wave f_C = 1.0 kHz, offset adjusted		0.04	0.2	mV (rms)
	V_C = 300 mV_{PP} square wave f_C = 1.0 kHz, offset not adjusted		20	150	mV (rms)
Carrier Suppression	f_S = 10 kHz, 300 mV (rms) f_C = 500 kHz, 60 mV (rms) sine wave offset adjusted	50	65		dB
	f_S = 10 kHz, 300 mV (rms) f_C = 10 MHz, 60 mV (rms) sine wave offset adjusted		50		dB
Transadmittance Bandwidth	R_L = 50 Ω Carrier Input Port, V_C = 60 mV (rms) sine wave f_S = 1.0 kHz, 300 mV (rms) sine wave		300		MHz
	Signal Input Port, V_S = 300 mV (rms) sine wave $V_7 - V_8$ = 0.5 V dc		80		MHz
Voltage Gain, Signal Channel	V_S = 100 mV (rms), f = 1.0 kHz $V_7 - V_8$ = 0.5 V dc	2.5	3.5		V/V
Input Resistance, Signal Port	f = 5.0 MHz $V_7 - V_8$ = 0.5 V dc		200		kΩ
Input Capacitance, Signal Port	f = 5.0 MHz $V_7 - V_8$ = 0.5 V dc		2.0		pF
Single Ended Output Resistance	f = 10 MHz		40		kΩ
Single Ended Output Capacitance	f = 10 MHz		5.0		pF
Input Bias Current	$(I_1 + I_4)/2$		12	30	μA
Input Bias Current	$(I_7 + I_8)/2$		12	30	μA
Input Offset Current	$(I_1 - I_4)$		0.7	5.0	μA
Input Offset Current	$(I_7 - I_8)$		0.7	5.0	μA
Average Temperature Coefficient of Input Offset Current	$0°C \leq T_A \leq +70°C$		2.0		nA/°C
Output Offset Current	$(I_6 - I_9)$		14	60	μA
Average Temperature Coefficient of Output Offset Current	$0°C < T_A < +70°C$		90		nA/°C
Signal Port Common Mode Input Voltage Range	f_S = 1.0 kHz		5.0		V_{p-p}
Signal Port Common Mode Rejection Ratio	$V_7 - V_8$ = 0.5 V dc		−85		dB
Common Mode Quiescent Output Voltage			8.0		Vdc
Differential Output Swing Capability			8.0		V_{p-p}
Positive Supply Current	$(I_6 + I_9)$		2.0	3.0	mA
Negative Supply Current	(I_{10})		3.0	4.0	mA
Power Dissipation			33		mW

TYPICAL PERFORMANCE CURVES

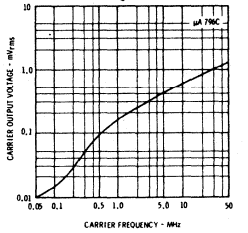
CARRIER SUPPRESSION VERSUS CARRIER INPUT LEVEL



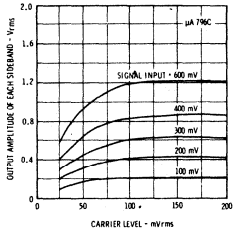
CARRIER SUPPRESSION VERSUS FREQUENCY



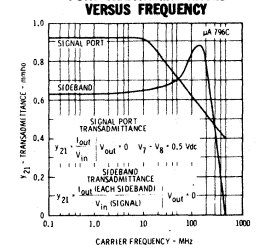
CARRIER FEEDTHROUGH VERSUS FREQUENCY



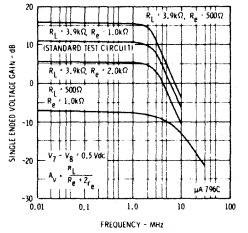
SIDEBAND OUTPUT VERSUS CARRIER LEVELS



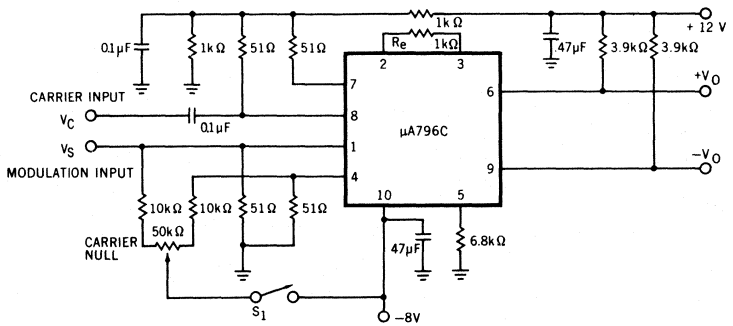
SIDEBAND AND SIGNAL PORT TRANSADMITTANCES VERSUS FREQUENCY



SIGNAL-PORT FREQUENCY RESPONSE



TYPICAL MODULATOR CIRCUIT

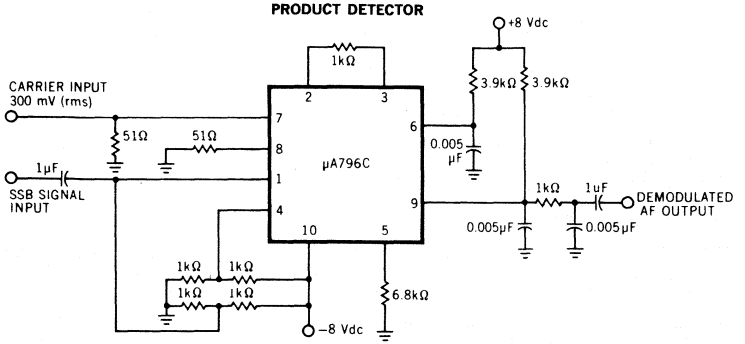


Note: S_1 is closed for "adjusted" measurements.

Fig. 1

TYPICAL APPLICATIONS

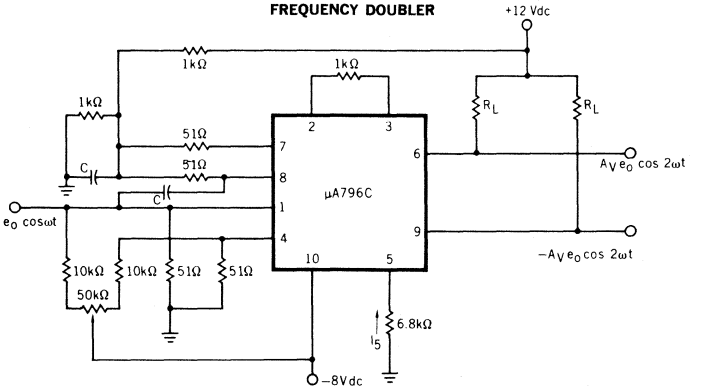
PRODUCT DETECTOR



This figure shows the μA796C used as a single sideband (SSB) suppressed carrier demodulator (product detector). The carrier signal is applied to the carrier input port with sufficient amplitude for switching operation. A carrier input level of 300 mV(rms) is optimum. The composite SSB signal is applied to the signal input port with an amplitude of 5.0 to 500 mV(rms). All output signal components except the desired demodulated audio are filtered out, so that an offset adjustment is not required. This circuit may also be used as an AM detector by applying composite and carrier signals in the same manner as described for product detector operation.

Fig. 2

FREQUENCY DOUBLER



The frequency doubler circuit shown will double low-level signals with low distortion. The value of C should be chosen for low reactance at the operating frequency.

Signal level at the carrier input must be less than 25 mV peak to maintain operation in the linear region of the switching differential amplifier. Levels to 50 mV peak may be used with some distortion of the output waveform. If a larger input signal is available a resistive divider may be used at the carrier input, with full signal applied to the signal input.

Fig. 3

μA796C APPLICATIONS INFORMATION

APP BRIEF 163 — Applications of the μA796 Modulator/Demodulator in Communication Circuits

For information on other Fairchild Communications Integrated Circuits, see the following data sheets:

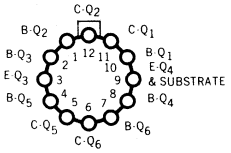
RF/IF Limiting Amp — μA703C μA703D
Fixed Gain, Low Distortion Amp — μA716C
High Frequency Communications System — μA719C
FM Stereo Multiplex Decoder — μA729
FM Stereo Multiplex Decoder — μA732
Dual Low Noise, High Gain Op-Amp — μA739C
Dual AC Amp — μA745
Color TV Chroma Demodulator — μA746
Dual AC Amp — μA749D
Gain Controlled IF Amp — μA757C
TV/FM Sound System — μA754C

μA3026 . μA3054
TRANSISTOR ARRAYS
FAIRCHILD LINEAR INTEGRATED CIRCUITS

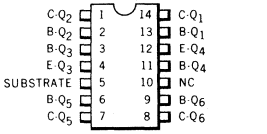
- **DUAL MATCHED DIFFERENTIAL PAIRS WITH CURRENT SOURCE**
- **V_{BE} MATCHED TO 5 mV MAX .**
- **FULL TEMPERATURE RANGE OPERATION**
- **WIDEBAND OPERATION – f_T 550 MHz TYP.**
- **DIRECT REPLACEMENT FOR μA3026/μA3054**

CONNECTION DIAGRAMS
(TOP VIEWS)

μA3026



μA3054



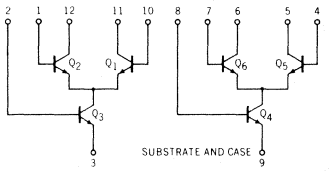
ABSOLUTE MAXIMUM RATINGS

Power Dissipation - Single transistor	300 mW
Power Dissipation - Total - μA3026 (Note 1)	600 mW
Power Dissipation - Total - μA3054 (Note 2)	750 mW
Supply Voltage, (Note 3)	20 V
Collector Current	50 mA
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +200°C
Lead Temperature (Soldering, 60 seconds)	+300°C

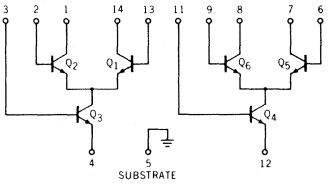
GENERAL DESCRIPTION – The μA3026 and μA3054 consist of dual differentially connected pairs with current source transistors constructed on a single silicon substrate using the Fairchild Planar* epitaxial process. The close electrical and thermal matching of the devices makes them suitable for a wide variety of communication and instrumentation applications from DC to 120 MHz. For other Fairchild Transistor Arrays, see the μA3045 data sheet.

SCHEMATIC DIAGRAMS

μA3026



μA3054



*Planar is a patented Fairchild process.

NOTES:

(1) Rating applies to an ambient temperature of +55°C. For operation above 55°C, derate linearly at 5 mW/°C.

(2) Rating applies to an ambient temperature of +55°C. For operation above 55°C, derate linearly at 6.67 mW/°C.

(3) Substrate must be connected to the most negative point in the external circuit to maintain normal operation. See electrical characteristics for individual junction breakdown voltages.

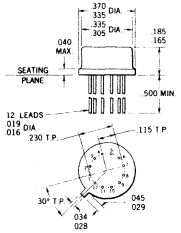
FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS @ $T_A = 25°C$

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
(Each Differential Amplifier)	$V_{CB} = 3$ V, $I_{EQ3} = I_{EQ4} = 2$ mA				
Offset Voltage			0.45	5.0	mV
Offset Current			0.3	2.0	μA
Input Bias Current			10	24	μA
(Each Transistor)					
V_{BE}	$V_{CB} = 3$ V, $I_C = 50$ μA		0.630	0.7	V
	$V_{CB} = 3$ V, $I_C = 1$ mA		0.715	0.8	V
	$V_{CB} = 3$ V, $I_C = 3$ mA		0.750	0.85	V
	$V_{CB} = 3$ V, $I_C = 10$ mA		0.800	0.9	V
I_{CBO}	$V_{CB} = 10$ V, $I_E = 0$		0.002	100	nA
V_{CEO}	$I_C = 1$ mA, $I_B = 0$	15	24		V
V_{CBO}	$I_C = 10$ μA, $I_E = 0$	20	60		V
V_{CIO} (collector-to-substrate)	$I_C = 10$ μA, $I_{CI} = 0$	20	60		V
V_{EBO}	$I_E = 10$ μA, $I_C = 0$	5.0	7.0		V

PACKAGE INFORMATION

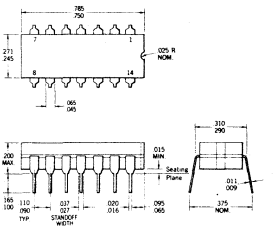
METAL CAN
U5G PACKAGE
Similar to JEDEC (TO–101) outline



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Pin 9 is connected to case through the substrate
Package weight is 1.08 gram

ORDER PART No.
DEVICE: μA3026
PRODUCT CODE: U5G7026312

CERAMIC DIP
U6A PACKAGE
In accordance with JEDEC (TO–116) outline



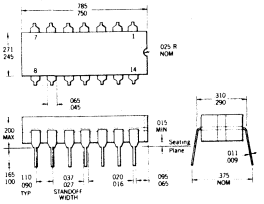
NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers.
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams

ORDER PART No.
DEVICE: μA3054
PRODUCT CODE: U6A7054312

μA3045
TRANSISTOR ARRAY
FAIRCHILD LINEAR INTEGRATED CIRCUITS

- MATCHED DIFFERENTIAL PAIR PLUS 3 NPN TRANSISTORS
- V_{BE} MATCHED TO 5 mV MAX
- LOW NOISE FIGURE –3.2 dB TYP @ 1 kHz
- INPUT OFFSET CURRENT –2 μA MAX AT I_C = 1 mA
- WIDEBAND OPERATION – f_T –300 MHz MIN
- DIRECT REPLACEMENT FOR CA3045/CA3046

PHYSICAL DIMENSIONS
CERAMIC DIP
6A PACKAGE
in accordance with
JEDEC (TO-116) outline



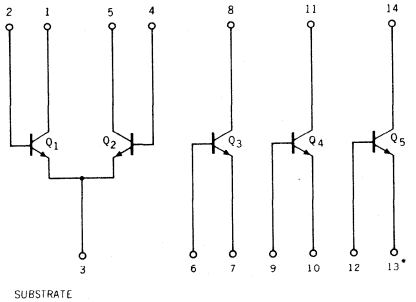
NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams

GENERAL DESCRIPTION – The μA3045 consists of 5 general purpose silicon NPN transistors constructed on a single silicon substrate using the Fairchild Planar* epitaxial process. Two of the transistors are internally connected to form a differential pair. The close electrical and thermal matching of these transistors makes this IC suitable for a wide variety of applications from DC to 120 MHz. For other Fairchild Transistor Arrays, see the following data sheets: μA3026 and μA3054.

ABSOLUTE MAXIMUM RATINGS

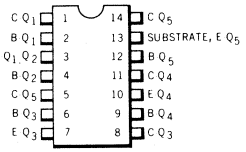
Power Dissipation (each transistor)	300 mW
Power Dissipation - total (Note 1)	750 mW
Collector Current	50 mA
Supply Voltage (Note 2)	20 V
Operating Temperature Range	–55°C to +125°C
Storage Temperature Range	–65°C to +200°C
Lead Temperature (Soldering, 60 seconds)	+300°C

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM

(TOP VIEW)



ORDER INFORMATION
DEVICE TYPE: μA3045
PRODUCT CODE: U6A7045312

Notes on back page.

*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS @ $T_A = 25^\circ C$

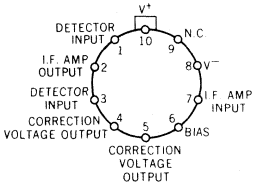
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CBO}	$I_C = 10\ \mu A$, $I_E = 0$	20	60		V
V_{CEO}	$I_C = 1$ mA, $I_B = 0$	15	24		V
V_{CIO} (collector-to-substrate)	$I_C = 10\ \mu A$, $I_{CI} = 0$	20	60		V
V_{EBO}	$I_E = 10\ \mu A$, $I_C = 0$	5.0	7.0		V
I_{CBO}	$V_{CB} = 10$ V, $I_E = 0$	0.002	40		nA
I_{CEO}	$V_{CE} = 10$ V, $I_B = 0$			0.5	μA
h_{FE}	$V_{CE} = 3$ V, $I_C = 1$ mA	40	100		
Input Offset Current	$V_{CE} = 3$ V, $I_C = 1$ mA		0.3	2.0	μA
V_{BE}	$V_{CE} = 3$ V, $I_E = 1$ mA		0.715		V
V_{OS}	$V_{CE} = 3$ V, $I_C = 1$ mA		0.45	5.0	mV
f_T	$V_{CE} = 3$V, $I_C = 3$ mA	300	550		kHz
V_{CES}	$I_B = 1$ mA, $I_C = 10$ mA		0.23		V

NOTES:
1. Rating applies to ambient temperature of +75°C. For operation above +75°C, derate linearly at 8.0 mW/°C.
2. Substrate must be connected to the most negative point in external circuit to maintain normal operation.

μA3064
TV AUTOMATIC FINE-TUNING CIRCUIT
FAIRCHILD LINEAR INTEGRATED CIRCUITS

- **HIGH SENSITIVITY**
- **25kHz MAX. FREQUENCY DEVIATION**
- **INTERNAL VOLTAGE REGULATOR**
- **INTERNAL AGC**

CONNECTION DIAGRAM
(TOP VIEW)



GENERAL DESCRIPTION – The μA3064 is a TV automatic fine-tuning linear integrated circuit constructed on a single silicon chip using the Fairchild Planar* epitaxial process. The μA3064 combines all of the automatic fine-tuning circuitry, except transformers, in one integrated circuit. Systems with low level I.F. amplifiers can now achieve tuning accuracies of ±25 kHz due to the μA3064's high sensitivity. Internal voltage regulation improves overall performance and reduces system cost. (For information on other Fairchild Linear communication integrated circuits, see last page).

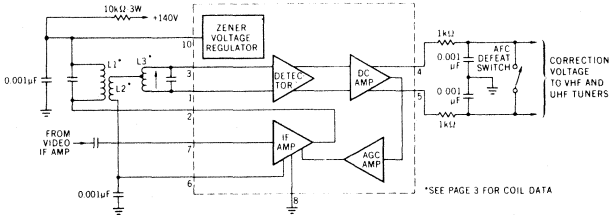
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage	Note 2
Internal Power Dissipation (Note 3)	700 mW
Detector Differential Voltage ($V_{1\text{-}3}$)	± 10 V
Detector Input Voltage Range (V_1, V_3)	+ 5 V, -6 V
I.F. Amp Output (V_2)	+ 20 V, 0 V
Bias Voltage (V_6)	+ 2 V, 0 V
Storage Temperature Range	-65°C to + 150°C
Operating Temperature range	-40°C to + 85°C
Lead Temperature (soldering, 60 seconds)	300°C

ORDER PART NO:

DEVICE TYPE	PRODUCT CODE
μA3064	U5A7064354 (Formed Leads)
μA3064T	U5E7064354 (Straight Leads)

BLOCK DIAGRAM



NOTES:
(1) All voltages referenced to V^- except as noted.
(2) V^+ terminal may be connected to any positive voltage source through a suitable dropping resistor, provided the dissipation rating is not exceeded.
(3) Derate linearly at 5.6 mW/°C for ambient temperatures above + 25°C.

*Planar is a patented Fairchild process.

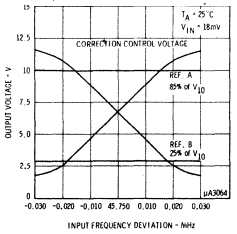
FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS (V_{CC} = + 30 V, R_S = 1.5 kΩ, T_A = 25°C unless otherwise specified)

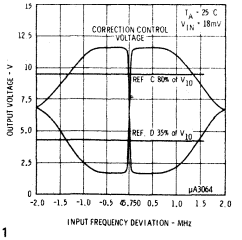
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Power Consumption	T_A = + 25°C	130	140	150	mW
	T_A = -25°C		135	150	mW
	T_A = + 85°C		145	150	mW
Supply Current – I^+	V^+ = + 10.5 V	4.0	6.5	9.5	mA
Regulated Supply Voltage – V^+		10.9	11.8	12.8	V
Quiescent Operating Current – I_2		1.0	2.0	4.0	mA
Quiescent Operating Voltages – V_4, V_5		5.0	6.9	8.0	V
Output Offset Voltage – (V_4 – V_5)		-1.0	0	1.0	V
Input Admittance – Y_{11}	f = 45.75 MHz		0.41 + j 1.0		mmho
Reverse Transfer Admittance – Y_{12}	f = 45.75 MHz		0 + j 3.4		μmho
Forward Transfer Admittance – Y_{21}	f = 45.75 MHz		24.5 -j 29		mmho
Output Admittance – Y_{22}	f = 45.75 MHz		0.04 + j 0.9		mmho
Correction Control Voltage – V_4 (Test Circuit 1)	V_{IN} = 18 mV RMS				
	f_o = 45.750 MHz				
	Δf as listed (MHz)				
	-0.030	85			% V^+
	+ 0.030			25	% V^+
	-0.900	80			% V^+
	+ 0.900			35	% V^+
	-1.500			80	% V^+
	+ 1.500	35			% V^+
Correction Control Voltage – V_5 (Test Circuit 1)	V_{IN} = 18 mV RMS				
	f_o = 45.750 MHz				
	Δf as listed (MHz)				
	-0.030			25	% V^+
	+ 0.030	85			% V^+
	-0.900			35	% V^+
	+ 0.900	80			% V^+
	-1.500	35			% V^+
	+ 1.500			80	% V^+

TYPICAL PERFORMANCE CURVES

NARROW-BAND DYNAMIC CONTROL VOLTAGE CHARACTERISTICS

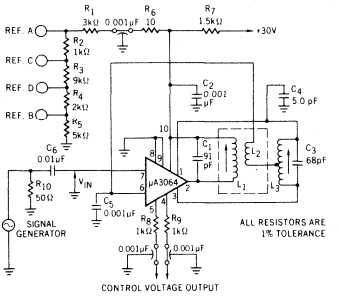


WIDE-BAND DYNAMIC CONTROL VOLTAGE CHARACTERISTICS



SEE TEST CIRCUIT 1

TEST CIRCUIT 1
CORRECTION VOLTAGES



NOTE: Parts placement is critical. Use P.C. board layout on last page for best results.

L_1 is aligned for symmetrical bandwidth on either side of 45.750 MHz.

L_2 tertiary winding wound on L_1 coil form

L_3 is aligned for zero differential output between terminals 4 and 5 at f_o = 45.750 MHz

REFERENCE VOLTAGE PERCENTAGES

Ref. A	85% of V_{10}
Ref. B	25% of V_{10}
Ref. C	80% of V_{10}
Ref. D	35% of V_{10}

COIL DATA FOR DISCRIMINATOR WINDINGS

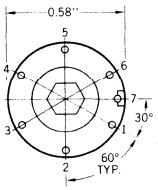
L_1 – Discriminator Primary: 3 1/6 turns; #20 Enamel-covered wire–close-wound, at bottom of coil form. Inductance of L_1 = 0.165 μH; Q_o = 120 at f_o = 45.75 MHz.
Start winding at Terminal #6; finish at Terminal #1. See Notes below.

L_2 – Tertiary Windings: 2 1/6 turns; #20 Enamel-covered wire–close wound over bottom end of L_1. Start winding at Terminal #3; finish at Terminal #4. See Notes below.

L_3 – Discriminator Secondary: 3 1/2 turns; center tapped, space wound at bottom of coil form. Inductance of L_3 = 0.180 μH; Q_o = 150 at f_o = 45.75 MHz.
Start winding at Terminal #2; finish at Terminal #5, connect center tap to Termmal #7. See Notes below.

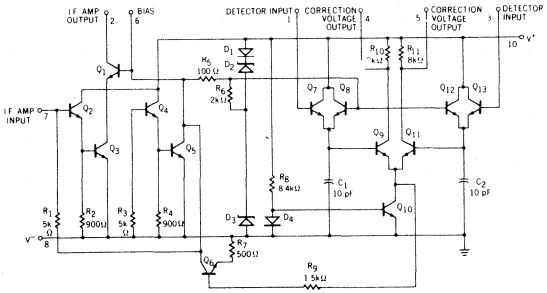
Notes:
1. Coil Forms; Cylindrical; 0.30" Dia. max.
2. Tuning Core: 0.250" Dia. x 0.37" Length.
   : Material: Carbinal J or equivalent.
3. Coil Form Base: See drawing below.
4. End of coil nearest terminal board to be designated the winding start end.

COIL FORM BASE TERMINAL DIAGRAM

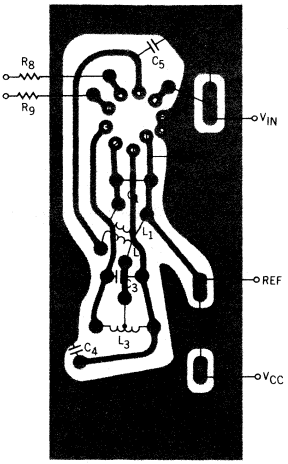


Coil	RCA Distributor Part No.
(L_1, L_2)	122 213
L_3	122 203

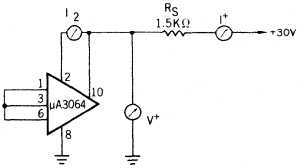
μA3064 EQUIVALENT CIRCUIT



PRINTED CIRCUIT BOARD FOR CORRECTION VOLTAGE TEST CIRCUIT
Full Size Bottom View

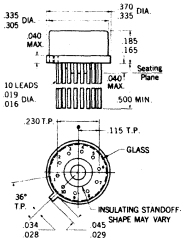


TEST CIRCUIT 2
Regulated Voltage, Total Supply Current and Quiescent Current at Terminal 2



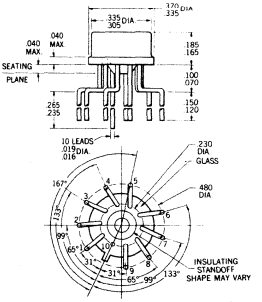
PHYSICAL DIMENSIONS

5E PACKAGE
In accordance with
JEDEC (TO-100) outline



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.32 grams

5A PACKAGE
Lead Formed 10 PIN Metal Can



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.32 grams
This is a "5E" package with leads formed in assembly

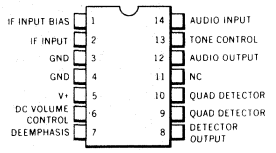
FOR INFORMATION ON OTHER FAIRCHILD COMMUNICATION INTEGRATED CIRCUITS, SEE THE FOLLOWING DATA SHEETS:

RF/IF LIMITING AMP – μA703, μA703C, μA703D
AUDIO AMP – μA716C
TV/FM SOUND IF – μA719, μA719C, μA754, μA754C, μA784, μA3065
VIDEO AMPLIFIERS – μA733, μA733C, μA751C
STEREO MULTIPLEX DECODER – μA729, μA732, μA767
STEREO AUDIO PREAMP – μA739C, μA749, μA749C, μA749D
DUAL AC AMPLIFIER/OSCILLATOR – μA745
COLOR TV CHROMA PROCESSING – μA746, μA780, μA781, μA786
AGC IF AMPLIFIER – μA757, μA757C, μA781
TV SIGNAL PROCESSING – μA785
BALANCED MODULATOR-DEMODULATOR – μA796, μA796C
PHASE LOCKED LOOP – μA780
TRANSISTOR AND DIODE ARRAYS – μA3018, μA3018A, μA3019, μA3026, μA3036, μA3045, μA3054
VOLTAGE REGULATOR – μA723, μA723C, μA109, μA209, μA309

μA3065
TV/FM SOUND SYSTEM
FAIRCHILD LINEAR INTEGRATED CIRCUITS

- **DC VOLUME CONTROL ELIMINATES NEED FOR SHIELDED CABLES**
- **EXCELLENT AM REJECTION -50dB TYPICAL AT 4.5 MHz**
- **DIFFERENTIAL PEAK DETECTOR REQUIRES ONLY ONE SINGLE-TUNED COIL**
- **INTERNAL ZENER DIODE REGULATED SUPPLY**
- **LOW HARMONIC DISTORTION**

CONNECTION DIAGRAM
(TOP VIEW)



GENERAL DESCRIPTION – The μA3065 Monolithic TV/FM Sound System consists of a Multi-stage Limiting IF Amplifier, DC Gain (Volume) control, FM Detector, and an Audio Driver constructed on a single silicon chip using the Fairchild planar* epitaxial process. Excellent sensitivity, high AM rejection and an internally regulated power supply coupled with low external component requirement makes the μA3065 suitable for a wide variety of applications including TV Sound Channels, Line Operated and Automobile FM Radios and Mobile Communications Equipment. (For other Fairchild Communications Integrated Circuits, see listing on last page.)

ABSOLUTE MAXIMUM RATINGS

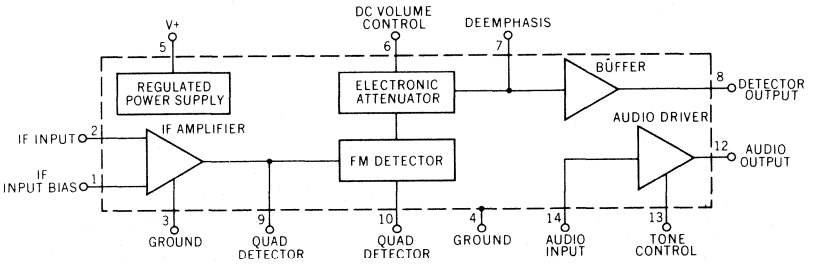
Supply Voltage	Note 1
Internal Power Dissipation (Note 2)	850 mW
Power Supply Current	50 mA
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	
Ceramic DIP	-65°C to + 150° C
Silicone DIP	-55°C to + 125° C
Lead Temperature Range	
Ceramic DIP (Soldering, 60 seconds)	300°C
Silicone DIP (Soldering, 10 seconds)	260°C

ORDERING INFORMATION

DEVICE TYPE	PRODUCT CODE
Silicone Quad-in-line	
μA3065	**U9C7065354**
Silicone Dual-in-line	
μA3065A	**U9A7065354**
Ceramic Quad-in-line	
μA3065B	**U7F7065354***
Ceramic Dual-in-line	
μA3065C	**U6A7065354**

***Available on special order.**
See Package Dimension on last page.

BLOCK DIAGRAM



*Planar is a patented Fairchild process

NOTES:
(1) V+ terminal may be connected to any positive voltage through a suitable dropping resistor, provided the dissipation rating is not exceeded.
(2) Rating applies to ambient temperature of 25°C. For ambient temperatures above 25°C, derate linearly at 6.67mW/°C.

FAIRCHILD SEMICONDUCTOR

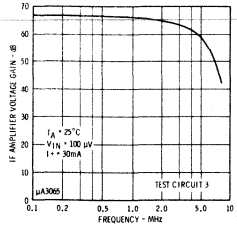
ELECTRICAL CHARACTERISTICS (T_A = 25°C, I^+ = 30 mA unless otherwise specified)

PARAMETER	CONDITIONS	TEST CIRCUIT	MIN	TYP	MAX	UNITS
STATIC CHARACTERISTICS						
Zener Regulating Voltage (V_5)			10.3	11.2	12.2	Volts
Supply Current (I_5)	V_{Supply} = 9.0V		10	16	24	mA
Internal Power Dissipation	I^+ = 33mA		343	370	400	mW
Voltage at IF Input Bias (V_1)				2.0		Volts
Voltage at DC Volume Control (V_6)				4.8		Volts
Voltage at De Emphasis (V_7)				6.1		Volts
Voltage at Quad Detector (V_9)				3.7		Volts
Voltage at Audio Output (V_{12})			4.0	5.1	5.8	Volts
DYNAMIC CHARACTERISTICS						
IF AMPLIFIER	(f_o = 4.5 MHz, FM±25KHz at 400 Hz, V_{IN} = 100μV)	1				
Input Limiting Voltage at -3dB point				200	400	μV
AM Rejection	AM = 30% at 4.5 MHz	1	40	50		dB
IF Transconductance	f = 4.5 MHz					
Magnitude				500		mmho
Phase Angle				46		degrees
Feedback Capacitance	f = 1.0 MHz, Pin 2 to Pin 9			<0.02		pF
Input Impedance Components	f = 4.5 MHz, Pin 1 to Pin 2					
Parallel Input Resistance				17		kΩ
Parallel Input Capacitance				4		pF
Output Impedance Components	f = 4.5 MHz, Pin 9 to Ground					
Parallel Output Resistance				3.25		kΩ
Parallel Output Capacitance				75		pF
DETECTOR	(f_o = 4.5 MHz, FM= ±25kHz at 400 Hz, V_{IN} = 100 mV)					
Recovered AF Voltage		1	0.5	0.75		Vrms
Total Harmonic Distortion		1		0.9	2.0	%
Output Resistance						
De emphasis Output				7.5		kΩ
Detector Output				300		Ω
ATTENUATOR						
Max. Attenuation	R_x = ∞	1	60	80		dB
Max. Play-through Voltage*	R_x = ∞	1		0.075	1.0	mV
AUDIO AMPLIFIER						
Voltage Gain	V_1 = 0.1 Vrms, f = 400 Hz	2	17.5	20		dB
Total Harmonic Distortion	V_0 = 2 Vrms, f = 400 Hz	2		1.5		%
Undistorted Output Voltage	THD = 5%, f = 400 Hz	2	2.0	2.5		Vrms
Input Resistance	f = 400 Hz			70		kΩ
Output Resistance	f = 400 Hz			270		Ω

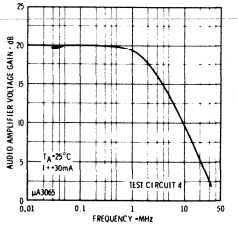
*Play-through voltage is the unwanted signal, measured at the detector output, when the volume control is set for minimum output.

TYPICAL PERFORMANCE CURVES

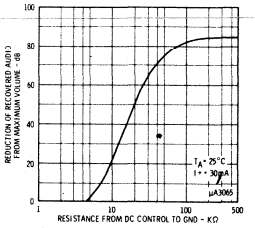
FREQUENCY RESPONSE OF IF AMPLIFIER SECTION



FREQUENCY RESPONSE OF AUDIO AMPLIFIER SECTION



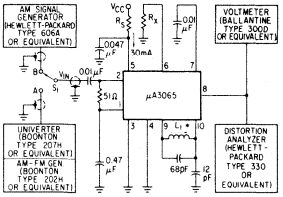
AUDIO GAIN REDUCTION VERSUS DC VOLUME CONTROL RESISTANCE



TEST CIRCUITS

TEST CIRCUIT 1

INPUT LIMITING VOLTAGE, AM REJECTION, RECOVERED AUDIO, TOTAL HARMONIC DISTORTION, MAXIMUM ATTENUATION, MAXIMUM "PLAY-THROUGH" TEST CIRCUIT.



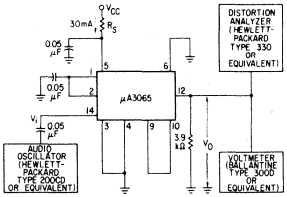
PINS 11, 12, 13, 14 NO CONNECTION

*L_1 = 16μH NOMINAL

$Q_{(UNLOADED)}$ = 50

TEST CIRCUIT 2

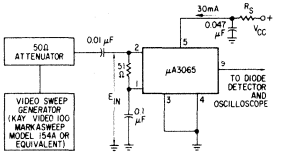
AUDIO VOLTAGE GAIN (UNDISTORTED OUTPUT)



PINS 7, 8, 11, 13 NO CONNECTION

TEST CIRCUIT 3

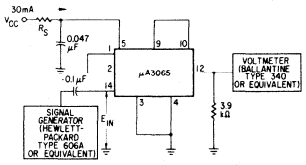
IF AMPLIFIER SECTION



E_{IN} = 100μVrms

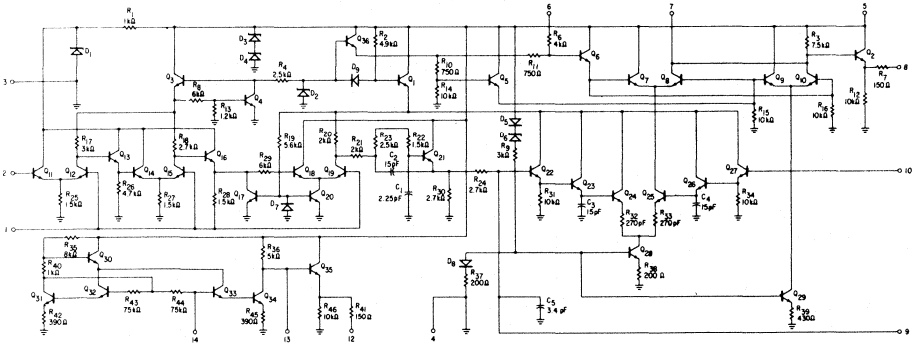
TEST CIRCUIT 4

AUDIO AMPLIFIER SECTION



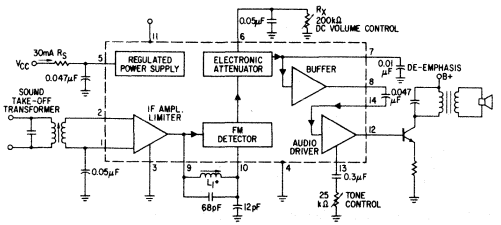
E_{IN} = 100 mV

EQUIVALENT CIRCUIT



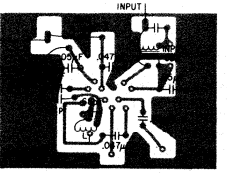
TYPICAL APPLICATION

TV SOUND SYSTEM



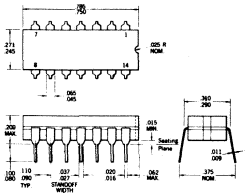
*L_I = 16μH NOMINAL , $Q_{(UNLOADED)}$ = 50

SUGGESTED CIRCUIT LAYOUT
COMPONENT SIDE



PACKAGE INFORMATION

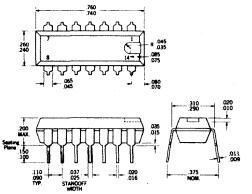
CERAMIC DIP
U6A PACKAGE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams

ORDER PART NO. U6A7065354
DEVICE TYPE μA3065C

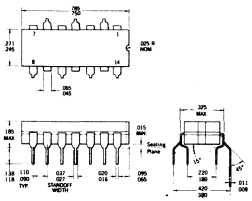
SILICONE DIP
U9A PACKAGE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimension should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 0.9 gram

ORDER PART NO. U9A7065354
DEVICE TYPE μA3065A

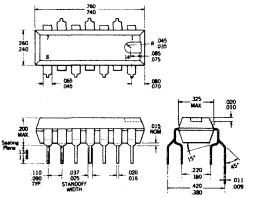
CERAMIC QUIL
U7F PACKAGE



NOTES:
All dimensions in inches
This is a "6A" package with leads formed in assembly
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams

ORDER PART NO. U7F7065354*
DEVICE TYPE μA3065B

SILICONE QUIL
U9C PACKAGE



NOTES:
All dimensions in inches
This is a "9A" package with leads formed in assembly
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are gold-plated kovar
Package weight is 0.9 gram

ORDER PART NO. U9C7065354
DEVICE TYPE μA3065

*AVAILABLE ON SPECIAL ORDER

FOR INFORMATION ON OTHER FAIRCHILD COMMUNICATIONS CIRCUITS SEE THE FOLLOWING DATA SHEETS:

RF/IF LIMITING AMP – μA703, μA703C, μA703D
AUDIO AMP – μA716C
TV/FM SOUND IF – μA719, μA719C, μA754, μA754C, μA784, μA3065
VIDEO AMPLIFIER – μA733, μA733C, μA751C
STEREO MULTIPLEX DECODER – μA729, μA732, μA767
STEREO AUDIO PREAMP – μA739C, μA749, μA749C, μA749D
DUAL AC AMPLIFIER–OSCILLATOR – μA745
COLOR TV CHROMA PROCESSING – μA746, μA780, μA786
AGC IF AMPLIFIER – μA757, μA757C
TV SIGNAL PROCESSING – μA785
AUTOMATIC FINE TUNING CIRCUIT – μA3064
BALANCED MODULATOR-DEMODULATOR – μA796, μA796C
GAIN CONTROLLED IF AMPLIFIER – μA781
TRANSISTOR AND DIODE ARRAYS – μA3018, μA3018A, μA3019, μA3026, μA3036, μA3045, μA3046, μA3054
VOLTAGE REGULATOR – μA723, μA723C

μA7524

TWO CHANNEL CORE MEMORY SENSE AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

- **±2 mV THRESHOLD VARIATION**
- **25 ns PROPAGATION DELAY**
- **DUAL INDEPENDENT STROBES**
- **TTμL COMPATIBLE**

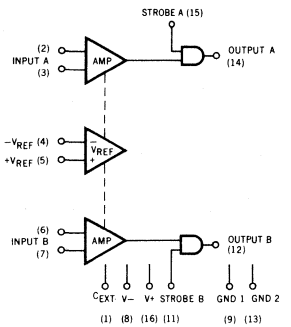
GENERAL DESCRIPTION — The μA7524 is a two channel core memory sense amplifier constructed on a silicon chip using the patented Fairchild Planar* epitaxial process. It can be used for small (1K to 8K words) memories as well as larger memory systems. The device is suitable for small core sizes facilitating very fast memory cycle times. The μA7524 features tight threshold accuracy, fast response time, and independent strobe selection. Unit to unit variations are minimized so that individual adjustments of the threshold and strobe timing are not necessary.

All logic inputs and outputs are fully TTμL compatible. The μA7524 is intended to be a pin for pin replacement for the 7524. The μA7524 can be combined with the Fairchild MSI Quad Latch 9314 to provide complete memory data register capability. For improved performance, see the μA761C or μA761D data sheets.

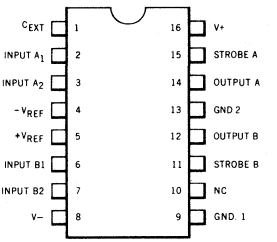
ABSOLUTE MAXIMUM RATINGS

Differential Input Voltage	±5.0 V
Supply Voltage	±7.0 V
Logic Input Voltage	+5.5 V
Power Dissipation (Note 1) 6M Package	400 mW
7B Package	500 mW
Storage Temperature 6M Package	−65°C to +150°C
7B Package	−55°C to +125°C
Operating Temperature	0°C to +70°C
Lead Temperature (6M Package, Soldering 10 seconds)	+260°C
(7B Package, Soldering 60 seconds)	+300°C
Signal Input	±3.0 V
Reference Input	±3.0 V

BLOCK DIAGRAM

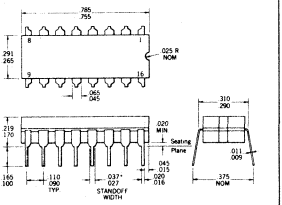


CONNECTION DIAGRAM



PHYSICAL DIMENSIONS

16 Lead Ceramic Dual In-Line



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020" diameter lead
Leads are tin-plated kovar
Package weight is 2.2 grams
*The .027/.037 dimension does not apply to the corner leads

ORDER PART NO. U7B7524392

Note 1: Rating applies for Ambient Temperature to 70°C.

*Planar is a patented Fairchild process.

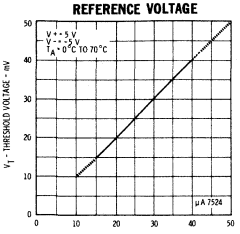
FAIRCHILD SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS ($V^+ = 5.0$ V, $V^- = -5.0$ V, 0°C to +70°C either Amplifier unless otherwise specified)

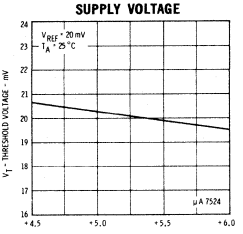
PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Threshold Voltage Range					
Minimum			10		mV
Maximum			50		mV
Threshold Uncertainty			±2.0		mV
Differential Input Threshold Voltage	$V_{ref} = 15$ mV	11		19	mV
	$V_{ref} = 40$ mV	36		44	mV
Differential Input Bias Current	$V_{IND} = 0$ mV		15	75	μA
Differential Input Offset Current	$V_{IND} = 0$ mV		1.0		μA
Differential Input Impedance	f = 1.0 kHz		2.5		kΩ
Positive Supply Current	$T_A = 25°C$		25		mA
Negative Supply Current	$T_A = 25°C$		10		mA
Output Short Circuit Current	$V^+ = 5.25$ V, $V^- = -5.25$ V	2.1		3.5	mA
LOGIC INPUT/OUTPUT CONDITIONS (See Fig. 2)					
Output Voltage Logical "1"	I Load = 400 μA $V_{in(1)}$ STROBE = 2.0 V $V_{in(0)}$ STROBE = 0.8 V $V^+ = 4.75$ V $V^- = -4.75$ V	2.4	3.9		V
Output Voltage Logical "0"	I Sink = 16 mA $V_{in(0)}$ STROBE = 0.8 V $V^+ = 4.75$ V $V^- = -4.75$ V		0.25	0.4	V
Logical "1" Input (Strobe Inputs)	$V_{in(0)}$ STROBE = 0.8 V $V^+ = 4.75$ V $V^- = -4.75$ V	2.0			V
Logical "0" Input (Strobe Inputs)	$V_{in(1)}$ STROBE = 2.0 V $V^+ = 4.75$ V $V^- = -4.75$ V			0.8	V
Logical "0" Input Current (Strobe Inputs)	$V_{in(0)}$ STROBE = 0.4 V $V^+ = 5.25$ V $V^- = -5.25$ V		−1.0	−1.6	mA
Logical "1" Input Current (Strobe Inputs)	$V_{in(1)}$ STROBE = 2.4 V $V^+ = 5.25$ V $V^- = -5.25$ V			40	μA
Logical "1" Input Current (Strobe Inputs)	$V_{in(1)}$ STROBE = V^+ $V^+ = 5.25$ V $V^- = -5.25$ V			1.0	mA
A.C. CHARACTERISTICS	$T_A = 25°C$				
Common Mode Input Firing Voltage	$t_r = t_f \leq 15$ ns $t_p = 50$ ns		±3.0		V
Common Mode Input Overload Recovery Time	$V_{inCM} = \pm 2.0$ V, $t_r = t_f = 20$ ns		20		ns
Input to Output Delay	t_{pd} (1) D		25	40	ns
(See Figure 1)	t_{pd} (0) D		35		ns
Strobe to Output Delay	t_{pd} (1) STROBE		15	30	ns
(See Figure 1)	t_{pd} (0) STROBE		25		ns
Differential Input Overload Recovery Time	$V_{in} + 2.0$ V, $t_r = t_f = 20$ ns		20		ns

TYPICAL PERFORMANCE CURVES

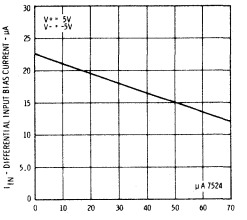
THRESHOLD VOLTAGE VERSUS REFERENCE VOLTAGE



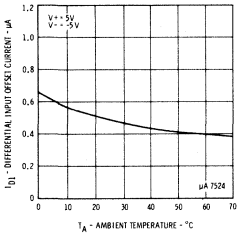
THRESHOLD VOLTAGE VERSUS SUPPLY VOLTAGE



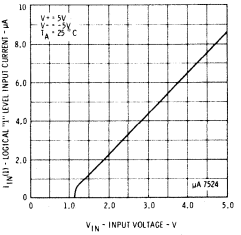
DIFFERENTIAL-INPUT BIAS CURRENT VERSUS AMBIENT TEMPERATURE



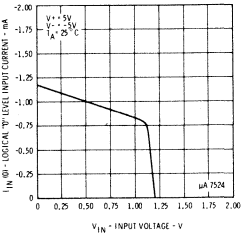
DIFFERENTIAL-INPUT OFFSET CURRENT VERSUS AMBIENT TEMPERATURE



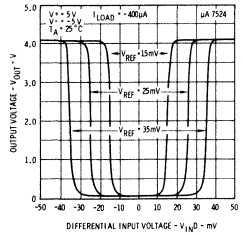
LOGICAL "1" LEVEL INPUT CURRENT VERSUS INPUT VOLTAGE



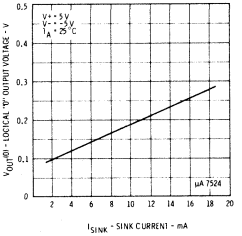
LOGICAL "0" LEVEL INPUT CURRENT VERSUS INPUT VOLTAGE



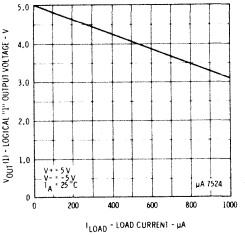
OUTPUT VOLTAGE VERSUS DIFFERENTIAL INPUT VOLTAGE



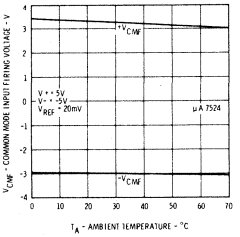
LOGICAL "0" OUTPUT VOLTAGE VERSUS SINK CURRENT



LOGICAL "1" OUTPUT VOLTAGE VERSUS LOAD CURRENT



COMMON-MODE FIRING VOLTAGE VERSUS AMBIENT TEMPERATURE



DEFINITION OF TERMS:

THRESHOLD VOLTAGE — The typical referred to input voltage which determines whether an input is a "1" or a "0". A signal whose magnitude is greater than the threshold level is sensed as a logic "1" and a signal whose magnitude is less as a "0".

THRESHOLD UNCERTAINTY — With all sense amps sharing the same input threshold setting, all input signals greater than the nominal threshold plus the uncertainty shall be sensed as a "1" and all input signals less than the nominal threshold less the uncertainty as a "0". This includes unit to unit, power supply and temperature variations.

PROPAGATION DELAY — The time delay measured from input threshold to output logic threshold with the strobe enabled.

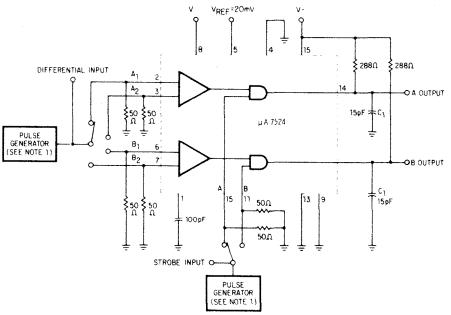
STROBE DELAY — The time delay measured from strobe to output logic threshold with a signal present exceeding the input threshold.

COMMON MODE RECOVERY TIME — The time from the turn off of the CM signal to the analog input threshold of the earliest sense line pulse signal that can be processed normally. Processed normally refers to bi-polar signals greater than or less than the input threshold with a corresponding proper output.

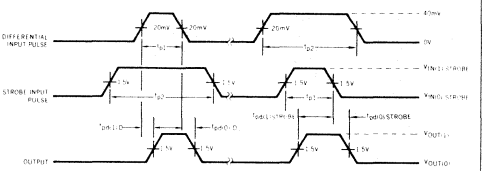
COMMON MODE FIRING VOLTAGE — The CM input voltage that exceeds the dynamic range of the inputs with strobe enabled resulting in the output switching states.

FIG. 1 PROPAGATION DELAY

TEST CIRCUITS

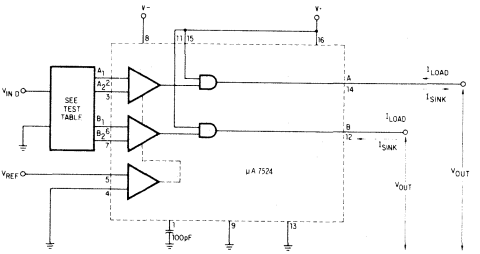


VOLTAGE WAVEFORMS



NOTES: 1. Pulse generators have the following characteristics:
$Z_{out} = 50\ \Omega$, $t_r = t_f = 15\ (\pm 5)$ ns, $t_{p1} = 100$ ns, $t_{p2} = 300$ ns, PRR = 1 MHz.
2. Strobe input pulse is applied to Strobe A when inputs A_1 - A_2 are being tested and to Strobe B when inputs B_1 - B_2 are being tested.
3. C_1 includes probe and jig capacitance.

FIG. 2 DC TEST



TEST TABLE

TYPE	INPUTS	V_{ref}	V_{inD}	OUTPUT		
				V_{out}	I_{sink}	I_{load}
μA7524	A_1 - A_2 or B_1 - B_2	15 mV	< 11 mV	⩽ 0.4 V	16 mA	—
	A_1 - A_2 or B_1 - B_2	15 mV	> 19 mV	⩾ 2.4 V	—	−400 μA
	A_1 - A_2 or B_1 - B_2	40 mV	< 36 mV	⩽ 0.4 V	16 mA	—
	A_1 - A_2 or B_1 - B_2	40 mV	> 44 mV	⩾ 2.4 V	—	−400 μA

μA7525
TWO CHANNEL CORE MEMORY SENSE AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

- **±2 mV THRESHOLD VARIATION**
- **25 ns PROPAGATION DELAY**
- **DUAL INDEPENDENT STROBES**
- **TTμL COMPATIBLE**

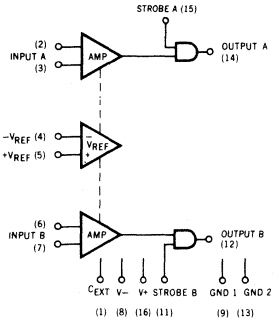
GENERAL DESCRIPTION — The μA7525 is a two channel core memory sense amplifier constructed on a silicon chip using the patented Fairchild Planar* epitaxial process. It can be used for small (1K to 8K words) memories as well as larger memory systems. The device is suitable for small core sizes facilitating very fast memory cycle times. The μA7525 features tight threshold accuracy, fast response time, and independent strobe selection. Unit to unit variations are minimized so that individual adjustments of the threshold and strobe timing are not necessary.

All logic inputs and outputs are fully TTμL compatible. The μA7525 is intended to be a pin for pin replacement for the 7525. The μA7525 can be combined with the Fairchild MSI Quad Latch 9314 to provide complete memory data register capability. For improved performance, see μA761C data sheet.

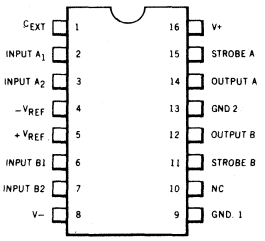
ABSOLUTE MAXIMUM RATINGS

Differential Input Voltage	±5.0 V
Supply Voltage	±7.0 V
Logic Input Voltage	+5.5 V
Power Dissipation (Note 1) 6M Package	400 mW
7B Package	500 mW
Storage Temperature 6M Package	−55°C to +125°C
7B Package	−65°C to +150°C
Operating Temperature	0°C to +70°C
Lead Temperature (6M Package, Soldering 10 seconds)	+260°C
(7B Package, Soldering 60 seconds)	+300°C
Signal Input	±3.0 V
Reference Input	±3.0 V

BLOCK DIAGRAM

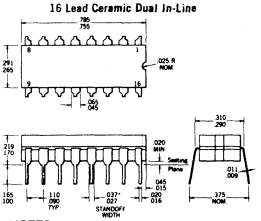


CONNECTION DIAGRAM



PHYSICAL DIMENSIONS

16 Lead Ceramic Dual In-Line



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020" diameter lead
Leads are tin-plated kovar
Package weight is 2.2 grams
*The .027/.037 dimension does not apply to the corner leads

ORDER PART NO. U7B7525393

Note 1: Rating applies for Ambient Temperature to 70°C.

*Planar is a patented Fairchild process.

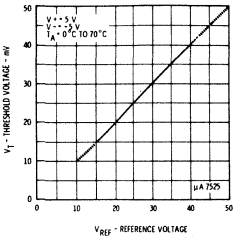
FAIRCHILD SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS ($V^+ = 5.0$ V, $V^- = -5.0$ V, 0°C to +70°C either Amplifier unless otherwise specified)

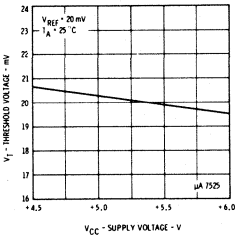
PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Threshold Voltage Range					
Minimum			10		mV
Maximum			50		mV
Threshold Uncertainty			±2.0		mV
Differential Input Threshold Voltage	$V_{ref} = 15$ mV	8.0		22	mV
	$V_{ref} = 40$ mV	33		47	mV
Differential Input Bias Current	$V_{IND} = 0$ mV		15	75	μA
Differential Input Offset Current	$V_{IND} = 0$ mV		1.0		μA
Differential Input Impedance	f = 1.0 kHz		2.5		kΩ
Positive Supply Current	$T_A = 25$°C		25		mA
Negative Supply Current	$T_A = 25$°C		10		mA
Output Short Circuit Current	$V^+ = 5.25$ V, $V^- = -5.25$ V	2.1		3.5	mA
LOGIC INPUT/OUTPUT CONDITIONS (See Fig. 2)					
Output Voltage Logical "1"	I Load = 400 μA $V_{in(1)}$ STROBE = 2.0 V $V_{in(0)}$ STROBE = 0.8 V $V^+ = 4.75$ V $V^- = -4.75$ V	2.4	3.9		V
Output Voltage Logical "0"	I Sink = 16 mA $V_{in(0)}$ STROBE = 0.8 V $V^+ = 4.75$ V $V^- = -4.75$ V		0.25	0.4	V
Logical "1" Input (Strobe Inputs)	$V_{in(0)}$ STROBE = 0.8 V $V^+ = 4.75$ V $V^- = -4.75$ V	2.0			V
Logical "0" Input (Strobe Inputs)	$V_{in(1)}$ STROBE = 2.0 V $V^+ = 4.75$ V $V^- = -4.75$ V			0.8	V
Logical "0" Input Current (Strobe Inputs)	$V_{in(0)}$ STROBE = 0.4 V $V^+ = 5.25$ V $V^- = -5.25$ V		−1.0	−1.6	mA
Logical "1" Input Current (Strobe Inputs)	$V_{in(1)}$ STROBE = 2.4 V $V^+ = 5.25$ V $V^- = -5.25$ V			40	μA
Logical "1" Input Current (Strobe Inputs)	$V_{in(1)}$ STROBE = V^+ $V^+ = 5.25$ V $V^- = -5.25$ V			1.0	mA
A.C. CHARACTERISTICS	$T_A = 25$°C				
Common Mode Input Firing Voltage	$t_r = t_f \leq 15$ ns $t_p = 50$ ns		±3.0		V
Differential Input Overload Recovery Time	$V_{in} + 2.0$ V, $t_r = t_f = 20$ ns		20		ns
Common Mode Input Overload Recovery Time	$V_{inCM} = \pm 2.0$ V, $t_r = t_f = 20$ ns		20		ns
Input to Output Delay	t_{pd} (1) D		25	40	ns
(See Figure 1)	t_{pd} (0) D		35		ns
Strobe to Output Delay	t_{pd} (1) STROBE		15	30	ns
(See Figure 1)	t_{pd} (0) STROBE		25		ns

TYPICAL PERFORMANCE CURVES

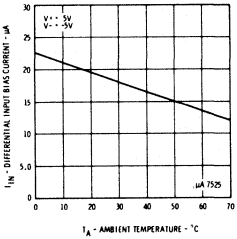
THRESHOLD VOLTAGE VERSUS REFERENCE VOLTAGE



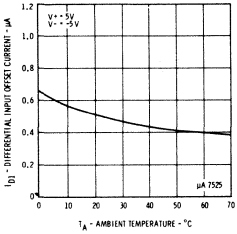
THRESHOLD VOLTAGE VERSUS SUPPLY VOLTAGE



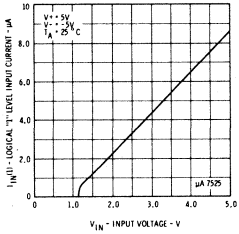
DIFFERENTIAL-INPUT BIAS CURRENT VERSUS AMBIENT TEMPERATURE



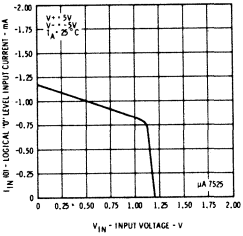
DIFFERENTIAL-INPUT OFFSET CURRENT VERSUS AMBIENT TEMPERATURE



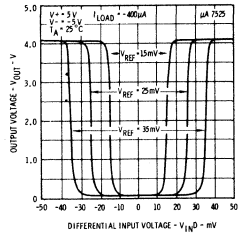
LOGICAL "1" LEVEL INPUT CURRENT VERSUS INPUT VOLTAGE



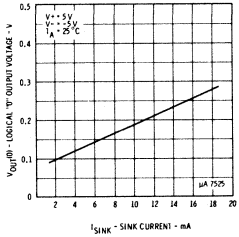
LOGICAL "0" LEVEL INPUT CURRENT VERSUS INPUT VOLTAGE



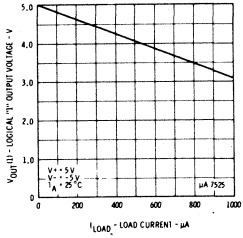
OUTPUT VOLTAGE VERSUS DIFFERENTIAL INPUT VOLTAGE



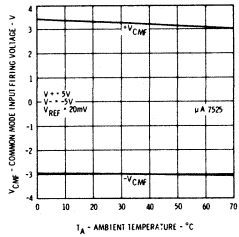
LOGICAL "0" OUTPUT VOLTAGE VERSUS SINK CURRENT



LOGICAL "1" OUTPUT VOLTAGE VERSUS LOAD CURRENT



COMMON-MODE FIRING VOLTAGE VERSUS AMBIENT TEMPERATURE



DEFINITION OF TERMS:

THRESHOLD VOLTAGE — The typical referred to input voltage which determines whether an input is a "1" or a "0". A signal whose magnitude is greater than the threshold level is sensed as a logic "1" and a signal whose magnitude is less as a "0".

THRESHOLD UNCERTAINTY — With all sense amps sharing the same input threshold setting, all input signals greater than the nominal threshold plus the uncertainty shall be sensed as a "1" and all input signals less than the nominal threshold less the uncertainty as a "0". This includes unit to unit, power supply and temperature variations.

PROPAGATION DELAY — The time delay measured from input threshold to output logic threshold with the strobe enabled.

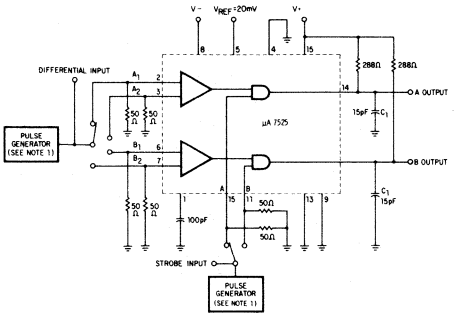
STROBE DELAY — The time delay measured from strobe to output logic threshold with a signal present exceeding the input threshold.

COMMON MODE RECOVERY TIME — The time from the turn off of the CM signal to the analog input threshold of the earliest sense line pulse signal that can be processed normally. Processed normally refers to bi-polar signals greater than or less than the input threshold with a corresponding proper output.

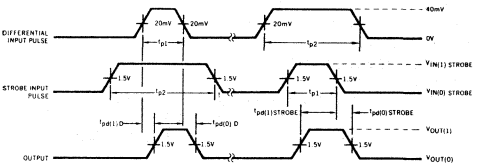
COMMON MODE FIRING VOLTAGE — The CM input voltage that exceeds the dynamic range of the inputs with strobe enabled resulting in the output switching states.

FIG. 1 PROPAGATION DELAY

TEST CIRCUITS

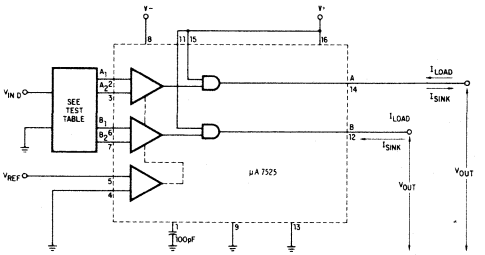


VOLTAGE WAVEFORMS



NOTES: 1. Pulse generators have the following characteristics: $Z_{out} = 50\ \Omega$, $t_r = t_f = 15\ (\pm 5)$ ns, $t_{p1} = 100$ ns, $t_{p2} = 300$ ns, PRR = 1 MHz.
2. Strobe input pulse is applied to Strobe A when inputs A_1 - A_2 are being tested and to Strobe B when inputs B_1 - B_2 are being tested.
3. C_1 includes probe and jig capacitance.

FIG. 2 DC TEST



TEST TABLE

TYPE	INPUTS	V_{ref}	V_{inD}	OUTPUT V_{out}	OUTPUT I_{sink}	OUTPUT I_{load}
μA7525	A_1 - A_2 or B_1 - B_2	15 mV	< 8 mV	⩽ 0.4 V	16 mA	—
	A_1 - A_2 or B_1 - B_2	15 mV	> 22 mV	⩾ 2.4 V	—	−400 μA
	A_1 - A_2 or B_1 - B_2	40 mV	< 33 mV	⩽ 0.4 V	16 mA	—
	A_1 - A_2 or B_1 - B_2	40 mV	> 47 mV	⩾ 2.4 V	—	−400 μA

9614

DUAL DIFFERENTIAL LINE DRIVER

FAIRCHILD INTEGRATED CIRCUIT

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 9614 is a CCSL compatible Dual Differential Line Driver. It is designed to drive transmission lines either differentially or single-ended, back-matched or terminated. The outputs are similar to TTμL, with the active pull-up and the pull-down split and brought out to adjacent pins. This allows multiplex operation (Wired-OR) at the driving site in either the single-ended mode via the uncommitted collector, or in the differential mode by use of the active pull-ups on one side and the uncommitted collectors on the other (See Fig. 5). The active pull-up is short circuit protected and offers a low output impedance to allow back-matching. The two pairs of outputs are complementary providing "NAND" and "AND" functions of the inputs adding greater flexibility. The input and output levels are CCSL compatible with clamp diodes provided at both input and output to handle line transients.

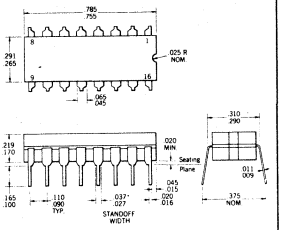
FEATURES:

- **SINGLE 5 VOLT SUPPLY**
- **CCSL COMPATIBLE INPUTS**
- **OUTPUT SHORT CIRCUIT PROTECTION**
- **INPUT CLAMP DIODES**
- **OUTPUT CLAMP DIODES FOR TERMINATION OF LINE TRANSIENTS**
- **COMPLIMENTARY OUTPUTS FOR 'NAND', 'AND' OPERATION**
- **UNCOMMITTED COLLECTOR OUTPUTS FOR WIRED-OR APPLICATION**
- **MILITARY TEMP RANGE**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Gnd Pin	−0.7 V to +7.0 V
Input Voltage	−0.5 V to +5.5 V
Voltage Supplied to Outputs (Open Collector)	−0.5 V to +12 V

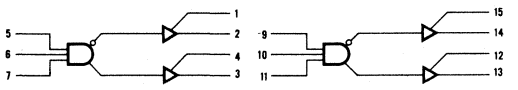
PHYSICAL DIMENSIONS
16 PIN DUAL IN-LINE PACKAGE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for a conventional .020 inch diameter Lead
Leads are tin-plated Kovar
Package weight is 2.0 grams
*The $\frac{.037}{.027}$ dimension does not apply to the corner leads

Fig. 1

LOGIC DIAGRAM



V_{CC} = Pin 16
Gnd = Pin 8

Fig. 3

16 PIN FLAT PACKAGE

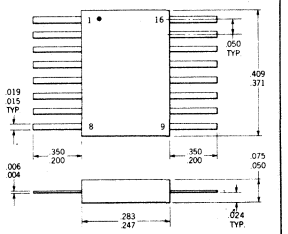


Fig. 2

ORDER INFORMATION

Specify U7B9614XXX for 16 Pin Dual In-Line package or U4L9614XXX for the 16 Pin Flatpak where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS
MILITARY TEMPERATURE RANGE (−55°C to +125°C, V_{CC} = 5.0 V ±10%) (U6B/4L961451X)

SYMBOL	CHARACTERISTIC	LIMITS							UNITS	CONDITIONS & COMMENTS	
		−55°C		+25°C			+125°C				
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.			
V_{OL}	Output Low Voltage		400		200	400		400	mV	I_{OL} = 40 mA	V_{CC} = 4.5 V
V_{OH}	Output High Voltage	2.4		2.4	3.2		2.4		V	I_{OH} = −10 mA	V_{CC} = 4.5 V
I_{SC}	Output "Short Circuit" Current			−40	−90	−120			mA	V_{OUT} = 0.0 V	V_{CC} = 5.5 V
I_{CEX}	Output Leakage Current				10	100		200	μA	V_{CEX} = 12.0 V	V_{CC} = 5.5 V
I_F	Input Forward Current		−1.60		−1.10	−1.60		−1.60	mA	V_F = 0.4 V	V_{CC} = 5.5 V
I_R	Input Reverse Current				35	60		100	μA	V_R = 4.5 V	V_{CC} = 5.5 V
V_{IL}	Guaranteed Input Low Voltage		0.8		1.3	0.9		0.8	V	V_{CC} = 5.5 V	
V_{IH}	Guaranteed Input High Voltage	2.0		1.7	1.5		1.4		V	V_{CC} = 4.5 V	
V_{OLC}	Clamped Output Low Voltage				−0.8	−1.5			V	I_{OLC} = −40 mA	V_{CC} = 5.5 V
I_{CC}	Supply Current				34	48.7			mA	Inputs = 0 V	V_{CC} = 5.5 V
I_{max}	Supply Current				46	65.7			mA	Inputs = 0 V	V_{MAX} = 7.0 V
t_{PLH}	Turn-Off Time				14	20			ns	C_L = 30 pF	V_{CC} = 5.0 V
t_{PHL}	Turn-On Time				18	20			ns	See Fig. 4	V_M = 1.5 V
V_{IC}	Input Clamp Voltage				−1.0	−1.5			V	V_{CC} = 4.5 V	I_{IC} = −12 mA

ELECTRICAL CHARACTERISTICS
INDUSTRIAL TEMPERATURE RANGE (0°C to +75°C, V_{CC} = 5.0 V ±5%) (U6B/4L961459X)

SYMBOL	CHARACTERISTIC	LIMITS							UNITS	CONDITIONS & COMMENTS	
		0°C		+25°C			+75°C				
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.			
V_{OL}	Output Low Voltage		450		200	450		450	mV	I_{OL} = 40 mA	V_{CC} = 4.75 V
V_{OH}	Output High Voltage	2.4		2.4	3.2		2.4		V	I_{OH} = −10 mA	V_{CC} = 4.75 V
I_{SC}	Output "Short Circuit" Current			−40	−90	−120			mA	V_{OUT} = 0.0 V	V_{CC} = 5.25 V
I_{CEX}	Output Leakage Current				10	100		200	μA	V_{CEX} = 5.25 V	V_{CC} = 5.25 V
I_F	Input Forward Current		−1.60		−1.10	−1.60		−1.60	mA	V_F = 0.45 V	V_{CC} = 5.25 V
I_R	Input Reverse Current				35	60		100	μA	V_R = 4.5 V	V_{CC} = 5.25 V
V_{IL}	Guaranteed Input Low Voltage		0.85		1.3	0.85		0.85	V	V_{CC} = 5.25 V	
V_{IH}	Guaranteed Input High Voltage	1.9		1.8	1.5		1.6		V	V_{CC} = 4.75 V	
V_{OLC}	Clamped Output Low Voltage				−0.8	−1.5			V	I_{OLC} = −40 mA	V_{CC} = 5.25 V
I_{CC}	Supply Current				33	48.7			mA	Inputs = 0 V	V_{CC} = 5.25 V
I_{max}	Supply Current				46	70			mA	Inputs = 0 V	V_{MAX} = 7.0 V
t_{PLH}	Turn-Off Time				14	30			ns	C_L = 30 pF	V_{CC} = 5.0 V
t_{PHL}	Turn-On Time				18	30			ns	See Fig. 4	V_M = 1.5 V
V_{IC}	Input Clamp Voltage				−1.0	−1.5			V	V_{CC} = 4.75 V	I_{IC} = −12 mA

SWITCHING CIRCUIT AND WAVEFORMS

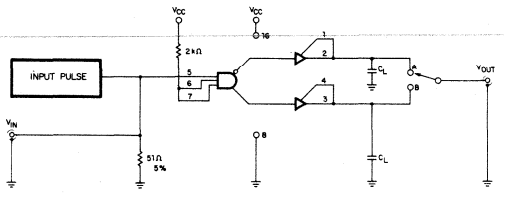
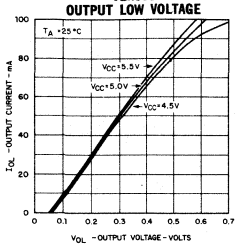


Fig. 4

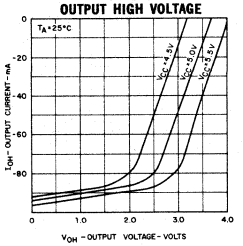
INPUT PULSE
Frequency = 500 kHz
Amplitude = 3.0 ±0.1 V
Pulse Width = 110 ±10 ns
$t_r = t_f \leq 5.0$ ns

TYPICAL ELECTRICAL CHARACTERISTICS

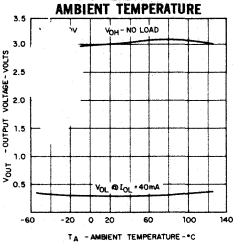
OUTPUT LOW CURRENT VERSUS OUTPUT LOW VOLTAGE



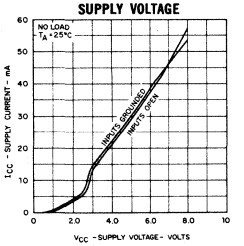
OUTPUT HIGH CURRENT VERSUS OUTPUT HIGH VOLTAGE



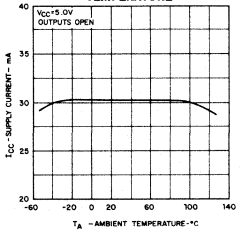
LOGIC LEVELS VERSUS AMBIENT TEMPERATURE



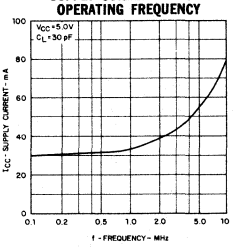
SUPPLY CURRENT VERSUS SUPPLY VOLTAGE



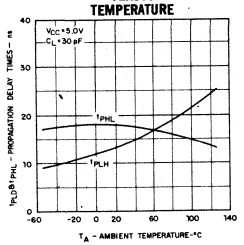
SUPPLY CURRENT VERSUS TEMPERATURE



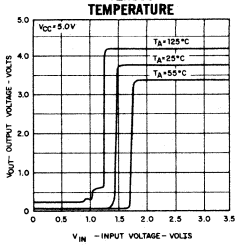
SUPPLY CURRENT VERSUS OPERATING FREQUENCY



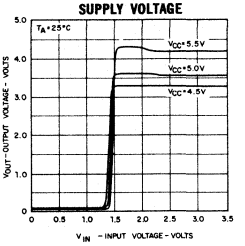
PROPAGATION DELAY TIME VERSUS TEMPERATURE



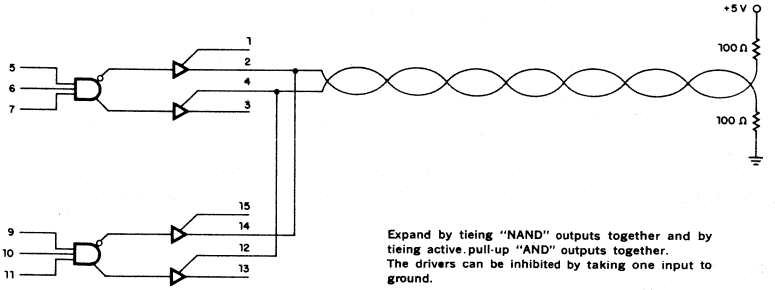
TRANSFER CHARACTERISTICS VERSUS TEMPERATURE



TRANSFER CHARACTERISTICS VERSUS SUPPLY VOLTAGE



APPLICATIONS



Expand by tieing "NAND" outputs together and by tieing active pull-up "AND" outputs together. The drivers can be inhibited by taking one input to ground.

Fig. 5 DIFFERENTIAL MODE EXPANSION

TYPICAL REFLECTION DIAGRAM

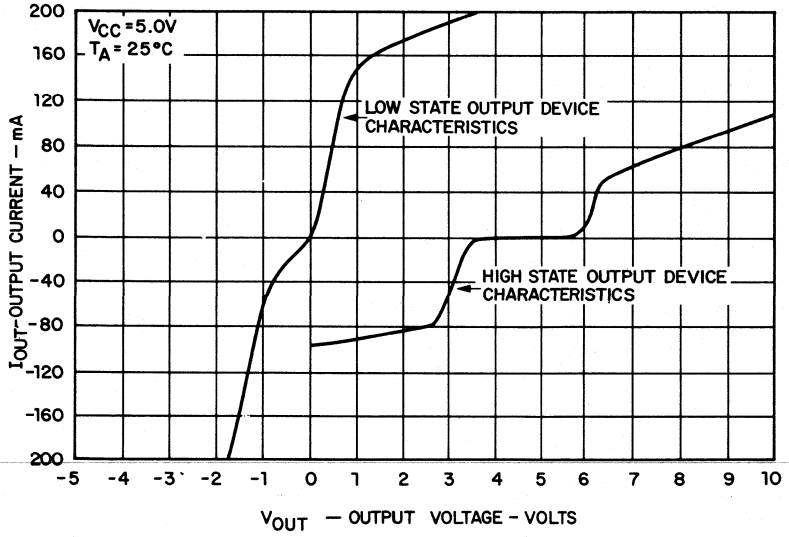


Fig. 6

9615

DUAL DIFFERENTIAL LINE RECEIVER

FAIRCHILD INTEGRATED CIRCUIT

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 9615 is a dual differential line receiver designed to receive differential digital data from transmission lines and operate over the military and industrial temperature ranges using a single 5 volt supply. It can receive ±500 mV of differential data in the presence of high level (±15 V) common mode voltages and deliver undisturbed CCSL logic to the output.

The response time can be controlled by use of an external capacitor. A strobe is provided along with a 130 Ω terminating resistor (at the inputs). The output has an uncommitted collector with an active pull-up available on an adjacent pin.

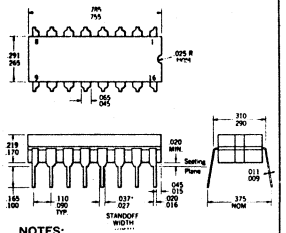
FEATURES:

- **CCSL COMPATIBLE OUTPUT**
- **HIGH COMMON MODE VOLTAGE RANGE**
- **CHOICE OF AN UNCOMMITTED COLLECTOR OR ACTIVE PULL-UP**
- **STROBE**
- **FULL MILITARY TEMPERATURE RANGE**
- **SINGLE 5 VOLT SUPPLY VOLTAGES**
- **FREQUENCY RESPONSE CONTROL**
- **130 Ω TERMINATING RESISTOR**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
Input Voltage Referred to Ground (Attenuator Inputs)	±20 V
Voltage Applied to Outputs-for High Output State without Active Pull-up	−0.5 V to +13.2 V
Voltage Applied to Strobe	−0.5 V to +5.5 V

PHYSICAL DIMENSIONS
16 PIN DUAL IN-LINE PACKAGE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead
Leads are tin plated Kovar
Package weight is 2.0 grams
*The .037 .027 dimension does not apply to the corner leads

Fig. 1

LOGIC DIAGRAM

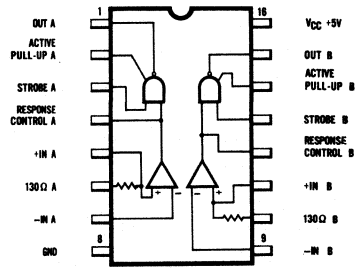


Fig. 3

16 PIN FLAT PACKAGE

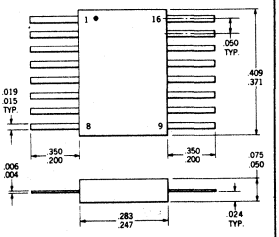


Fig. 2

ORDER INFORMATION

Specify U7B9614XXX for 16 pin Dual In-Line package or U4L9615XXX for 16 pin Flat Package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

FAIRCHILD SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS (Temperature Range −55°C to +125°C, V_{CC} = 5.0 V ±10%) (Part No. U6B/4L961551X)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OL}	Output Low Voltage		0.40		0.18	0.40		0.40	Volts	V_{CC} = 4.5 V, V_{OUT} = ** I_{OL} = 15.0 mA, *V_{DIFF} = 0.5 V
V_{OH}	Output High Voltage	2.2		2.4	3.2		2.4		Volts	V_{CC} = 4.5 V, V_{OUT} = ** I_{OH} = −5.0 mA, *V_{DIFF} = −0.5 V
I_{CEX}	Output Leakage Current					100		200	μA	V_{CEX} = 12 V, *V_{DIFF} = V_{CC} = 4.5 V
I_{SC}	Output Shorted Current			−15	−39	−80			mA	V_{CC} = 5.5 V, **V_{SC} = 0 V, *V_{DIFF} = −0.5 V
I_{IN}	Input Current		−0.9		−0.49	−0.7		−0.7	mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V Other Input = 5.5 V
$I_{IN(ST)}$	Strobe Input Current				−1.15	−2.4			mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V *V_{DIFF} = 0.5 V
$I_{IN(R-C)}$	Response Control Input Current			−1.2	−3.4				mA	V_{CC} = 5.5 V, *V_{DIFF} = 0.5 V
V_{CM}	Common Mode Voltage	−15	+15	−15	±17.5	+15	−15	+15	Volts	V_{CC} = 5.0 V, *V_{DIFF} = 2.0 V
$I_{R(ST)}$	Strobe Input Leakage Current					2.0		5.0	μA	V_{CC} = 4.5 V, *V_{DIFF} = −0.5 V V_R = 4.5 V
R_{IN}	Input Resistor			77	130	167			ohms	V_{CC} = 5.0 V, $V_{IN(R)}$ = 1.0 V, +Input = Gnd.
V_{TH}	Differential Input Threshold Voltage		500		80	500		500	mV	V_{CC} = 5.0 V ±10%
I_{CC}	Power Supply Current				28.7	50			mA	V_{CC} = 5.5 V, −Inputs = 0 V, +Inputs = 0.5 V
t_{pd+}	Turn-off Time				30	50			ns	R_L = 3.9 kΩ, V_{CC} = 5.0 V, C_L = 30 pF, Fig. 4
t_{pd-}	Turn-on Time				30	50			ns	R_L = 390 Ω, V_{CC} = 5.0 V, C_L = 30 pF, Fig. 4

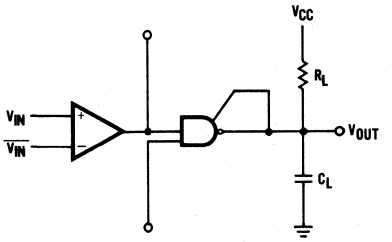
*V_{DIFF} is a differential input voltage referred from A+ to A− and from B+ to B−.
**Connect Output "A" to Active Pull-up "A" and Output "B" to Active Pull-up "B".

ELECTRICAL CHARACTERISTICS (Temperature Range 0°C to +75°C, V_{CC} = 5.0 V ±5%) (Part No. U6B/4L961559X)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OL}	Output Low Voltage		0.45		0.25	0.45		0.45	Volts	V_{CC} = 4.75 V, V_{OUT} = ** I_{OL} = 15.0 mA, *V_{DIFF} = 0.5 V
V_{OH}	Output High Voltage	2.4		2.4	3.3		2.4		Volts	V_{CC} = 4.75 V, V_{OUT} = ** I_{OH} = −5.0 mA, *V_{DIFF} = −0.5 V
I_{CEX}	Output Leakage Current					100		200	μA	V_{CEX} = 5.25 V, *V_{DIFF} = V_{CC} = 4.75 V
I_{SC}	Output Shorted Current			−14		−100			mA	V_{CC} = 5.25 V, **V_{SC} = 0 V, *V_{DIFF} = −0.5 V
I_{IN}	Input Current		−0.9		−0.49	−0.7		−0.7	mA	V_{CC} = 5.25 V, V_{IN} = 0.45 V Other Input = 5.25 V
$I_{IN(ST)}$	Strobe Input Current				−1.15	−2.4			mA	V_{CC} = 5.25 V, V_{IN} = 0.45 V *V_{DIFF} = 0.5 V
$I_{IN(R-C)}$	Response Control Input Current			−1.2	−3.4				mA	V_{CC} = 5.25 V, *V_{DIFF} = 0.5 V
V_{CM}	Common Mode Voltage	−15	+15	−15	±17.5	+15	−15	+15	Volts	V_{CC} = 5.0 V, *V_{DIFF} = 2.0 V
$I_{R(ST)}$	Strobe Input Leakage Current					5.0		10	μA	V_{CC} = 4.75 V, *V_{DIFF} = −0.5 V V_R = 4.5 V
R_{IN}	Input Resistor			74	130	179			ohms	V_{CC} = 5.0 V, $V_{IN(R)}$ = 1.0 V, +Input = Gnd.
V_{TH}	Differential Input Threshold Voltage		500		80	500		500	mV	V_{CC} = 5.0 V ±5%
I_{CC}	Power Supply Current				28.7	50			mA	V_{CC} = 5.25 V, +Inputs = 0.5 V, −Inputs = 0 V
t_{pd+}	Turn-off Time				30	75			ns	R_L = 3.9 kΩ, V_{CC} = 5.0 V, C_L = 30 pF, Fig. 4
t_{pd-}	Turn-on Time				30	75			ns	R_L = 390 Ω, V_{CC} = 5.0 V, C_L = 30 pF, Fig. 4

*V_{DIFF} is a differential input voltage referred from A+ to A− and from B+ to B−.
**Connect Output "A" to Active Pull-up "A" and Output "B" to Active Pull-up "B".

SWITCHING TIME TEST CIRCUIT



WAVEFORMS

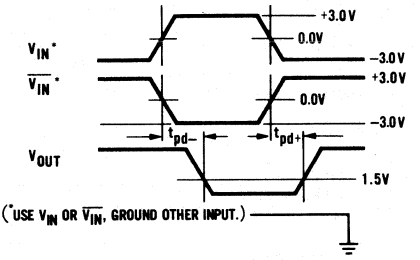
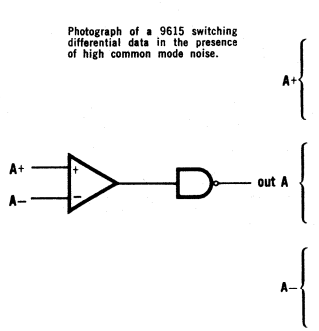
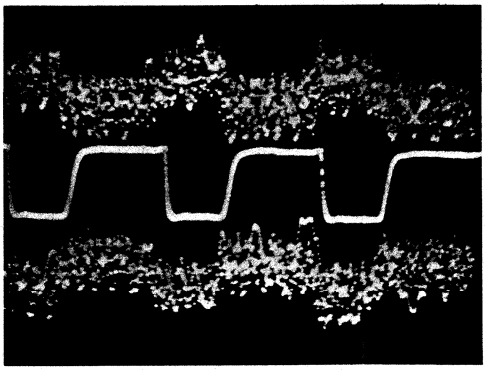


Fig. 4

Photograph of a 9615 switching differential data in the presence of high common mode noise.





VERTICAL=2.0V/DIV. HORIZONTAL=50ns/DIV.

Fig. 5

STANDARD USAGE

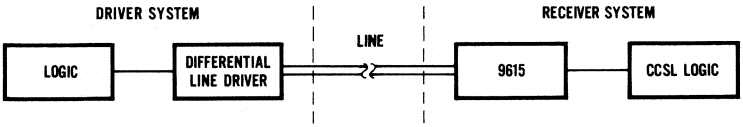
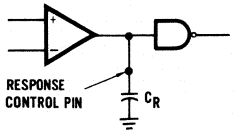


Fig. 6

FREQUENCY RESPONSE CONTROL



FREQUENCY RESPONSE VERSUS CAPACITANCE

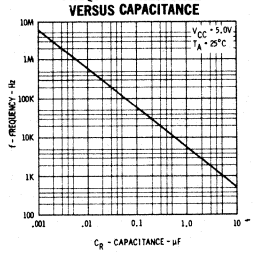
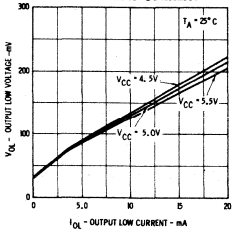


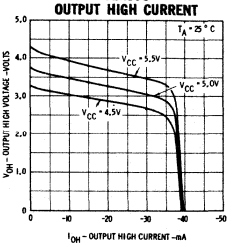
Fig. 7

TYPICAL ELECTRICAL CHARACTERISTICS

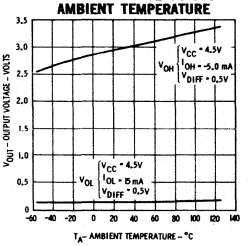
OUTPUT LOW VOLTAGE VERSUS OUTPUT LOW CURRENT



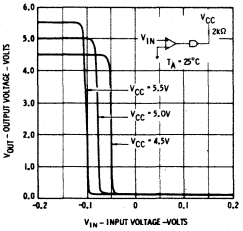
OUTPUT HIGH VOLTAGE VERSUS OUTPUT HIGH CURRENT



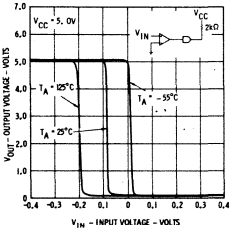
OUTPUT VOLTAGE VERSUS AMBIENT TEMPERATURE



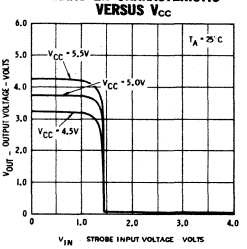
INPUT-OUTPUT TRANSFER CHARACTERISTIC VERSUS V_{CC}



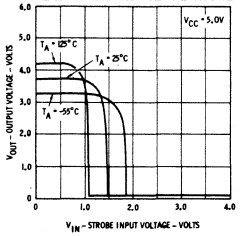
INPUT-OUTPUT TRANSFER CHARACTERISTIC VERSUS TEMPERATURE



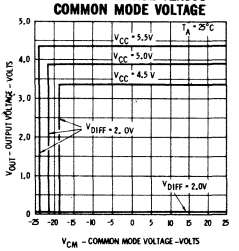
STROBE INPUT-OUTPUT TRANSFER CHARACTERISTIC VERSUS V_{CC}



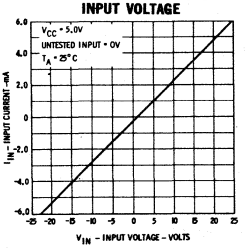
STROBE INPUT-OUTPUT TRANSFER CHARACTERISTIC VERSUS AMBIENT TEMPERATURE



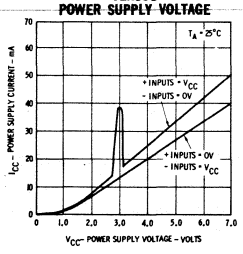
OUTPUT VOLTAGE VERSUS COMMON MODE VOLTAGE



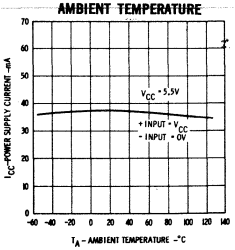
INPUT CURRENT VERSUS INPUT VOLTAGE



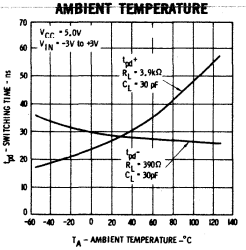
POWER SUPPLY CURRENT VERSUS POWER SUPPLY VOLTAGE



POWER SUPPLY CURRENT VERSUS AMBIENT TEMPERATURE



SWITCHING TIME VERSUS AMBIENT TEMPERATURE



9620
DUAL DIFFERENTIAL LINE RECEIVER
FAIRCHILD INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 9620 is a dual differential line receiver designed to receive differential digital data from transmission lines and operate over the military and industrial temperature ranges. It can receive ±500 mV of differential data in the presence of high level (±15 V) common mode voltages and deliver undisturbed CCSL logic to the output. In addition to line reception the 9620 can perform many functions, a few of which are presented in the applications section. It can interface with nearly all input logic levels including CML, CTμL, HLLDTμL, RTμL and CCSL. HLLDTμL logic can be provided by tieing the output to V_{CC2}(+12 V) through a resistor. The outputs can also be wire OR'ed. The 9620 offers the advantages of logic compatible voltages (+5 V, +12 V), CCSL output characteristics, and a flexible input array with a high common mode range. The direct inputs are provided in addition to the attenuated inputs (normally used) to allow the input attenuation and response time to be changed by use of external components.

FEATURES:

- **CCSL COMPATIBLE OUTPUT**
- **HIGH COMMON MODE VOLTAGE RANGE**
- **WIRED-OR CAPABILITY**
- **DIRECT INPUTS (A_D, B_D)**
- **FULL MILITARY TEMPERATURE RANGE**
- **LOGIC COMPATIBLE SUPPLY VOLTAGES**

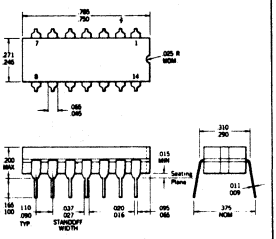
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC1} Pin Potential to Ground Pin	−0.5 V to +7.0 V
Input Voltage Referred to Ground (Attenuator Inputs)	±20 V
Voltage Applied to Outputs for High Output State	−0.5 V to +13.2 V
V_{CC2} Pin Potential to Ground Pin	V_{CC1} to +15 V

ORDER INFORMATION

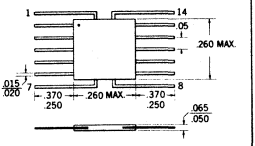
Specify U6A9620XXX for 14 pin Dual In-Line package or U3I9620XXX for 14 pin Flat Package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

TYPICAL DUAL IN-LINE PACKAGE
In Accordance With
JEDEC (TO-116) Outline

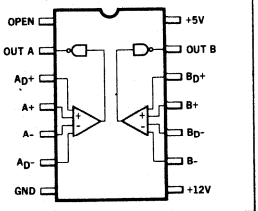


NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.
2. Board drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

14-PIN FLAT PACKAGE



LOGIC DIAGRAM



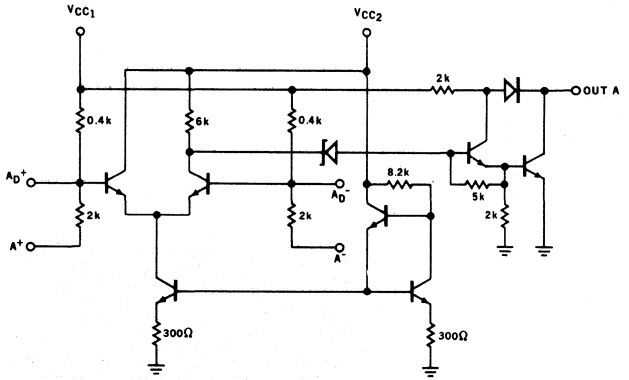
FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS (Temperature Range −55°C to +125°C, $V_{CC1} = 5.0\ V \pm 10\%$, $V_{CC2} = 12.0\ V \pm 10\%$)

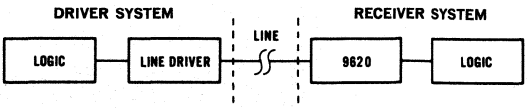
SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	−55°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+125°C MIN.	+125°C MAX.	UNITS	CONDITIONS & COMMENTS	
V_{OL}	Output Low Voltage		0.40		0.25	0.40		0.45	Volts	$V_{CC1} = 4.5\ V$ $I_{OL} = 15.0\ mA$	$V_{CC2} = 10.8\ V$ $*V_{DIFF} = 0.5\ V$
V_{OH}	Output High Voltage	2.8		3.0	3.3		2.9		Volts	$V_{CC1} = 4.5\ V$ $I_{OH} = -0.2\ mA$	$V_{CC2} = 10.8\ V$ $*V_{DIFF} = -0.5\ V$
I_{CEX}	Output Leakage Current		50			100		200	μA	$V_{CEX} = 13.2\ V$	
I_{SC}	Output Shorted Current			−1.4	−2.15	−3.1			mA	$V_{CC1} = 5.0\ V$	$V_{CC2} = 12.0\ V$
I_F	Input Forward Current		−3.1		−2.1	−3.0		−3.0	mA	$V_{CC1} = 5.0\ V$	$V_{CC2} = 12.0\ V$
†V_{TH}	Differential Input Threshold Voltage		500		120	500		500	mV	$V_{CC1} = 5.0\ V$	$V_{CC2} = 12.0\ V$
†V_{CM}	Common Mode Voltage	−15	15	−15	±17.5	15	−15	15	Volts	$V_{CC1} = 5.0\ V$ $*V_{DIFF} = 2.0\ V$	$V_{CC2} = 12.0\ V$
I_{VCC1}	5 V Supply Current		13		8.2	13		13	mA	$V_{CC1} = 5.5\ V$ $V_{CC2} = 13.2\ V$	+Input = 5.5 V −Input = 0 V
I_{VCC2}	12 V Supply Current		8.0		5.6	8.0		8.0	mA	$V_{CC1} = 5.5\ V$ $V_{CC2} = 13.2\ V$	+Input = 5.5 V −Input = 0 V
t_{pd+}	Turn-off Time				35	50			ns	$R_L = 3.9\ k\Omega$	$C_L = 30\ pF$
t_{pd-}	Turn-on Time				20	50			ns	$R_L = 390\ \Omega$	$C_L = 30\ pF$

†All input voltages are referred to the attenuated inputs (A^+, A^-, B^+, B^-)
*V_{DIFF} is a differential input voltage referred from A+ to A− and from B+ to B−.

Fig. 1 — SCHEMATIC DIAGRAM



STANDARD USAGE

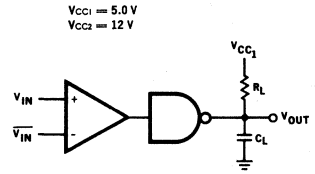


ELECTRICAL CHARACTERISTICS (Temperature Range 0°C to +75°C, $V_{CC1} = 5.0\ V \pm 5\%$, $V_{CC2} = 12.0\ V \pm 5\%$)

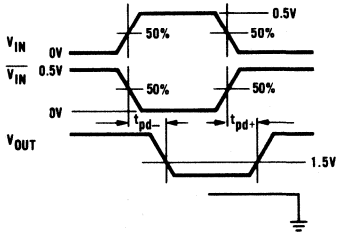
SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+75°C MIN.	+75°C MAX.	UNITS	CONDITIONS & COMMENTS	
V_{OL}	Output Low Voltage		0.45		0.25	0.45		0.50	Volts	$V_{CC1} = 4.75\ V$ $I_{OL} = 15.0\ mA$	$V_{CC2} = 11.4\ V$ $*V_{DIFF} = 0.5\ V$
V_{OH}	Output High Voltage	2.8		3.0	3.3		2.9		Volts	$V_{CC1} = 4.75\ V$ $I_{OH} = -0.2\ mA$	$V_{CC2} = 12.6\ V$ $*V_{DIFF} = -0.5\ V$
I_{CEX}	Output Leakage Current		50			100		200	μA	$V_{CEX} = 5.25\ V$	
I_{SC}	Output Shorted Current			−1.4	−2.15	−3.1			mA	$V_{CC1} = 5.0\ V$	$V_{CC2} = 12.0\ V$
I_F	Input Forward Current		−3.1		−2.1	−3.0		−3.0	mA	$V_{CC1} = 5.0\ V$	$V_{CC2} = 12.0\ V$
$\dagger V_{TH}$	Differential Input Threshold Voltage		500		120	500		500	mV	$V_{CC1} = 4.75\ V$	$V_{CC2} = 12.6\ V$
$\dagger V_{CM}$	Common Mode Voltage	−12	12	−12	±17.5	12	−12	12	Volts	$V_{CC1} = 5.0\ V$ $*V_{DIFF} = 2.0\ V$	$V_{CC2} = 12.0\ V$
I_{VCC1}	5 V Supply Current		13.5		8.2	13.5		13.5	mA	$V_{CC1} = 5.25\ V$ $V_{CC2} = 12.6\ V$	+Input = 5.25 V −Input = 0 V
I_{VCC2}	12 V Supply Current		8.5		5.6	8.5		8.5	mA	$V_{CC1} = 5.25\ V$ $V_{CC2} = 12.6\ V$	+Input = 5.25 V −Input = 0 V
t_{pd+}	Turn-off Time				35	75			ns	$R_L = 3.9\ k\Omega$	$C_L = 30\ pF$
t_{pd-}	Turn-on Time				20	75			ns	$R_L = 390\ \Omega$	$C_L = 30\ pF$

†All input voltages are referred to the attenuated inputs (A^+, A^-, B^+, B^-)
*V_{DIFF} is a differential input voltage referred from A+ to A− and from B+ to B−.

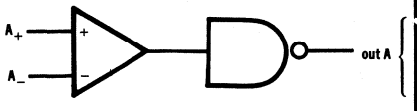
Fig. 2 — SWITCHING TIME TEST CIRCUIT

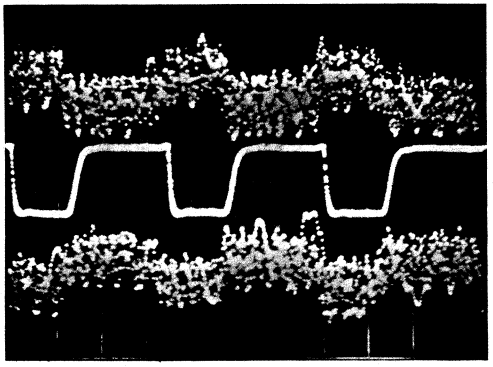


WAVEFORMS



Photograph of a 9620 switching differential data in the presence of high common mode noise.

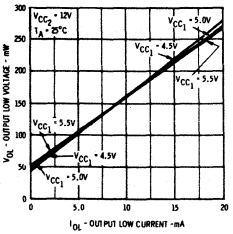




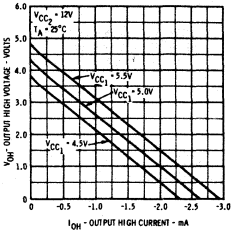
VERT = 2.0 V/div. HORIZ = 50 ns/div.

TYPICAL ELECTRICAL CHARACTERISTICS

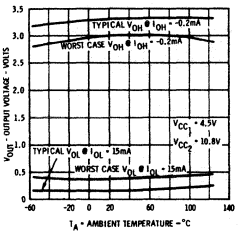
TYPICAL OUTPUT LOW VOLTAGE VERSUS OUTPUT LOW CURRENT



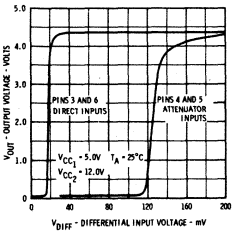
TYPICAL OUTPUT HIGH VOLTAGE VERSUS OUTPUT HIGH CURRENT



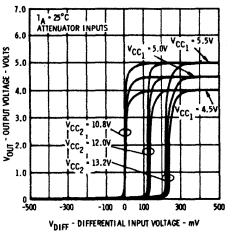
LOGIC LEVELS VERSUS AMBIENT TEMPERATURE



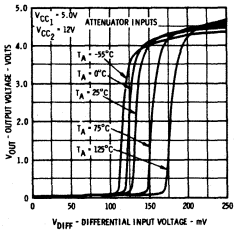
TYPICAL V_{out} VERSUS V_{DIFF} TRANSFER CHARACTERISTIC



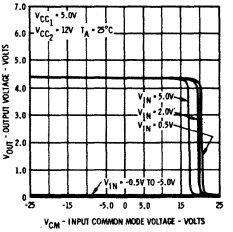
TYPICAL V_{out} VERSUS V_{DIFF} TRANSFER CHARACTERISTIC



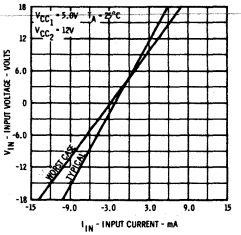
TYPICAL V_{out} VERSUS V_{DIFF} TRANSFER CHARACTERISTIC



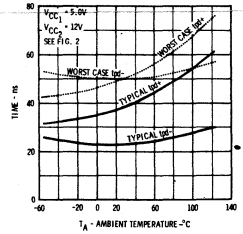
TYPICAL V_{out} VERSUS V_{CM} CHARACTERISTICS



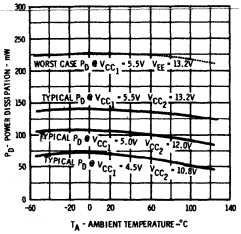
INPUT VOLTAGE VERSUS INPUT CURRENT



SWITCHING TIME VERSUS AMBIENT TEMPERATURE

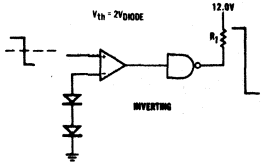


POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



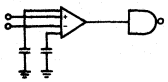
APPLICATIONS

DIGITAL COMPARATOR WITH DIODE REFERENCE AND HIGH LEVEL LOGIC OUT

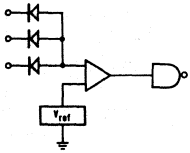


$R_1 \geq 750\ \Omega$

DIGITAL DIFFERENTIAL LINE RECEIVER WITH INPUTS ROLLED OFF

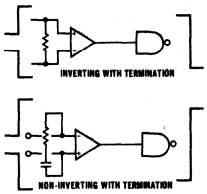


EXPANDED INTERFACE

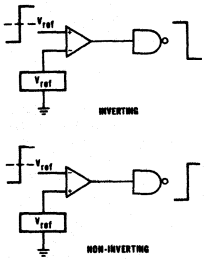


V_{ref} = Resistor, Diodes, or Supply

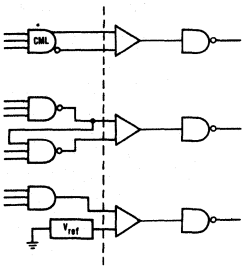
DIGITAL DIFFERENTIAL AMPLIFIER (Line Receiver)



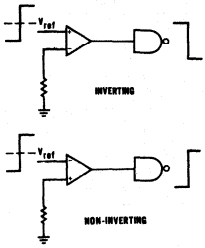
DIGITAL COMPARATOR



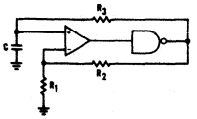
INTERFACING METHODS



DIGITAL COMPARATOR WITH RESISTIVE DIVIDER AS REFERENCE

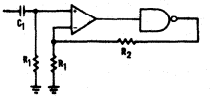


MULTIVIBRATOR



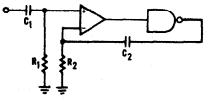
TYPICALLY
$R_1 = 1.6\ k\Omega$, $R_2 = 2.7\ k\Omega$, $T = 1.3\ R_1C$

A.C. COUPLED DIGITAL AMPLIFIER WITH HYSTERESIS



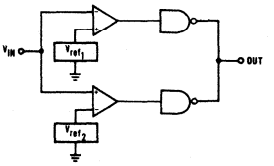
TYPICALLY
$R_1 = 1.6\ k\Omega$, $R_2 = 2.7\ k\Omega$

MONOSTABLE MULTIVIBRATOR NEGATIVE EDGE TRIGGERING



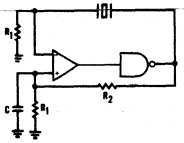
TYPICALLY
$C_1 = 0.1\ \mu F$, $R_1 = 1.2\ k\Omega$, $R_2 = 1.0\ k\Omega$
Pulse Width = $50\ ns + 3.15 \times 10^3\ C_2$

DOUBLE-ENDED COMPARATOR



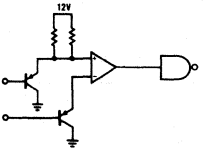
$V_{OH} = V_{Ref1} < V_{IN} < V_{Ref2}$

CRYSTAL CONTROLLED MULTIVIBRATOR



TYPICALLY
$R_1 = 1.6\ k\Omega$, $R_2 = 2.7\ k\Omega$, $C = \frac{R_2}{1000}$

HIGH INPUT IMPEDANCE LINE RECEIVER (Positive Signals Only)



9621
DUAL-LINE DRIVER
FAIRCHILD INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 9621 was designed to drive transmission lines in either a differential or a single-ended mode. Output clamp diodes and back-matching resistors for 130Ω twisted pair are provided. The output has the capability of driving high capacitance loads. It can typically switch >200 mA during transients.

FEATURES

- **CCSL COMPATIBILITY**
- **TRANSMISSION LINE BACK-MATCHING**
- **OUTPUT CLAMP DIODES**
- **HIGH CAPACITANCE DRIVE**
- **HIGH OUTPUT VOLTAGE**
- **MILITARY TEMPERATURE RANGE**

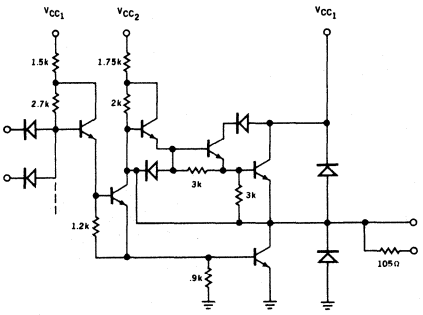
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC1} Pin Potential to Ground Pin	+3.8 V to +8 V
Input Voltage	−.5 V to +15 V
Voltage Applied to Outputs	−2 V to +V_{CC1} + 1 V
V_{CC2} Pin Potential to Ground Pin	V_{CC1} to +15 V

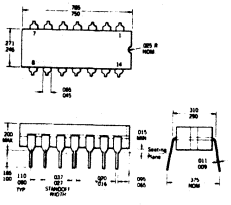
ORDER INFORMATION

Specify U6A9621XXX for 14 pin Dual In-Line Package or U319621XXX for 14 pin Flat Package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

SCHEMATIC DIAGRAM

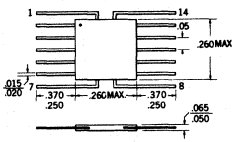


TYPICAL DUAL IN-LINE PACKAGE
Similar to
JEDEC (TO-116) Outline

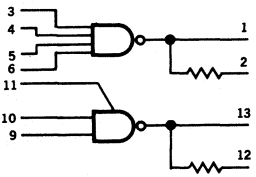


NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

14 PIN FLAT PACKAGE



LOGIC DIAGRAM



V_{CC_1}=14
V_{CC_2}=8
GND=7

FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS
MILITARY TEMPERATURE RANGE −55°C to +125°C (UXX962151X)

SYMBOL	NOTES	CHARACTERISTICS	LIMITS						UNITS	CONDITIONS & COMMENTS	
			−55°C		+25°C			+125°C			
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN. MAX.			
V_{OL}		Output Low Voltage		350		200	350	400	mV	I_{OL} = 20 mA	V_{CC1} = 4.5 V V_{CC2} = 10.8 V
V_{OH}		Output High Voltage	4.0		4.0	4.3		4.0	V	I_{OH} = −20 mA	V_{CC1} = 4.5 V V_{CC2} = 10.8 V
I_{SC}	1	Output "Short Circuit" Current			−180	−300			mA	V_{OUT} = 0 V	V_{CC1} = 4.5 V V_{CC2} = 10.8 V
I_{OL}	1	Output Low Current			150	200			mA	V_{OUT} = 5.0 V	V_{CC1} = 4.5 V V_{CC2} = 10.8 V
I_F		Input Forward Current		1.8		1.15	1.8	1.8	mA	V_F = 0 V	V_{CC1} = 5.5 V V_{CC2} = 13.2 V
I_R		Input Reverse Current		2.0		<1.0	2.0	5.0	μA	V_R = 5.5 V	V_{CC1} = 5.5 V V_{CC2} = 13.2 V
V_{OLR}	2	Resistive Output Low Voltage				380	500		V	I_{OL} = 2.8 mA	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
V_{OHR}	2	Resistive Output High Voltage			4.0	4.2			V	I_{OH} = −2.3 mA	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
V_{OLC}	3	Clamped Output Low Voltage				−1.0	−2.0		V	I_{OL} = −20 mA	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
V_{OHC}	3	Clamped Output High Voltage				6.0	7.0		V	I_{OH} = 20 mA	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
I_{CC1}		+5 V Supply Current		7.0		4.7	7.0	7.3	mA	Inputs Open	V_{CC1} = 5.5 V V_{CC2} = 13.2 V
I_{CC2}		+12 V Supply Current		9.8		6.5	9.8	9.8	mA		
t_{pd+}	4	Turn-Off Time				30	150		ns	C_L = 5000 pF	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
t_{pd-}	4	Turn-On Time				80	150		ns		
t_{pd+}		Turn-Off Time				13	25		ns	C_L = 30 pF	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
t_{pd-}		Turn-On Time				9	25		ns		
V_{IL}		Input Low Voltage		1.3		1.5	1.0	0.7	V	V_{CC1} = 5.5 V V_{CC2} = 10.8 V	
V_{IH}		Input High Voltage	2.2		2.0	1.7		1.8	V	V_{CC1} = 4.5 V V_{CC2} = 13.2 V	

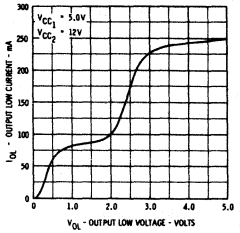
NOTES:
(1) Pulse tests to insure transient current handling (test time = 3 seconds maximum — one side only).
(2) Test output resistance including 105Ω output resistor.
(3) Tests output clamp diodes.
(4) With both sides loaded at T_A = +125°C, maximum frequency = 500 kHz for Dual In-Line package (θ_{JA} = 95°C/W) or 300 kHz for Ceramic Flat Pak (θ_{JA} = 165°C/W).

ELECTRICAL CHARACTERISTICS
INDUSTRIAL TEMPERATURE RANGE 0°C to +75°C (UXX962159X)

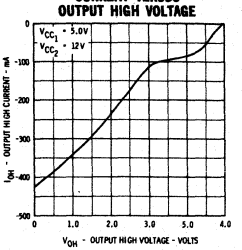
SYMBOL	NOTES	CHARACTERISTICS	LIMITS							UNITS	CONDITIONS & COMMENTS	
			0°C		+25°C			+75°C				
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.			
V_{OL}		Output Low Voltage		400		200	400		450	mV	I_{OL} = 20 mA	V_{CC1} = 4.75 V V_{CC2} = 11.4 V
V_{OH}		Output High Voltage	4.2		4.2	4.4		4.2		V	I_{OH} = −20 mA	V_{CC1} = 4.75 V V_{CC2} = 11.4 V
I_{SC}	1	Output "Short Circuit" Current			−100	−300				mA	V_{OUT} = 0 V	V_{CC1} = 4.75 V V_{CC2} = 11.4 V
I_{OL}	1	Output Low Current			75	200				mA	V_{OUT} = 5.0 V	V_{CC1} = 4.75 V V_{CC2} = 11.4 V
I_F		Input Forward Current		1.8		1.15	1.8		1.8	mA	V_F = 0 V	V_{CC1} = 5.25 V V_{CC2} = 12.6 V
I_R		Input Reverse Current		5.0		<1.0	5.0		10.0	μA	V_R = 5.5 V	V_{CC1} = 5.25 V V_{CC2} = 12.6 V
V_{OLR}	2	Resistive Output Low Voltage				380	500			V	I_{OL} = 2.8 mA	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
V_{OHR}	2	Resistive Output High Voltage			4.0	4.2				V	I_{OH} = −2.3 mA	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
V_{OLC}	3	Clamped Output Low Voltage				−1.0	−2.0			V	I_{OL} = −20 mA	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
V_{OHC}	3	Clamped Output High Voltage				6.0	7.0			V	I_{OH} = 20 mA	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
I_{CC1}		+5 V Supply Current		7.0		4.7	7.0		7.3	mA	Inputs Open	V_{CC1} = 5.25 V V_{CC2} = 12.6 V
I_{CC2}		+12 V Supply Current		9.8		6.5	9.8		9.8	mA		
t_{pd+}	4	Turn-Off Time				30	200			ns	C_L = 5000 pF	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
t_{pd-}	4	Turn-On Time				80	200			ns		
t_{pd+}		Turn-Off Time				13	40			ns	C_L = 30 pF	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
t_{pd-}		Turn-On Time				9	40			ns		
V_{IL}		Input Low Voltage		1.3		1.5	1.0		0.7	V	V_{CC1} = 5.25 V V_{CC2} = 12.6 V	
V_{IH}		Input High Voltage	2.2		2.0	1.7		1.8		V	V_{CC1} = 4.75 V V_{CC2} = 11.4 V	

NOTES:
(1) Pulse tests to insure transient current handling (test time = 3 seconds maximum — one side only).
(2) Test output resistance including 105Ω output resistor.
(3) Tests output clamp diodes.
(4) Maximum frequency = 500 kHz with both sides loaded at T_A = +75°C for both Dual In-Line package and Ceramic Flat Pak.

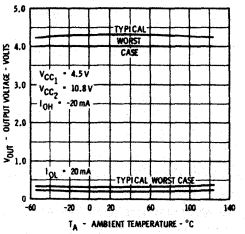
TYPICAL OUTPUT LOW CURRENT VERSUS OUTPUT LOW VOLTAGE



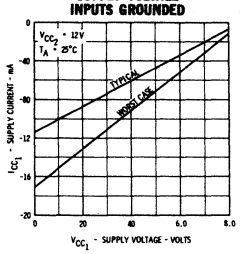
TYPICAL OUTPUT HIGH CURRENT VERSUS OUTPUT HIGH VOLTAGE



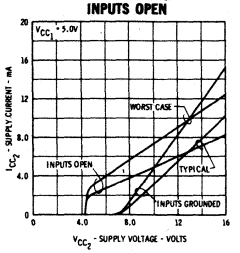
LOGIC LEVELS VERSUS AMBIENT TEMPERATURE



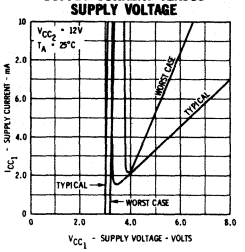
SUPPLY CURRENT VERSUS SUPPLY VOLTAGE INPUTS GROUNDED



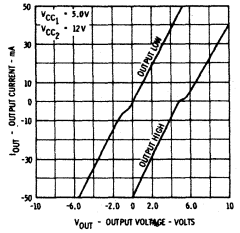
SUPPLY CURRENT VERSUS SUPPLY VOLTAGE INPUTS OPEN



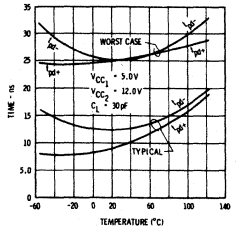
SUPPLY CURRENT VERSUS SUPPLY VOLTAGE



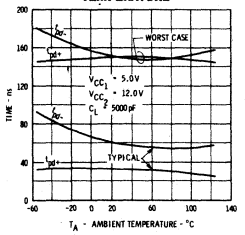
TYPICAL OUTPUT IMPEDANCE WITH BACK MATCHING RESISTORS



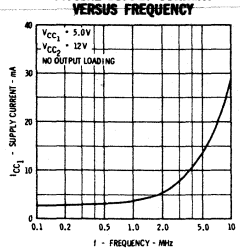
SWITCHING TIME VERSUS TEMPERATURE



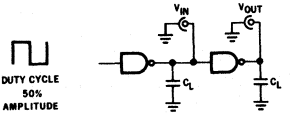
SWITCHING TIME VERSUS TEMPERATURE



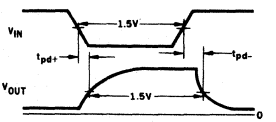
TYPICAL SUPPLY CURRENT VERSUS FREQUENCY



SWITCHING TIME TEST CIRCUIT



WAVEFORMS



DESCRIPTION OF REFLECTION DIAGRAM USAGE

The reflections on any line may be found by using the following procedure:

1. Draw the driver output characteristics for both the "high state" and the "low state" on an I - V graph in the same manner as the reflection diagram.
2. Draw the receiver input characteristic on the same graph. The two points of intersection of the receiver and driver characteristics are the two DC operating points.
3. Choose to analyze either the reflections for the output going low or high. In the example chosen the negative transition is analyzed.
4. Draw a line with a slope equal to the impedance of the line to be used, ($Z_0 = 100\Omega$ in the example), from the "high state" operating point (labeled A on our graph) to the "low state" output device characteristic (B_1). B_1 equals the conditions at the driver output immediately after turn-on.
5. Reverse the slope of Z_0 and sketch it from B_1 to the receiver input characteristic (C_1). C_1 equals the conditions at the receiver when the wavefront B_1 first reaches it.
6. By continuing this procedure of reversing the slope of Z_0 at each node all the reflections (B_1, C_1, B_2, C_2, B_3, C_3 - - - B_N, C_N), where B_X is the voltage at the driver and C_X is the voltage at the receiver, can be found.

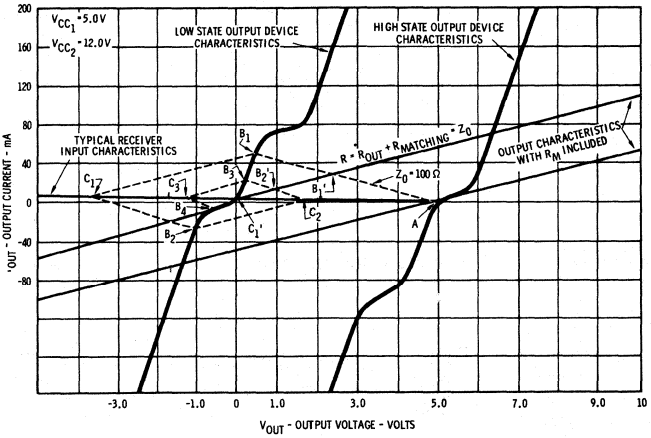
The same procedure is used to check the reflections when switching the output high.

BACK-MATCHING, also referred to as reverse termination, offers several advantages to the user. It reduces the system power by not requiring the high current for resistive termination and it reduces the DC line losses because IR drops in the line become minimum.
To back-match any line (output switching low):

1. Measure the output resistance, R_{out}, from the "low state" operating point to B_1.
2. Subtract R_{out} from Z. ($R_{out} + R_M = Z_0$). This value R_M, is the required back-matching resistance.
3. Place R_M in series with the output of driver.
4. The reflections that occur on the line with R_M inserted can be treated in the same manner as the general case. The results are B_1' and C_1' and the receiver will not see any reflections.

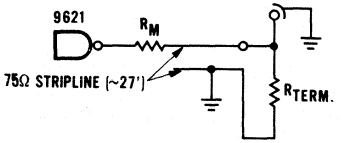
When switching the line differentially $R_M + R_{out} = Z_0/2$. The matched output characteristics of the 9621 make it possible to back-match effectively and require analysis of switching only one state.

TYPICAL REFLECTION DIAGRAM*



* GRAPHICAL ANALYSIS
First Presented by John B. James of I.C.T. (Eng.) LTD.

REFLECTION TEST CIRCUIT

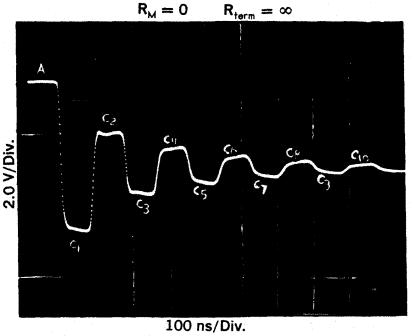


The reflections are two delay's of the line wide. R_{term} is the total impedance seen at the receiving end.

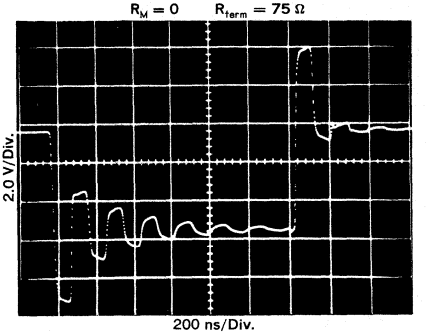
BACK MATCHING TABLE

Z_O	R_M when used single ended	R_M when used differentially
50 Ω	32 Ω	16 Ω
75 Ω	62 Ω	30 Ω
92 Ω	82 Ω	41 Ω
100 Ω	90 Ω	45 Ω
130 Ω	120 Ω	60 Ω
300 Ω	290 Ω	145 Ω
600 Ω	590 Ω	295 Ω

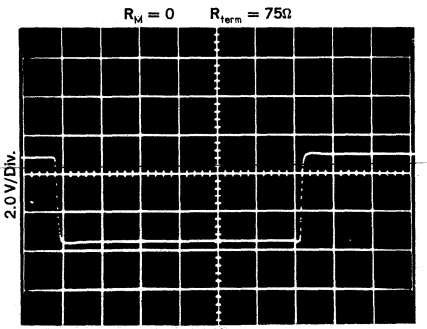
$R_M = 0$ $R_{term} = \infty$



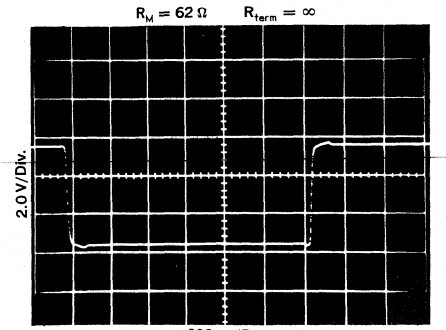
$R_M = 0$ $R_{term} = 75\ \Omega$



$R_M = 0$ $R_{term} = 75\Omega$



$R_M = 62\ \Omega$ $R_{term} = \infty$



9622
DUAL LINE RECEIVER
A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 9622 is a dual line receiver designed to discriminate a worst case logic swing of 2 volts from a ± 10 volt common mode noise signal or ground shift. A 1.5 volt threshold is built into the differential amplifier to offer a CCSL compatible threshold voltage and maximum noise immunity. The offset is obtained by use of current sources and matched resistors and varies only ± 5% (75 mV) over the military and industrial temperature ranges.

The 9622 allows the choice of output states with the inputs open without affecting circuit performance by use of S3. A 130 Ω terminating resistor is provided at the input of the each line receiver. An enable is also provided for each line receiver. The output is CCSL compatible. The output high level can be increased to +12 V by tieing it to a positive supply through a resistor. The outputs can be wire-OR'ed.

FEATURES:

- **CCSL COMPATIBLE THRESHOLD VOLTAGE**
- **INPUT TERMINATING RESISTORS**
- **CHOICE OF OUTPUT STATE WITH INPUTS OPEN**
- **CCSL COMPATIBLE OUTPUT**
- **HIGH COMMON MODE**
- **WIRE-OR CAPABILITY**
- **ENABLE INPUTS**
- **FULL MILITARY TEMPERATURE RANGE**
- **LOGIC COMPATIBLE SUPPLY VOLTAGES**

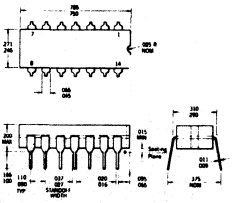
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Input Voltage	±15 V
Voltage Applied to Outputs for High Output State	−0.5 V to +13.2 V
V_{EE} Pin Potential to Ground Pin	−0.5 V to −12 V
Enable Pin Potential to Ground Pin	−0.5 V to +15 V

ORDER INFORMATION

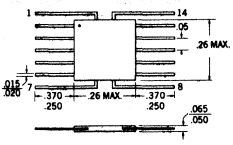
Specify U6A9622XXX for 14 pin Dual In-Line package, U3I9622XXX for 14 pin Flat package where XXX is 51? for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

TYPICAL DUAL IN-LINE PACKAGE
In Accordance With
JEDEC (TO-116) Outline

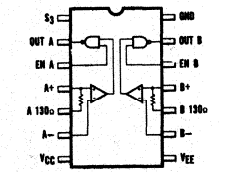


NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

FLAT PACKAGE
TOP VIEW



LOGIC DIAGRAM



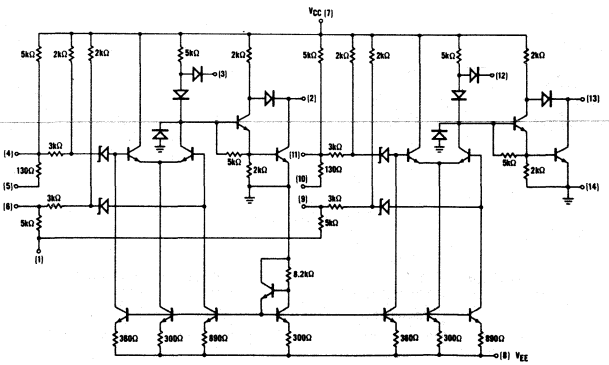
FAIRCHILD
SEMICONDUCTOR

ELECTRICAL CHARACTERISTICS (Temperature Range −55°C to +125°C, V_{CC} = 5.0 V ±10%, V_{EE} = −10 V ±10%) (Part No. UXX962251X)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	−55°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+125°C MIN.	+125°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OL}	Output Low Voltage		0.40		0.25	0.40		0.40	V	V_{CC} = 4.5 V V_{EE} = −11 V *V_{DIFF} = 2.0 V I_{OL} = 12.4 mA
V_{OH}	Output High Voltage	2.8		3.0	3.3		2.9		V	V_{CC} = 4.5 V V_{EE} = −9.0 V *V_{DIFF} = 1.0 V I_{OH} = −0.2 mA
I_{CEX}	Output Leakage Current		50			100		200	μA	V_{CC} = 4.5 V V_{EE} = −11 V *V_{DIFF} = 1.0 V V_{CEX} = 12 V
I_{SC}	Output Shorted Current	−1.3	−3.1	−1.4	−2.15	−3.1	−1.3	−3.1	mA	V_{CC} = 5.0 V V_{EE} = −10 V *V_{DIFF} = 1.0 V V_{SC} = 0 V
$I_{R(ENABLE)}$	Enable Input Leakage Current					2.0		5.0	μA	V_{CC} = 4.5 V V_{EE} = −11 V S_3 = 4.5 V V_R = 4.0 V
$I_{F(ENABLE)}$	Enable Input Forward Current		−1.5		−0.96	−1.5		−1.5	mA	V_{CC} = 5.5 V V_{EE} = −9.0 V S_3 = 0 V V_F = 0 V
$I_{F(+Input)}$	+ Input Forward Current		−2.3		−1.67	−2.1		−2.0	mA	V_{CC} = 5.0 V V_{EE} = −10 V − Input = Gnd V_F = 0 V
$I_{F(-Input)}$	− Input Forward Current		−2.6		−1.87	−2.4		−2.3	mA	V_{CC}, S_3 = 5.0 V V_{EE} = −10 V + Input = Gnd V_F = 0 V
$V_{IL(ENABLE)}$	Input Low Voltage		1.3		1.4	1.0		0.7	V	V_{CC} = 5.0 V ±10% V_{EE} = −10 V ±10%
V_{th}	Differential Input Threshold Voltage	1.0	2.0	1.0	1.5	2.0	1.0	2.0	V	V_{CC} = 5.0 V ±10% V_{EE} = −10 V ±10%
V_{CM}	Common Mode Voltage			−10	±12	+10			V	V_{CC} = 5.0 V V_{EE} = −10 V *V_{DIFF} = 1.0 V or 2.0 V
$R_{130}\Omega$	Terminating Resistance			100	130	175			Ω	
I_{CC}	5 V Supply Current				13.7	22.9			mA	V_{CC} = 5.5 V V_{EE} = −11 V S_3, + Inputs = 5.5 V, − Inputs = 0 V
I_{EE}	−10 V Supply Current				−6.5	−11.1			mA	V_{CC} = 5.5 V V_{EE} = −11 V S_3, + Inputs = 5.5 V, − Inputs = 0 V
t_{pd+}	Turn-off Time				38	50			ns	V_{CC} = 5.0 V V_{EE} = −10 V V_{IN} 0→3 V, R_L = 3.9 kΩ, C_L = 30 pF
t_{pd-}	Turn-on Time				35	50			ns	V_{CC} = 5.0 V V_{EE} = −10 V V_{IN} 0→3.0 V, R_L = 0.39 kΩ, C_L = 30 pF

*V_{DIFF} is a differential input voltage referred from A+ to A− and from B+ to B−.

SCHEMATIC DIAGRAM
(LINE RECEIVER)

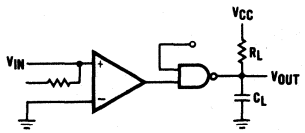


ELECTRICAL CHARACTERISTICS (Temperature Range 0°C to +75°C, $V_{CC} = 5.0\ V \pm 5\%$, $V_{EE} = -10\ V \pm 5\%$) (Part No. UXX962259X)

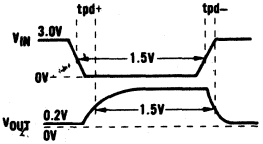
SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+75°C MIN.	+75°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OL}	Output Low Voltage		0.45		0.25	0.45		0.45	V	$V_{CC} = 4.75\ V$ $V_{EE} = -10.5\ V$ *$V_{DIFF} = 2.0\ V$ $I_{OL} = 14.1\ mA$
V_{OH}	Output High Voltage	2.9		3.0	3.3		2.9		V	$V_{CC} = 4.75\ V$ $V_{EE} = -9.5\ V$ *$V_{DIFF} = 1.0\ V$ $I_{OH} = -0.2\ mA$
I_{CEX}	Output Leakage Current		80			100		200	μA	$V_{CC} = 4.75\ V$ $V_{EE} = -10.5\ V$ *$V_{DIFF} = 1.0\ V$ $V_{CEX} = 5.25\ V$
I_{SC}	Output Shorted Current	−1.3	−3.1	−1.4	−2.15	−3.2	−1.3	−3.1	mA	$V_{CC} = 5.0\ V$ $V_{EE} = -10\ V$ *$V_{DIFF} = 1.0\ V$ $V_{SC} = 0\ V$
$I_{R(ENABLE)}$	Enable Input Leakage Current					5		10	μA	$V_{CC} = 4.75\ V$ $V_{EE} = -10.5\ V$ $S_3 = 4.75\ V$ $V_R = 4.0\ V$
$I_{F(ENABLE)}$	Enable Input Forward Current		−1.5		−.96	−1.5		−1.5	mA	$V_{CC} = 5.25\ V$ $V_{EE} = -9.5\ V$ $S_3 = 0\ V$ $V_F = 0\ V$
$I_{F(+Input)}$	+ Input Forward Current		−2.6		−1.67	−2.4		−2.3	mA	$V_{CC} = 5.0\ V$ $V_{EE} = -10\ V$ − Input = Gnd $V_F = 0\ V$
$I_{F(-Input)}$	− Input Forward Current		−2.9		−1.87	−2.7		−2.6	mA	V_{CC}, $S_3 = 5.0\ V$ $V_{EE} = -10\ V$ + Input = Gnd $V_F = 0\ V$
$V_{IL(ENABLE)}$	Input Low Voltage		1.2		1.4	1.0		0.85	V	$V_{CC} = 5.0\ V \pm 5\%$ $V_{EE} = -10\ V \pm 5\%$
V_{th}	Differential Input Threshold Voltage	1.0	2.0	1.0	1.5	2.0	1.0	2.0	V	$V_{CC} = 5.0\ V \pm 5\%$ $V_{EE} = -10\ V \pm 5\%$
V_{CM}	Common Mode Voltage			−7.5	±12	+7.5			V	$V_{CC} = 5.0\ V$ $V_{EE} = -10\ V$ *$V_{DIFF} = 1.0\ V$ or $2.0\ V$
$R_{130}\Omega$	Terminating Resistance			91	130	185			Ω	
I_{CC}	5 V Supply Current				13.7	22.9			mA	$V_{CC} = 5.25\ V$ $V_{EE} = -10.5\ V$ S_3, +Inputs = 5.25 V, −Inputs = 0 V
I_{EE}	−10 V Supply Current				−6.5	−11.1			mA	$V_{CC} = 5.25\ V$ $V_{EE} = -10.5\ V$ S_3, +Inputs = 5.25 V, −Inputs = 0 V
t_{pd+}	Turn-off Time				38	100			ns	$V_{CC} = 5.0\ V$ $V_{EE} = -10\ V$ V_{IN} 0→3.0 V, $R_L = 3.9\ k\Omega$, $C_L = 30\ pF$
t_{pd-}	Turn-on Time				35	100			ns	$V_{CC} = 5.0\ V$ $V_{EE} = -10\ V$ V_{IN} 0→3.0 V, $R_L = 0.39\ k\Omega$, $C_L = 30\ pF$

*V_{DIFF} is a differential input voltage referred from A+ to A−, and from B+ to B−.

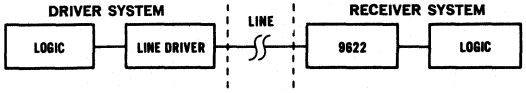
SWITCHING TIME TEST CIRCUIT



WAVEFORMS

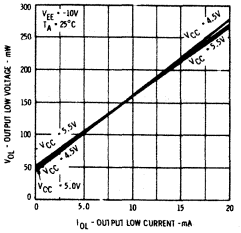


STANDARD USAGE

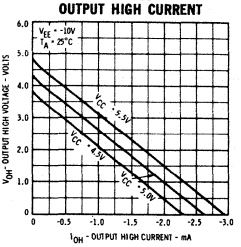


TYPICAL ELECTRICAL CHARACTERISTICS

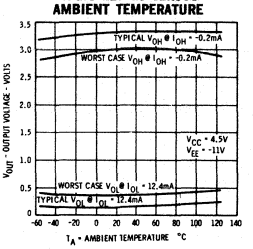
TYPICAL OUTPUT LOW VOLTAGE VERSUS OUTPUT LOW CURRENT



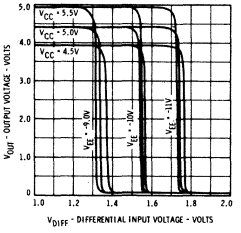
TYPICAL OUTPUT HIGH VOLTAGE VERSUS OUTPUT HIGH CURRENT



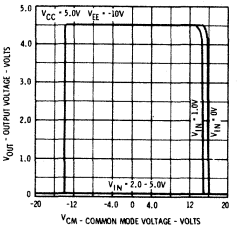
LOGIC LEVELS VERSUS AMBIENT TEMPERATURE



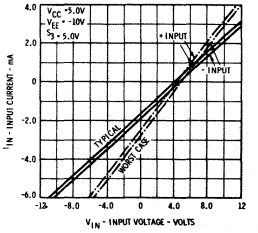
TYPICAL V_{out} - V_{DIFF} TRANSFER CHARACTERISTICS



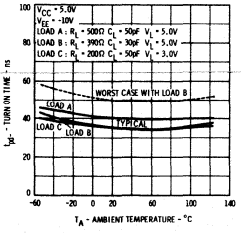
TYPICAL OUTPUT VOLTAGE VERSUS COMMON MODE VOLTAGE



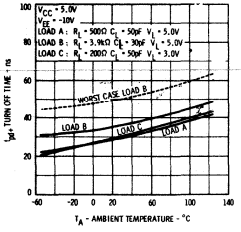
INPUT CURRENT VERSUS INPUT VOLTAGE



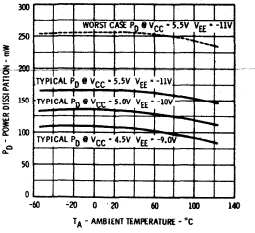
TURN ON TIME VERSUS AMBIENT TEMPERATURE



TURN OFF TIME VERSUS AMBIENT TEMPERATURE



POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



9624 . 9625

DUAL TTuL , MOS INTERFACE ELEMENTS

A FAIRCHILD TRANSISTOR-TRANSISTOR MICROLOGIC INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 9624 is a dual two-input TTμL compatible interface gate specifically designed to drive MOS. The output swing is adjustable and will allow it to be used as a data driver, clock driver or discrete MOS driver. It has an active output for driving medium capacitive loads.

The 9625 is a dual MOS to TTμL level converter. It is designed to convert standard negative MOS logic levels to TTμL levels. The 9625 features a high input impedance which allows preservation of the driving MOS logic level.

Both the 9624 and 9625 are available in the 14-pin ceramic Dual In-Line package and the ¼ x ¼ Flat Pak.

NOTE: The TTμL and MOS devices manufactured by Fairchild Semiconductor are considered as positive TRUE logic (the more positive voltage level is assigned the binary state of "1" or TRUE). Following MIL-STD-806B logic symbol specifications, the 9624 is represented as a NAND gate and the 9625 as a non-inverting buffer. This convention (of assuming MOS as a positive TRUE logic) has not been uniformly accepted by the industry; therefore, it is necessary to note that with negative TRUE MOS logic (the more negative voltage level is assigned the binary state "1" or TRUE), the 9624 acts as an AND gate and the 9625 as an inverter.

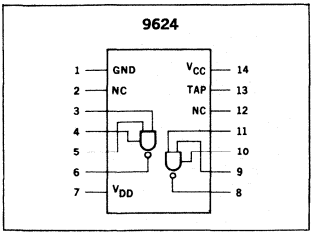
- **TTμL COMPATIBLE INPUTS/OUTPUT**
- **MOS COMPATIBLE OUTPUT/INPUTS**
- **LOW POWER**

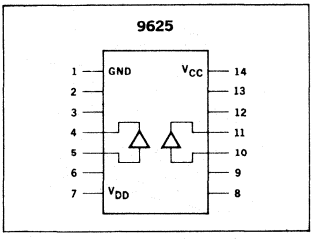
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	V_{DD} to +10 V
Voltage Applied to Outputs for high output state (9624)	V_{DD} to $+V_{CC}$ value
Voltage Applied to Outputs for high output state (9625)	−0.5 V to V_{CC} value
Input Voltage (D.C.) (9624)	−0.5 V to +5.5 V
Input Voltage (D.C.) (9625)	V_{CC} to V_{DD}
V_{DD} Pin Potential to Ground Pin	−30 V to +0.5 V
V_{DD} Pin Potential to Tap Pin (9624)	−30 V to +0.5 V
V_{TAP}	V_{CC} + 0.5 V

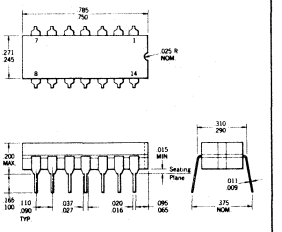
ORDER INFORMATION

Specify U6A9624XXX and U6A9625XXX for 14-pin TO-116 Dual In-Line package or U3I9624XXX and U3I9625XXX for 14-pin Flat Package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.



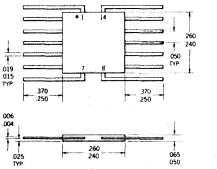


TYPICAL DUAL IN-LINE PACKAGE
In Accordance With
JEDEC (TO-116) Outline



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers.
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams

FLAT PACKAGE
in accordance with JEDEC (TO-86) outline
14 Lead CERPAK



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.26 gram

FAIRCHILD
SEMICONDUCTOR

TABLE I —
ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH1}	Output High Voltage	−1.0		−1.0	−0.5		−1.0		Volts	$V_{CC} = 4.5\ V$, $V_{DD} = -28\ V$, $V_{TAP} = 0\ V$ $I_{OH} = -10\ \mu A$
V_{OH2}	Output High Voltage	+3.5		+3.5	+4.0		+3.5			$V_{CC} = 5.5\ V$, $V_{DD} = -20\ V$, $V_{TAP} = 5.5\ V$ Inputs at threshold voltages (V_{IL}) $I_{OH} = -10\ \mu A$
V_{OL}	Output Low Voltage			See Note 1					Volts	$V_{CC} = 4.5\ V$, $I_{OL} = 10\ mA$, $V_{DD} = -15$ to $-28\ V$ @ V_{IH}, $0 \le V_{TAP} \le V_{CC}$ **SEE NOTE 2**
V_{IH}	Input High Voltage	2.1		1.9			1.7		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.40			−1.25		−1.13	mA	$V_{CC} = 5.5\ V$, $V_F = 0.4\ V$ $V_{DD} = -11$ to $-28\ V$
I_R	Input Leakage Current		2.0			2.0		5.0	μA	$V_{CC} = 5.5\ V$, $V_R = 4.0\ V$ $V_{DD} = -11$ to $-28\ V$
I_{CEX}	Output Leakage Current					50			μA	$V_{CC} = 5.5\ V$, $V_{TAP} = 0\ V$ $V_{DD} = -28\ V$, $V_{OUT} = 0\ V$
I_{SC}	Output Short Circuit Current	−12	−31	−14		−32	−11	−28	mA	$V_{CC} = 4.5\ V$, $V_{TAP} = 0\ V$, $V_{IN} = 0\ V$ $V_{DD} = -11\ V$, $V_{OUT} = -11\ V$
I_{VCC}	V_{CC} Supply Current					6.1			mA	$V_{CC} = 5.5V$, $V_{DD} = -15\ V$, $V_{TAP} = 0\ V$ Inputs Open
I_{MAX}	Max. Current					10			mA	$V_{CC} = 10\ V$, $V_{DD} = -30\ V$, Inputs Open $V_{TAP} = 0\ V$
t_{pd+}	Switching Speed				190	250			ns	$V_{CC} = 5.0\ V$, See Figure 2
t_{pd-}	Switching Speed				50	100			ns	$V_{DD} = -13\ V$, $V_{TAP} = 0\ V$

Note 1: Max = V_{DD} +1.0 V over Temperature Range
Typ = V_{DD} +0.2 V over Temperature Range

Note 2: At no time shall the voltage from V_{DD} to V_{TAP} exceed 30 volts. See absolute maximum ratings on Page 1.

SCHEMATIC DIAGRAM

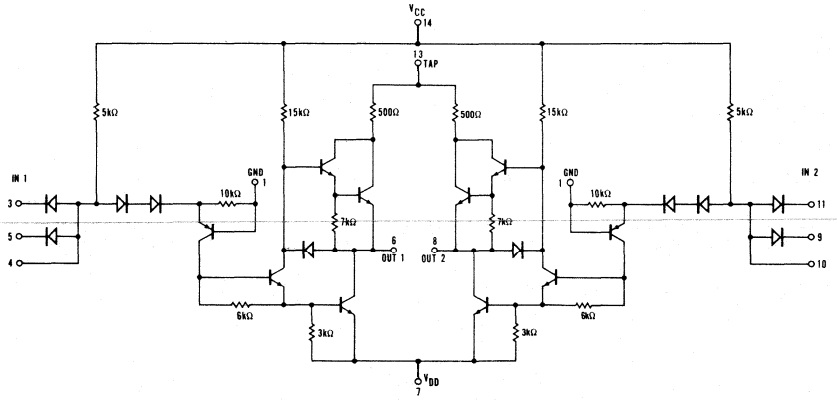


Fig. 1

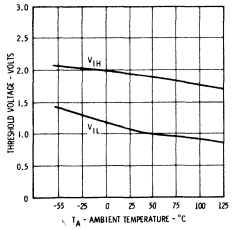
TABLE II —
ELECTRICAL CHARACTERISTICS (T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+75°C MIN.	+75°C MAX.	UNITS	CONDITIONS
V_{OH1}	Output High Voltage	−1.0		−1.0	−0.5		−1.0		Volts	V_{CC} = 4.75 V, V_{DD} = −28 V, V_{TAP} = 0 V I_{OH} = −10 μA
V_{OH2}	Output High Voltage	+3.25		+3.25	+3.75		+3.25		Volts	V_{CC} = 5.25 V, V_{DD} = −20 V, V_{TAP} = 5.25 V I_{OH} = −10 μA Inputs at threshold voltages (V_{IL} or V_{IH})
V_{OL}	Output Low Voltage			See Note 1					Volts	V_{CC} = 4.5 V, I_{OL} = 10 mA, V_{DD} = −11 to −28 V @ 0 ≤ V_{TAP} ≤ V_{CC} **SEE NOTE 2**
V_{IH}	Input High Voltage	2.0		1.9			1.8		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.2			1.1		0.95	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.32			−1.25		−1.20	mA	V_{CC} = 5.25 V, V_F = 0.45 V
I_R	Input Leakage Current		5.0			5.0		10	μA	V_{CC} = 5.25 V, V_R = 4.5 V
I_{CEX}	Output Leakage Current					100			μA	V_{CC} = 5.25 V, V_{TAP} = 0 V V_{DD} = −28 V, V_{OUT} = 0 V
I_{SC}	Output Short Circuit Current	−12	−31	−14		−32	−12	−31	mA	V_{CC} = 4.75 V, V_{TAP} = 0 V, V_{IN} = 0 V V_{DD} = −11 V, V_{OUT} = −11 V
I_{VCC}	V_{CC} Supply Current					6.1			mA	V_{CC} = 5.25 V, V_{DD} = −15 V, V_{TAP} = 0 V Input Open
I_{MAX}	Max. Current					10			mA	V_{CC} = 10 V, V_{DD} = −30 V, V_{TAP} = 0 V Input Open
t_{pd+}	Switching Speed				190	250			ns	V_{CC} = 5.0 V, See Figure 2
t_{pd-}	Switching Speed				50	100			ns	V_{DD} = −13 V, V_{TAP} = 0 V

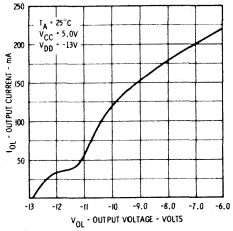
Note 1: Max = V_{DD} +1.0 V over Temperature Range
Typ = V_{DD} +0.2 V over Temperature Range
Note 2: At no time shall the voltage from V_{DD} to V_{TAP} exceed 30 volts. See absolute maximum ratings on Page 1.

ELECTRICAL CHARACTERISTICS • 9624

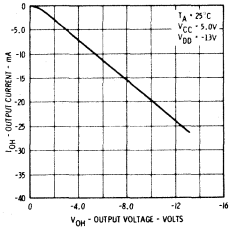
THRESHOLD VOLTAGE VERSUS AMBIENT TEMPERATURE



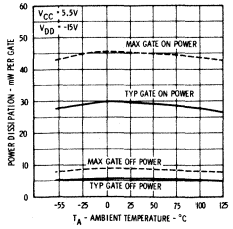
TYPICAL OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (LOW STATE)



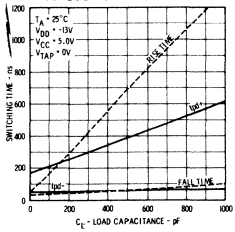
TYPICAL OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (HIGH STATE)



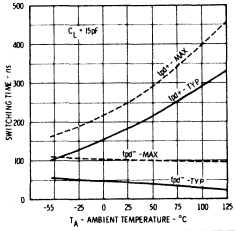
POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



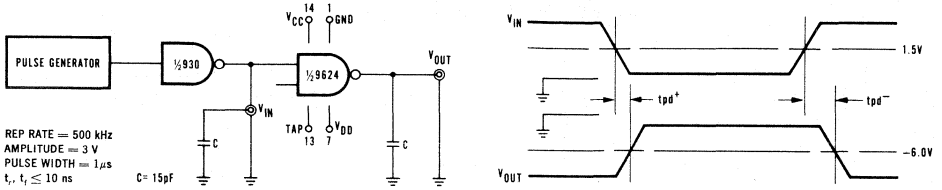
TYPICAL SWITCHING TIME VERSUS LOAD CAPACITANCE



SWITCHING TIME VERSUS AMBIENT TEMPERATURE



SWITCHING TIME TEST CIRCUIT AND WAVEFORMS
9624



TESTS	CONDITIONS			
	T_A (°C)	V_{CC} (Volts)	V_{DD} (Volts)	Tap Voltage
t_{pd}^+, t_{pd}^-	25	5.0	−13	0

Fig. 2

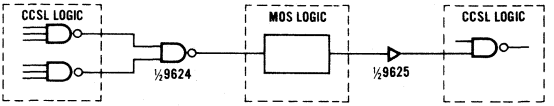
LOADING RULES:



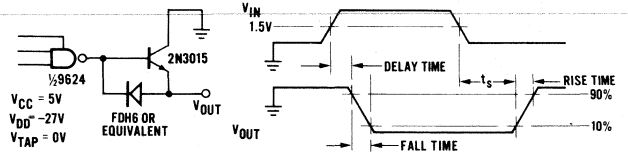
*The extender pin allows the number of inputs to be extended by adding diodes or the DTμL 933 extender.

**Fan out into MOS is limited only by MOS leakage currents.

APPLICATION:



CLOCK DRIVING (using a high capacitance drive scheme)



TYPICAL SWITCHING TIMES VERSUS LOAD CAPACITANCE

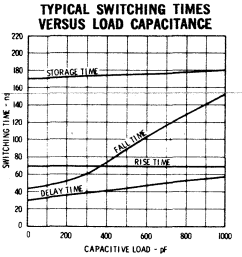


TABLE III —
ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	CHARACTERISTICS	LIMITS						UNITS	CONDITIONS
		−55°C		+25°C			+125°C		
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN. MAX.		
V_{OH}	Output High Voltage	2.5		2.6			2.5	Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -60\ \mu A$ $V_{DD} = -11\ V$ Inputs at threshold voltages (V_{IH})
V_{OL}	Output Low Voltage		0.5			0.5	0.5	Volts	$V_{CC} = 5.5\ V$, $I_{OL} = 1.5\ mA$ $V_{CC} = 4.5\ V$, $I_{OL} = 1.2\ mA$ $V_{DD} = -11\ V$ Inputs at threshold voltages (V_{IL})
V_{IH}	Input High Voltage	−3.0				−3.0	−3.0	Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		−9.0			−9.0	−9.0	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		210			210	210	μA	$V_{CC} = 5.0\ V$, $V_F = -3.0\ V$, $V_{DD} = -13\ V$
I_{CEX}	Output Leakage Current					50		μA	$V_{CC} = V_{CEX} = 4.5\ V$, $V_{DD} = -13\ V$
I_{VCCL}	Supply Current					4.8		mA	$V_{CC} = 5.5\ V$, $V_{DD} = -15\ V$, $V_{IN} = -10\ V$
I_{VCCH}	Supply Current					2.1			$V_{CC} = 5.5\ V$, $V_{DD} = -15\ V$, $V_{IN} = 0\ V$
I_{VDD}	V_{DD} Supply Current					−9.0		mA	$V_{CC} = 5.5\ V$, $V_{DD} = -15\ V$ Input open or gnd
I_{MAX}	Max. V_{DD} Supply Current					−25		mA	$V_{CC} = 8.0\ V$, $V_{DD} = -20\ V$, $V_{IN} = 0\ V$
t_{pd+}	Switching Speed				55	100		ns	$V_{CC} = 5.0\ V$, $V_{DD} = -13\ V$ See Figure 4
t_{pd-}	Switching Speed				90	150		ns	

SCHEMATIC DIAGRAM

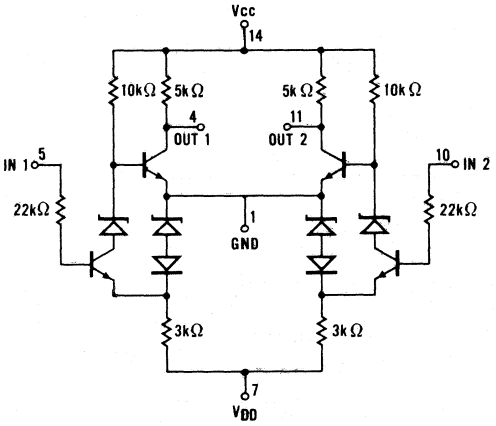
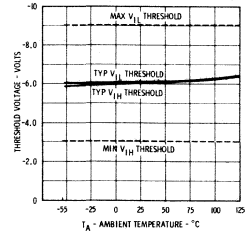


Fig. 3

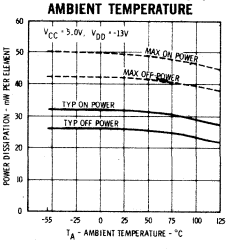
TABLE IV —
ELECTRICAL CHARACTERISTICS (T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	MAX.	LIMITS +25°C MIN.	TYP.	MAX.	LIMITS +75°C MIN.	MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.5		2.6			2.5		Volts	V_{CC} = 4.75 V, I_{OH} = −60 μA V_{DD} = −11 V Inputs at threshold voltages (V_{IH})
V_{OL}	Output Low Voltage		0.5			0.5		0.5	Volts	V_{CC} = 5.25 V, I_{OL} = 1.52 mA V_{CC} = 4.75 V, I_{OL} = 1.33 mA Inputs at threshold voltages (V_{IL})
V_{IH}	Input High Voltage	−3.0				−3.0	−3.0		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		−9.0			−9.0		−9.0	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current	210				210	210		μA	V_{CC} = 5.0 V, V_F = −3.0 V, V_{DD} = −13 V
I_{CEX}	Output Leakage Current					100			μA	V_{CC} = V_{CEX} = 4.75 V, V_{DD} = −13 V
I_{VCCL}	Supply Current					4.8			mA	V_{CC} = 5.25 V, V_{DD} = −15 V, V_{IN} = −10 V
I_{VCCH}	Supply Current					2.1			mA	V_{CC} = 5.25 V, V_{DD} = −15 V, V_{IN} = 0 V
I_{VDD}	V_{DD} Supply Current					−9.0			mA	V_{CC} = 5.5 V, V_{DD} = −15 V Input open or gnd
I_{MAX}	Max. V_{DD} Supply Current					−25			mA	V_{CC} = 8.0 V, V_{DD} = −20 V, V_{IN} = 0 V
t_{pd+}	Switching Speed				55	100			ns	V_{CC} = 5.0 V, V_{DD} = −13 V See Figure 4
t_{pd-}	Switching Speed				90	150			ns	

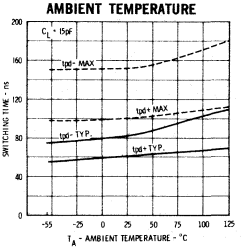
THRESHOLD VOLTAGE VERSUS AMBIENT TEMPERATURE



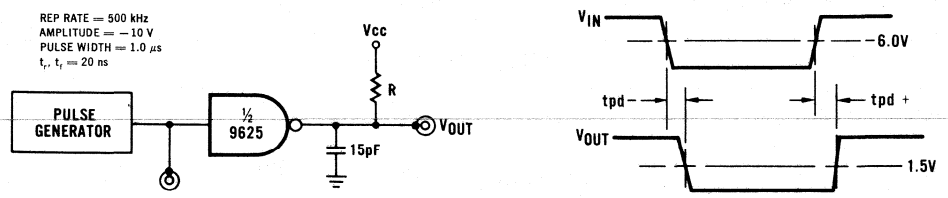
POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



SWITCHING TIME VERSUS AMBIENT TEMPERATURE



SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



TESTS	CONDITIONS T_A (°C)	V_{CC} (Volts)	V_{DD} (Volts)	R (kΩ)
t_{pd}^+, t_{pd}^-	25	5.0	−13	3.75

Fig. 4

LUMINANCE COMBINATION TBA500

CHROMINANCE COMBINATION TBA510

LUMINANCE COMBINATION

The TBA500 is an integrated luminance amplifier circuit for colour television receivers incorporating delay line matching stages and a d.c. control which maintains a constant black level over its range of operation. A beam current limiting facility is provided, reducing the picture contrast and then brightness.
Horizontal and vertical blanking pulses may be applied.
An a.g.c. detector is incorporated; this circuit can, however, also be used as a gated luminance black level clamp.

TYPICAL DATA				
Supply voltage	V_{12-16}	nom.	12	V
Input signal (peak to peak value)	$V_{2-16(p-p)}$	typ.	2	V
Output signal (peak to peak value)	$V_{10-16(p-p)}$	typ.	4	V
Linearity at maximum contrast	m	>	0.9	

PACKAGE OUTLINE: 16 lead dual in-line

CHROMINANCE COMBINATION

The TBA510 is an integrated chrominance amplifier circuit for colour television receivers incorporating a variable gain a.c.c. chroma amplifier circuit, a d.c. control for chroma saturation which can be ganged to the receiver contrast control, chroma blanking and burst gating functions, a burst output stage, a colour killer stage and a P.A.L. delay line driver stage.

TYPICAL DATA				
Supply voltage	V_{1-16}	nom.	12	V
Input signal (colour bars) peak-to-peak value	$V_{4-16(p-p)}$	nom.	150	mV
Output signal (peak-to-peak value)	$V_{9-16(p-p)}$	typ.	1	V
Burst signal output (peak-to-peak value)	$V_{12-16(p-p)}$	typ.	1	V

PACKAGE OUTLINE: 16 lead dual in-line

FAIRCHILD
SEMICONDUCTOR

COLOUR DEMODULATOR TBA520

R.G.B. MATRIX PRE-AMPLIFIER TBA530

COLOUR DEMODULATOR

The TBA520 is an integrated colour demodulator circuit for colour television receivers, incorporating two active synchronous demodulators for R-Y and B-Y chrominance signals, a matrix (producing the G-Y colour difference signal), P.A.L. phase switch and flip-flop. It is suitable for d.c.-coupled drive to the picture tube when associated with the matrix integrated circuit (TBA530) and R.G.B. output stages.

TYPICAL DATA				
Supply voltage (stabilised)	V_{6-16}	nom.	12	V
Ambient temperature	T_{amb}		25	°C
Gain of R-Y demodulator	G_{13-4}	typ.	7	
Gain of B-Y demodulator	G_{9-7}	typ.	12.5	
Impedance of chrominance inputs	$\lvert Z_{9-16}\rvert$	typ.	1 kΩ in	
	$\lvert Z_{13-16}\rvert$	parallel with 10 pF		
Impedance of colour-difference signal outputs	$\lvert Z_{4-16}\rvert$	typ.	2.7	kΩ
	$\lvert Z_{7-16}\rvert$	typ.	2.7	kΩ
	$\lvert Z_{5-16}\rvert$	typ.	2.7	kΩ

PACKAGE OUTLINE: 16 lead dual in-line

R.G.B. MATRIX PRE-AMPLIFIER

The TBA530 is an integrated R.G.B. matrix pre-amplifier for colour television receivers incorporating a matrix pre-amplifier for R.G.B. cathode or grid drive of the picture tube without clamping circuits. The chip lay-out has been designed to ensure tight thermal coupling between all the transistors in each channel to minimise and equalise thermal drifts between channels. Also, each channel follows an identical lay-out to ensure equal frequency behaviour of the three channels.

This integrated circuit has been designed to be driven from the TBA520 synchronous demodulator integrated circuit.

TYPICAL DATA				
Supply voltage	V_{8-6}	nom.	12	V
Ambient temperature	T_{amb}		25	°C
Gain of luminance and colour-difference channels	G	typ.	100	
Total current consumption	I_{tot}	typ.	30	mA

PACKAGE OUTLINE: 16 lead dual in-line

REFERENCE COMBINATION TBA540

REFERENCE COMBINATION

The TBA540 is an integrated reference oscillator circuit for colour television receivers incorporating an automatic phase and amplitude controlled oscillator employing a quartz crystal, together with a half-line frequency synchronous demodulator circuit. The latter compares the phases and amplitude of the swinging burst ripple and the P.A.L. flip-flop waveform, and generates appropriate a.c.c., colour killer and identification signals. The use of synchronous demodulation for these functions permits a high standard of noise immunity.

TYPICAL DATA

Supply voltage	V_{3-16}	nom.	12	V
Total current drain	I_3	typ.	33	mA
R-Y reference signal output peak-to-peak value	$V_{4-16(p-p)}$	typ.	1.5	V
Colour killer output: colour on	V_{7-16}	typ.	12	V
colour off	V_{7-16}	<	250	mV
A.C.C. output voltage range				
at correct phase of P.A.L. switch	V_{9-16}		+4 to + 0.2	V
at incorrect phase of P.A.L switch	V_{9-16}		+4 to +10	V

PACKAGE OUTLINE: 16 lead dual in-line

LUMINANCE AND CHROMINANCE CONTROL COMBINATION TBA560

LUMINANCE & CHROMINANCE CONTROL COMBINATION

The TBA560 is a monolithic integrated circuit used in the decoding system of colour television receivers. The circuit consists of a chrominance amplifier.

The luminance amplifier input is matched to the luminance delay line and performs the following functions:

d.c. contrast control * brightness control * black level clamping * blanking * beam current limiting.

The chrominance amplifier comprises:

gain-controlled amplifier * chrominance gain control tracked with contrast control * separate d.c. saturation control * P.A.L. delay line driver * burst gate * colour killer.

QUICK REFERENCE DATA

Supply voltage	V_{11-16}	nom.	12	V
Supply current	I_{11}	nom.	24	mA
Luminance signal input current	$I_{3(p-p)}$	typ.	1.5	mA
Chrominance input signal	$V_{1-15(p-p)}$	$>$	4	mV
		$<$	80	mV
Luminance output signal at nominal contract setting	$V_{5-16(p-p)}$	typ.	3	V[1])
Chrominance output signal at nominal contrast and saturation setting	$V_{9-16(p-p)}$	typ.	2	V[1])
Contrast control range		$\geqslant$	20	dB
Saturation control range		$\geqslant$	20	dB
Burst output (closed a.c.c. loop)	$V_{7-16/p-p)}$	typ.	1	V

[1]) Nominal setting: maximum contrast or saturation minus 6 dB

PACKAGE OUTLINE: 16 lead dual in-line

9644
DUAL HIGH-VOLTAGE, HIGH CURRENT DRIVER
A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 9644 is a Dual 4-Input NAND Gate whose output can sink 500 mA in the low state, and maintain 30 volts in the high state. The outputs are uncommitted collectors in a Darlington configuration which have typical saturation voltages of 0.8 volts at low currents and 1.2 volts at 500 mA. The inputs are CCSL Compatible and feature input clamp diodes. The input fan-in requirement is typically ½ a normal DTμL Unit Load. An input strobe common to both gates is provided, and an expander input node on each gate is available for input diode expansion. Separate ground pins are provided for each gate to minimize ground pin offset voltages at high current levels.

- **500 mA CURRENT SINKING CAPABILITY**
- **OUTPUT VOLTAGES UP TO 30 VOLTS**
- **LOW AVERAGE POWER, TYPICALLY 30 mW PER GATE**
- **HIGH SPEED, TYPICALLY 50 ns DELAY TIMES**
- **CCSL COMPATIBLE INPUTS**
- **INPUT CLAMP DIODES**
- **LOW FAN-IN LOADING REQUIREMENTS**
- **COMMON STROBE INPUT**
- **EXPANDER NODE FOR INPUT DIODE EXPANSION**

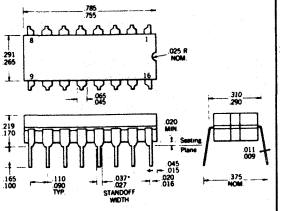
ABSOLUTE MAXIMUM RATING

Storage Temperature		−65°C to +175°C
Temperature (Ambient) Under Bias		−55°C to +125°C
V_{CC} Pin Potential to Ground Pin		−0.5 V to +8.0 V
Input Voltages (D.C.)		−0.5 V to +5.5 V
Voltage Applied to Outputs (Output High)	See Safe Area	−0.5 V to +30 V
Output Current (D.C.) (Output Low)	Curves Page 3	640 mA

ORDER INFORMATION:

Specify U7B9644XXX for 16 pin Dual In-Line package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to 75°C temperature range.

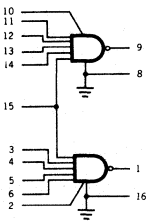
PHYSICAL DIMENSIONS
16 Lead MSI Dual In-Line



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for a conventional .020 inch diameter Lead
Leads are tin plated Kovar
Package weight is 2.2 grams
*The $^{.037}_{.027}$ dimension does not apply to the corner leads

Fig. 1

LOGIC DIAGRAM



$V_{CC} = 7$

Fig. 2

FAIRCHILD
SEMICONDUCTOR

FAIRCHILD INTEGRATED CIRCUIT 9644

ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

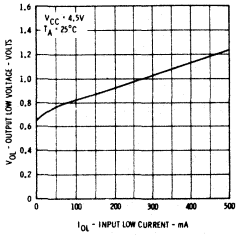
SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OL}	Output Low Voltage		1.7		1.25	1.5		1.5	Volts	$V_{CC} = 4.5\ V$, $I_{OL} = 500\ mA$, Inputs = V_{IH}
					0.8	1.0			Volts	$V_{CC} = 5.0\ V$, $I_{OL} = 100\ mA$, Inputs = V_{IH}
I_{CEX}	Output Leakage Current				<1.0	200		500	μA	$V_{CC} = 5.5\ V$, $V_{CEX} = 30\ V$, $V_{IN} = V_{IL}$
I_R	Input Reverse Current				<1.0	2.0		5.0	μA	$V_{CC} = 5.5\ V$, $V_{IN} = 4.5\ V$, Other Inputs = Gnd
I_F	Input Forward Current		−0.75		−0.18	−0.75		−0.75	mA	$V_{CC} = 5.5\ V$, $V_{IN} = 0.4\ V$
I_{RS}	Strobe Reverse Current				<1.0	4.0		10	μA	$V_{CC} = 5.5\ V$, $V_{IN} = 4.5\ V$, Other Inputs = Gnd
I_{FS}	Strobe Forward Current		−1.5		−0.36	−1.5		−1.5	mA	$V_{CC} = 5.5\ V$, $V_{IN} = 0.4\ V$
I_{FX}	Expander Node Forward Current				−2.68	−3.9			mA	$V_{CC} = 5.5\ V$, $V_{IN} = 0.4\ V$
I_{CC}	V_{CC} Current (Gate On)				20.4	30			mA	$V_{CC} = 5.5\ V$, Inputs = Open
I_{MAX}	Max. V_{CC} Rating				7.0	12			mA	$V_{CC} = 8.0\ V$, Inputs = Gnd
V_{F3}	Input Clamp Diode Voltage				−0.8	−1.5			Volts	$V_{CC} = 4.5\ V$, $I_{IN} = -10\ mA$, Other Inputs = Open
V_{IL}	Input Low Voltage		1.3		1.1	1.0		0.7	Volts	Guaranteed Input Low Threshold
V_{IH}	Input High Voltage	2.3		2.1	1.7		1.9		Volts	Guaranteed Input High Threshold
t_{pd+}	Propagation Delay				50	100			ns	$V_{CC} = 5.0\ V$, $C_L = 40\ pF$,
t_{pd-}	Propagation Delay				50	100			ns	$R_L = 75\ \Omega$ to $+30\ V$ (See Fig. 3)

ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0 \pm 5\%$)

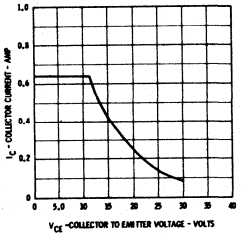
SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OL}	Output Low Voltage		1.6		1.25	1.5		1.5	Volts	$V_{CC} = 4.75\ V$, $I_{OL} = 500\ mA$, Inputs = V_{IH}
					0.8	1.0			Volts	$V_{CC} = 5.0\ V$, $I_{OL} = 100\ mA$, Inputs = V_{IH}
I_{CEX}	Output Leakage Current				<1.0	250		500	μA	$V_{CC} = 5.25\ V$, $V_{CEX} = 30\ V$, $V_{IN} = V_{IL}$
I_R	Input Reverse Current				<1.0	5.0		10	μA	$V_{CC} = 5.25\ V$, $V_{IN} = 4.5\ V$, Other Inputs = Gnd
I_F	Input Forward Current		−0.75		−0.18	−0.75		−0.75	mA	$V_{CC} = 5.25\ V$, $V_{IN} = 0.45\ V$
I_{RS}	Strobe Reverse Current				<1.0	10		20	μA	$V_{CC} = 5.25\ V$, $V_{IN} = 4.5\ V$, Other Inputs = Gnd
I_{FS}	Strobe Forward Current		−1.5		−0.36	−1.5		−1.5	mA	$V_{CC} = 5.25\ V$, $V_{IN} = 0.45\ V$
I_{FX}	Expander Node Forward Current				−2.68	−3.9			mA	$V_{CC} = 5.25\ V$, $V_{IN} = 0.45\ V$
I_{CC}	V_{CC} Current (Gate On)				20.4	30			mA	$V_{CC} = 5.25\ V$, Inputs = Open
I_{MAX}	Max. V_{CC} Rating				7.0	12.8			mA	$V_{CC} = 8.0\ V$, Inputs = Gnd
V_{F3}	Input Clamp Diode Voltage				−0.8	−1.5			Volts	$V_{CC} = 4.75\ V$, $I_{IN} = -10\ mA$, Other Inputs = Open
V_{IL}	Input Low Voltage		0.85		1.1	0.85		0.75	Volts	Guaranteed Input Low Threshold
V_{IH}	Input High Voltage	2.2		2.1	1.7		2.1		Volts	Guaranteed Input High Threshold
t_{pd+}	Propagation Delay				50	200			ns	$V_{CC} = 5.0\ V$, $C_L = 40\ pF$,
t_{pd-}	Propagation Delay				50	200			ns	$R_L = 75\ \Omega$ to $+30\ V$ (See Fig. 3)

ELECTRICAL CHARACTERISTICS

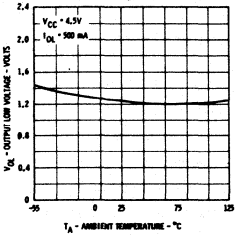
OUTPUT LOW VOLTAGE VERSUS INPUT LOW CURRENT



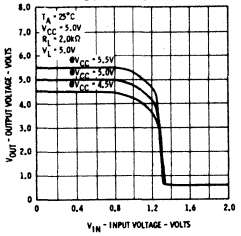
SAFE AREA CURVE



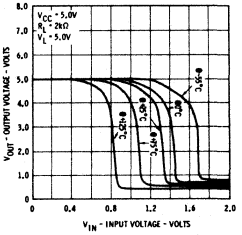
OUTPUT LOW VOLTAGE VERSUS AMBIENT TEMPERATURE



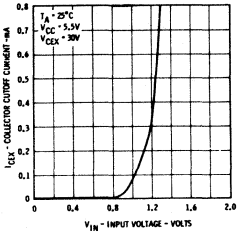
OUTPUT VOLTAGE VERSUS INPUT VOLTAGE AND SUPPLY VOLTAGE



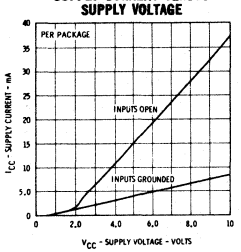
OUTPUT VOLTAGE VERSUS INPUT VOLTAGE AND TEMPERATURE



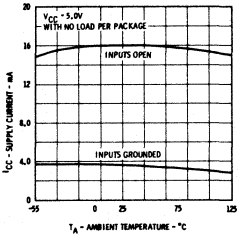
COLLECTOR CUTOFF CURRENT VERSUS INPUT VOLTAGE



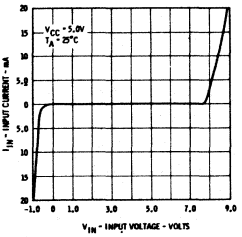
SUPPLY CURRENT VERSUS SUPPLY VOLTAGE



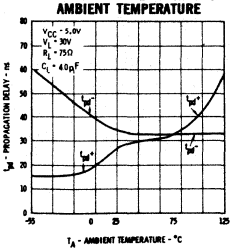
SUPPLY CURRENT VERSUS AMBIENT TEMPERATURE



INPUT CURRENT VERSUS INPUT VOLTAGE



PROPAGATION DELAY VERSUS AMBIENT TEMPERATURE



CURRENT SINKING DERATING CURVE

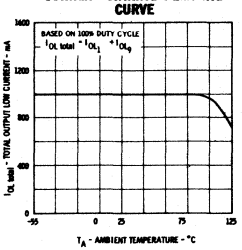
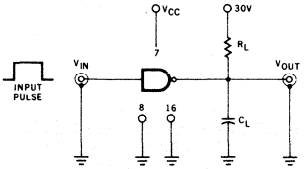
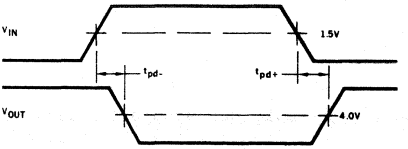


Fig. 3 — SWITCHING CIRCUIT AND WAVEFORMS

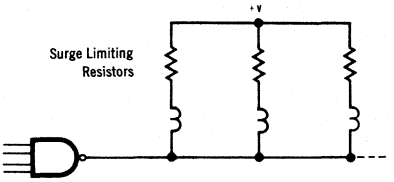




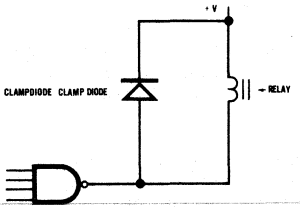
Input Requirements:

Frequency	≃ 100 kHz
Amplitude	3 ±0.1 V
Pulse Width	≃ 500 ns
Rise Time	≤ 10 ns
Fall Time	≤ 10 ns

$R_L = 75\ \Omega$
$C_L = 40$ pF



$I_{OL} \leq 500\ mA = N \bullet I_{Bulb} + N \bullet I_{Surge}$



The clamp diode must be capable of keeping the 9644 within its SAFE AREA. The clamp diode must handle all the coil current.

+V	$R_{COIL\ (min)}$	I_{max}
28 V	280 Ω	100 mA
24 V	160 Ω	150 mA
18 V	57 Ω	300 mA
15 V	35 Ω	400 mA
12 V	22 Ω	500 mA
6 V	10 Ω	500 mA
5 V	8 Ω	500 mA

APPLICATIONS BRIEF 44

GATED PULSE RATE FUNCTION MULTIPLIER

A simple but accurate scheme for multiplying two process control signals is described in this application brief. The two input signals must be in the form of variable frequency pulse trains. Such pulse trains are obtained, for example, as outputs from certain transducers measuring rotational speed (magnetic or photoelectric pick-ups), flow (turbine flow meters), acceleration (pulsed rebalance accelerometers), and others.

Figure 1 shows the basic scheme in block diagram form. One of the two pulse trains is used to trigger an accurate one-shot. The output of this one-shot opens a gate in the path of the second pulse train for a fixed time interval. The frequency of the second pulse train must be many times that of the first one. The number of pulses per time permitted to pass is then proportional to the product of the two applied signals.

The accuracy of this multiplier is primarily determined by the relationship between the highest pulse rate $f_{1\ max}$ of the "gate opening" pulse train and the lowest pulse rate $f_{2\ min}$ of the pulse train passing through the gate. The mathematical relationship is given by:

$$\%\text{ Accuracy} = \frac{f_{1\ max}}{f_{2\ min}} 100$$

The frequency of $f_{1\ max}$ should be chosen around 30 to 50 Hz fixing the minimum frequency for f_2 at 30 to 50 kHz for an accuracy of about .1%.

If instead of a pulse train output an analog output is desired, another one-shot with accurate pulse height output and a filter should be added (see Figure 1). The purpose of the low pass filter is to average the input from the one-shot to produce an analog D.C. level.

A possible circuit for one-shot number one is shown in Figure 2. The capacitor C has to be chose to fit the particular application as far as pulse duration is concerned. For one-shot number two, the pulse height has to be kept at a definite voltage level. This is done by the circuit of Figure 3.

FAIRCHILD
SEMICONDUCTOR

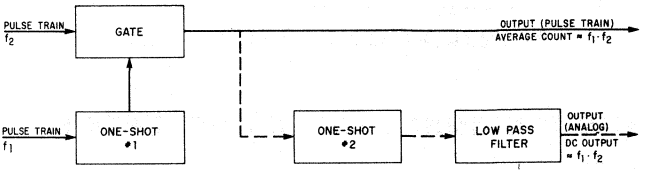


FIG. 1 BLOCK DIAGRAM OF GATED PULSE RATE FUNCTION MULTIPLIER

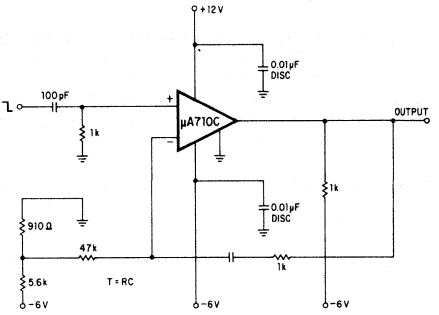


FIG. 2 ONE-SHOT #1

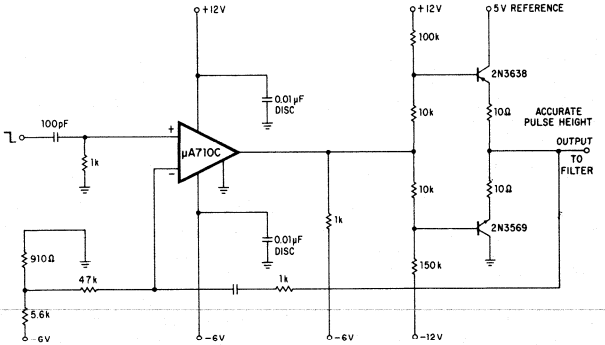


FIG. 3 ONE-SHOT #2

APPLICATIONS BRIEF 50

MULTI-SIGNAL PROCESSING CIRCUIT

The circuit described in this note is capable of producing an output proportional to the ratio of two variable analog inputs multiplied by a variable frequency pulse train. Since any one of three variables can be held constant, this circuit exhibits great flexibility. It can be applied to such areas as process control systems, analog computers, instrumentation, and others.

In mathematical form, the circuit produces an output signal given by the equation:

$$z = k \frac{x_1}{x_2} y$$

where x_1 = analog input 1

x_2 = analog input 2

y = pulse train (frequency) input

k = constant

z = output

The output can be obtained as a pulse width modulated signal when the output of the basic unit shown in Figure 1 is used directly. An analog output signal is obtained by adding an accurate pulse height limiter and low-pass filter as shown in Figure 2.

Description of Basic Unit:

The basic unit as shown in Figure 1 consists of three integrated circuits and a few discrete components. A μA709 is connected as an integrator. The capacitor of this integrator can be discharged through the 2N4343, thus, resetting the integrator.

The operation of the circuit can best be described by assuming that the capacitor C has just been discharged and the 2N4343 has returned to its off-state (high impedance between source and drain). If at that instant a positive d.c. signal $x_1(t)$ is present at the input of the integrator, the output voltage will change as a function of time, as shown in Figure 3. (For simplicity, we assumed that signal $x_1(t)$ does not change during this process.) The output voltage is a ramp function with a slope given by the values of R_1, C_1, and $x_1(0)$, which is the value of $x_1(t)$ at $t = 0$ and assumed constant.

FAIRCHILD
SEMICONDUCTOR

$$V_{OUT}(t) = \frac{-1}{R_1C_1} \int x_1(t)\, dt = \frac{-x_{1(0)}}{R_1C_1}\, t \text{ for } t > 0$$

The output voltage $V_{OUT}(t)$ is allowed to increase negatively until it reaches a value which is equal to the value of the negative analog input signal $x_2(t)$. When that happens (time T in Figure 3), the μA710 comparator will change its output state. This sets an R-S flip-flop, changing the output state. By using the appropriate flip-flop output, this change turns on transistor 2N3567 which will essentially ground the gate on the p channel junction FET. The source to drain impedance will therefore drop and short the capacitor of the integrator. That state of the circuit will remain in effect until a pulse at input y resets the R-S flip-flop. The flip-flop will then turn off the 2N3567 transistor and remove the short from capacitor C_1 by pulling the gate of the 2N4343 junction FET up. Now the cycle starts over again.

From Figure 3, it is seen that the time T is determined by the following relationship:

$$T = \frac{x_2\, R_1C_1}{x_1(0)}$$

Output z of the flip-flop produces a pulse of width T for every pulse arriving at input y. The pulse width is, therefore, proportional to the ratio of x_2 to x_1. Since the pulse height is constant, the area of each pulse is proportional to this ratio. Since the number of pulses produced is equal to the number of pulses applied in the pulse train y, the average value of the pulse train function z at the output of this basic unit is proportional to the ratio x_2 to x_1 times the frequency of the input pulse train y. NOTE: The time between pulses at y must always be greater than T.

Typical Uses for the Multi-Signal Processing Circuit:

Since one of the inputs to the circuit is a variable frequency pulse train, this unit is ideally suited for use in process control systems where one of the variables is rotational or translational speed. By employing a photo electric or magnetic pick-up, speed is converted to a pulse train.

The other two input variables should be analog and, therefore, can be taken from a large number of transducers with analog outputs, such as pressure transducers, temperature sensors, humidity sensors, torque transducers, and many others. As a typical example, we could consider an industrial weigh feeder system. The rate at which material is moved on a conveyer belt is obtained by multiplying belt velocity by the belt load.

As another example, we can cite a system in which the power of a rotating shaft has to be obtained for feedback or monitoring. Again, the product of a pulse train (shaft speed) and an analog signal (output of torque transducer) has to be formed, which can easily be performed by the unit described in this note.

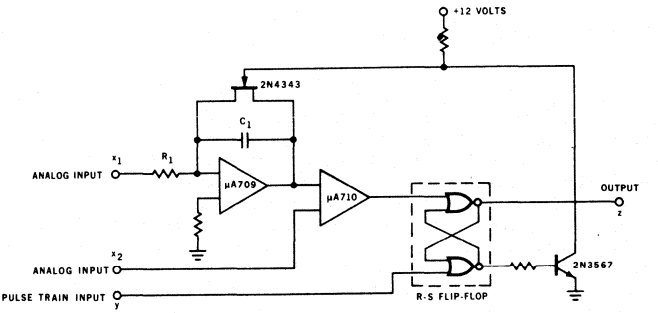


FIG. 1. BASIC UNIT OF MULTI-SIGNAL PROCESSING CIRCUIT PRODUCING PULSE-WIDTH MODULATED OUTPUT SIGNAL Z.

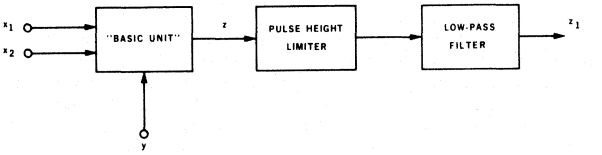


FIG. 2. MULTI-SIGNAL PROCESSING CIRCUIT PRODUCING ANALOG OUTPUT SIGNAL Z_1.

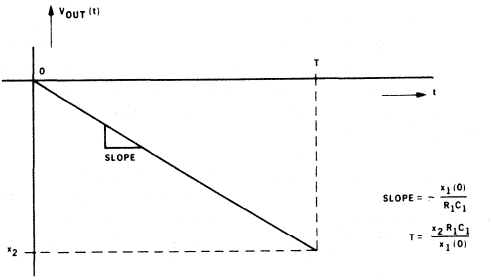


FIG. 3. OUTPUT VOLTAGE OF INTEGRATOR AS A FUNCTION OF TIME.

APPLICATIONS BRIEF 51

ANALOG TO PULSE WIDTH CONVERTOR

INTRODUCTION:

The salient features of the analog to pulse width converter described in this note are its simplicity and accuracy. Only one integrated circuit, μA709, and a few discrete elements are used, yet accuracy and temperature stability are very good. The circuit can be used to change analog signals from sensors and transducers into a pulse width or time ratio modulated square wave. Such a signal change is desirable to avoid the drawbacks of analog signal transmission and signal conditioning in industrial process control systems or in similar situations.

DESCRIPTION OF CIRCUIT:

The basic circuit diagram of the converter is shown in Figure 1. The analog voltage signal V_{IN} is applied to the inverting input (pin 2) of a μA709 operational amplifier through resistor R_{IN}. Capacitor C, which is connected from pin 2 to ground, will be charged and discharged through resistor R_{IN} and the feed-back resistor R_F. There is also feed-back from the zener-limited output terminal applied to the non-inverting input (pin 3) of the μA709 through resistors R_1 and R_2. R_3 connected in series with the output of the μA709 will keep the output current within proper limits. A zener regulated zeroing network connected to the inverting input of the operational amplifier completes the circuit of the converter.

PRINCIPLE OF OPERATION:

Let us assume that a positive analog signal is applied to the input of the converter and that the output voltage is in its positive state. (As will be shown, there are only two output voltage levels possible - one positive and one negative.) Under these conditions, capacitor C will be charged positively with respect to ground through resistor R_{IN} by the applied input voltage V_{IN} and through resistor R_F by the output voltage V_{OUT}. (We ignore the current from the zeroing network for the moment.) As the voltage on the capacitor is rising and finally becomes a small amount larger than the voltage at the non-inverting input (pin 3), the output of the operational amplifier will go negative. This small negative output is immediately fed back to the non-inverting input and, therefore, "reinforced" causing an abrupt change from the positive state to the negative state of V_{OUT}. With V_{OUT} at its negative limit, the capacitor C is discharged through R_F faster than it is charged through R_{IN} reducing its voltage. When the capacitor voltage drops a small amount below the now negative voltage on the non-inverting input, the output voltage V_{OUT} will go positive and snap to its positive state caused by the feed-back action to the non-inverting input. Now the cycle will start over again.

The zeroing network allows adjustment of the pulse width. With zero input signal, the time ratio of the square wave can be adjusted to give an average value of zero volts. If t_1 denotes the duration of the positive output state and t_2 the duration of the negative output state, then t_1 equals t_2 for the balanced condition. Refer to the output waveform shown in Figure 1.

FAIRCHILD
SEMICONDUCTOR

The time t_1 can be found from the following mathematical expression:

$$\left(\frac{V_{IN}}{R_{IN}} + \frac{V_{OUT}}{R_F} + \frac{V_{REF}}{R_4} \right) t_1 = 2\, C\, V_{OUT} \frac{R_1}{R_1 + R_2}$$

The time t_2 is obtained from:

$$\left(\frac{V_{IN}}{R_{IN}} - \frac{V_{OUT}}{R_F} + \frac{V_{REF}}{R_4} \right) t_2 = 2\, C\, V_{OUT} \frac{R_1}{R_1 + R_2}$$

The ratio of the time t_1 to the period of the square wave $T = t_1 + t_2$ is given by the expression:

$$\frac{t_1}{t_1 + t_2} = \frac{1}{2} - \frac{\frac{V_{IN}}{R_{IN}} + \frac{V_{REF}}{R_4}}{2\, \frac{V_{OUT}}{R_F}}$$

It is interesting to note that the capacitance does not show up in this relationship. Any changes in the value of C will, therefore, not affect the accuracy of this ratio which is a linear function of the input voltage V_{IN}. It should be mentioned that both $\pm V_{OUT}$ and V_{REF} have to be held constant with temperature to insure high accuracy of the converter.

The frequency of the rectangular wave is given by

$$f = \frac{1}{t_1 + t_2} = \frac{1 - \left(\frac{V_{IN}}{R_{IN}} + \frac{V_{REF}}{R_4} \right)^2 \left(\frac{R_F}{V_{OUT}} \right)^2}{4\, \frac{R_1}{R_1 + R_2}\, R_F\, C}$$

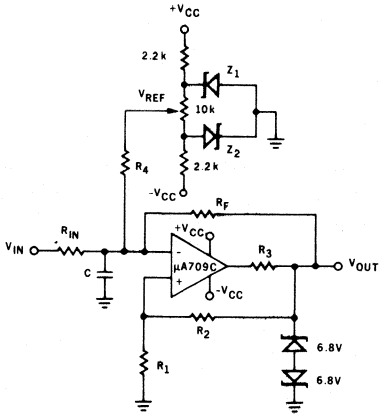
From this equation it can be seen that the frequency is dependent upon the square of the applied input voltage as well as the capacitor C. By proper choice of the input signal range, the variation in f can be kept quite low. For many applications, a small variation in frequency is of no consequence anyway.

If a true pulse width modulated signal in place of the time ratio modulated square wave is desired, a simple grounded emitter transistor stage with zenered output (Figure 2) can be added to the circuit of Figure 1.

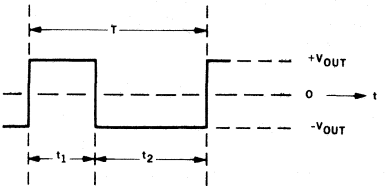
APPLICATIONS:

The conversion of an analog signal to a pulse width modulated signal overcomes many of the problems encountered when analog signals have to be transmitted in the presence of noise. Many industrial control systems use transducers for temperature, pressure, humidity, etc. which have electric analog outputs. By adding this simple converter, some of the advantages of transducers with digital output can be realized.

Another typical use for the converter described in this note is in connection with analog multipliers. By modulating the pulse height in proportion to a second analog signal, the average value of the resulting pulse train is proportional to the product of the two applied analog values.



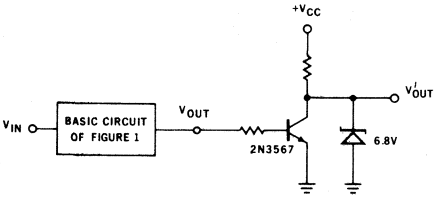
R_{IN} = 10k
R_F = 4.7k
R_1 = 2.2k
R_2 = 1M
R_3 = 1k
R_4 = 47k
C = 2.2μF
$V_{Z_1} = V_{Z_2} \approx 1/3\ V_{CC}$

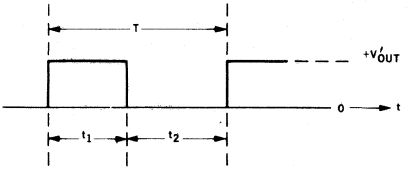


Basic Circuit Diagram of Analog to Time Ratio Modulated Square Wave Converter.

Typical Output Voltage Waveform.

FIGURE 1.





Typical Output Voltage.

FIGURE 2.

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APPLICATIONS BRIEF 54

FOUR QUADRANT ANALOG MULTIPLIER

INTRODUCTION

The multiplier described in this applications brief is capable of finding the product of two analog signals. It is a "four quadrant" multiplier since it will accept both positive and negative values of the two input signals and produce the mathematically correct sign for the output signal.

PRINCIPLE OF OPERATION

A schematic block diagram of the multiplier is shown in Figure 1. The basic blocks are an analog-to-pulse-width converter, an inverter, an electronic switch, a summer and a filter. (In the actual implementation of the multiplier the summer and filter blocks are combined into one unit).

The first of the two factors (an analog voltage signal v_a) is applied to the analog-to-pulse width converter which produces an output voltage v_p in the form of a time ratio modulated square wave as shown in Figure 2. The time ratio of this square wave $t_1/(t_1 + t_2)$ is proportional to the voltage v_a.

The second factor of the product to be found (an analog voltage signal v_b) is made available to the electronic switch in both its positive and, after passing through the inverter, its negative form. Depending on whether the output of the converter is positive or negative, either switch SW1 or switch SW2 will be closed. This in turn applies either the negative or the positive version of v_b to the summer for a period of time dictated by the output of the converter. The output of the summer (see Figure 3) will, therefore, be a square wave whose amplitude h is proportional to v_b and whose time ratio is proportional to v_a. In mathematical form:

$$h = k_1 \cdot v_b$$

$$\frac{t_1}{T} = k_2 \cdot v_a$$

The output of the summer is applied to a low-pass filter which produces the average of the applied square wave function v_s

$$v_{out} = \frac{1}{T} \int_{(T)} v_s\,(t)\,dt = K_3 \cdot v_a \cdot v_b$$

K_1, K_2, and K_3 are constants.

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SEMICONDUCTOR

DESCRIPTION OF CIRCUIT

The total circuit is shown in Figure 4. The basic blocks are identified again.

The analog to pulse width converter uses a μA741. The "bucket" capacitor is charged and discharged as the output voltage toggles between its positive and negative states. This toggle action is caused by the resistive feedback circuit to the non-inverting input of the μA741. (See also Applications Brief No. 51).

The inverter is a straight forward circuit using another μA741. One of the advantages of using the μA741 is that it will not require external compensation.

The electronic switch consists of two junction FET's, one p-channel and one n-channel. These FET's are driven by the output of the analog to pulse width converter. To obtain a better switched wave form, a 62pF capacitor is connected across the 1MΩ resistors in the gate circuit.

As mentioned before the summer and low-pass filter are combined in a circuit using one μA741. For the circuit chosen the transfer function from either input (coming from the electronic switch) to the output is given as

$$H(s) = \frac{1/R_{IN}\, R_F}{s + 1/R_F C_F}$$

and, with the chosen values this becomes

$$H(s) = \frac{10}{s + 10}$$

making the corner frequency of the filter

$$f_c = \frac{10}{2\pi} \doteq 1.6 \text{ Hz}$$

It should be mentioned that with additional circuitry the three μA741's could be replaced by μA709's.

Linearity and accuracy of this circuit is better than 1%. No measurable drift was detected at room temperature over a 24 hr. period. With the element values as shown the output frequency of the analog to pulse width converter is 2.15 kHz. The frequency response of the multiplier will be determined by the chosen converter frequency.

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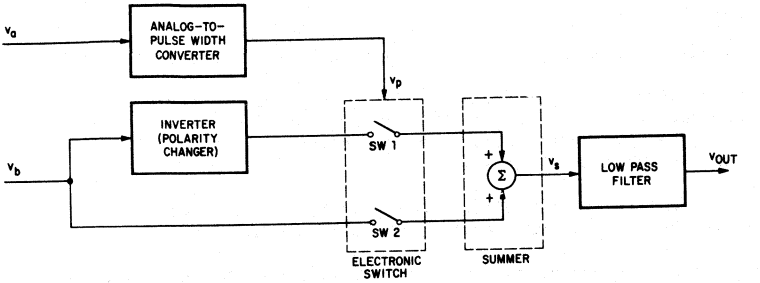


Fig. 1. Block diagram of four quadrant analog multiplier.

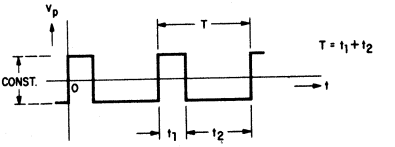


Fig. 2. Output voltage v_p of analog-to-pulse width converter.

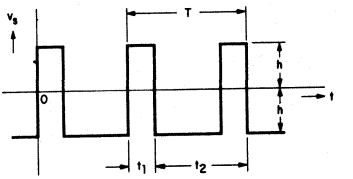


Fig. 3. Output voltage v_s of summer.

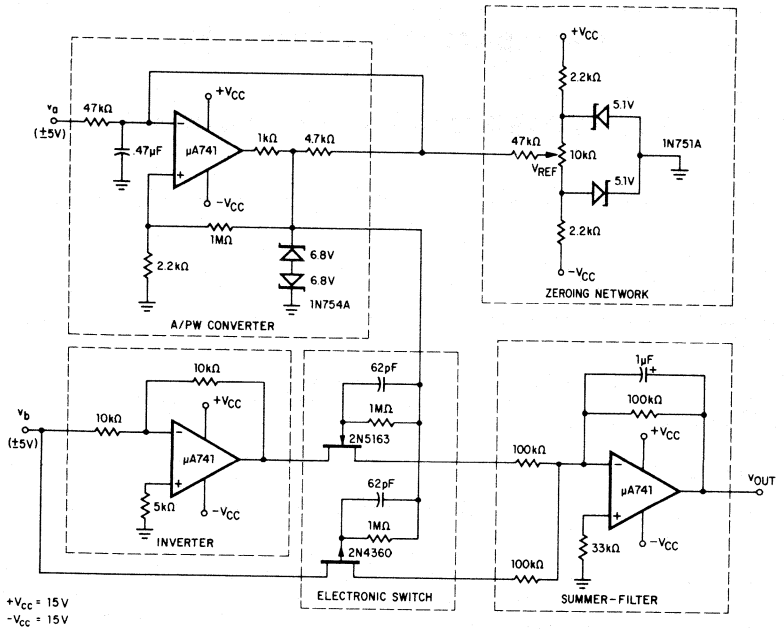


Fig. 4. Circuit diagram of four quadrant analog multiplier.

APPLICATIONS BRIEF 66

FM STEREO MULTIPLEX DECODER

INTRODUCTION

An economical, high quality FM stereo multiplex decoder is described. This circuit, utilizing a μA709C integrated amplifier, features ease of alignment and is compatible with both mono and stereo signals.

CIRCUIT DESCRIPTION

The circuit can be grouped into three sections; a 19 KHz amplifier, a doubler and amplifier, and a diode switching section.

Q_1 operates as a high selective 19 KHz amplifier and emitter follower. High selectivity and good rejection of frequencies other than 19 KHz is achieved with the transformer T_1 and the coil L_1. The emitter of Q_1 provides a low impedance source and a clean composite signal for the 38 KHz transformer (see Picture 2). The secondary of T_1 feeds the μA709C amplifier with a 19 KHz signal.

The μA709C operates as a 19 KHz amplifier and provides a signal for doubling in the 38 KHz transformer T_2. This is achieved by changing the bias on the second stage of the μA709C with a resistor R_1 from Pin 1 to ground which clips the lower part of the 19 KHz signal. The clipped 19 KHz output of the μA709C resonates the transformer T_2 tuned to 38 KHz. By adding the composite signal to the center of the 38 KHz transformer secondary results into an AM modulated signal as shown in Picture 3.

The diodes for decoding are fed from T_2 over a 27 μsec time constant for proper switching action (see Picture 4). C_1 and C_2 provide filtering of the 38 KHz switching pulses and recovery of the audio modulation with left and right channel separated. R_2, R_3, C_3, and C_4 provide the FM de-emphasis roll off in conjunction with C_1 and C_2.

Due to the good limiting of the μA709C, very little phase shift occurs with change of signal level or supply voltage and, therefore, constant separation is obtained.

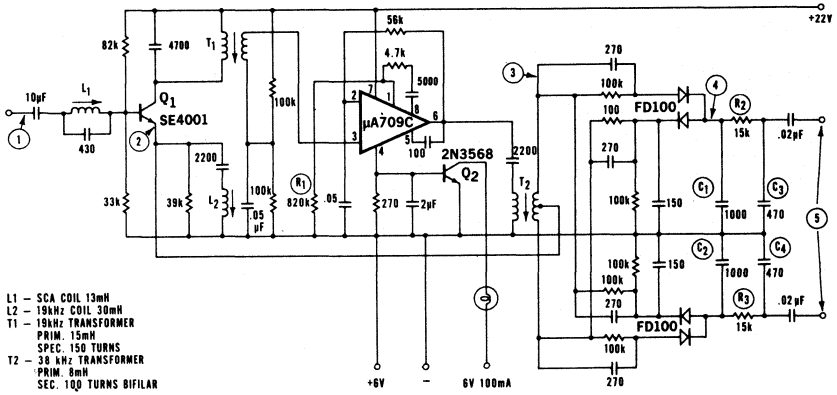
For the stereo indicator, a bypassed current sensing resistor is inserted between the μA709 and ground which drives, utilizing the current swing of the μA709, the transistor Q_2 and operates the beacon light.

Alignment of the coils is quite simple, by adjusting each coil until a maximum 38 KHz signal is achieved at T_2. Final separation adjustment is done by monitoring the output of the unwanted channel and adjusting the 38 KHz transformer T_2 for minimum output.

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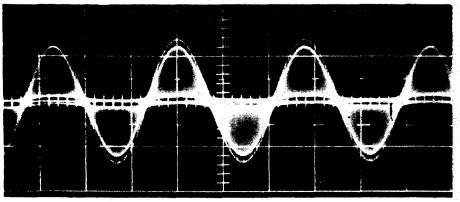
PERFORMANCE SPECIFICATION

Separation	100 Hz	1 KHz	10 KHz
1V Input L to R	>33 db	>33 db	>18 db
1V Input R to L	>33 db	>33 db	>18 db
45 mV Input L to R		>27 db	
45 mV Input R to L		>27 db	
Supply Voltage			
Variation 16V to 28V		>30 db	
Insertion Loss At Stereo		2 db	
Insertion Loss At Mono		4.5 db	
Input Impedance		22 K	
Output Impedance		47 K	
Distortion Mono Input 1V 1 KHz	.25% (Generator .1%)		

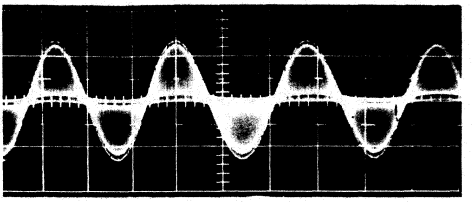


L1 – SCA COIL 13mH
L2 – 19kHz COIL 30mH
T1 – 19kHz TRANSFORMER
PRIM. 15mH
SPEC. 150 TURNS
T2 – 38 kHz TRANSFORMER
PRIM. 8mH
SEC. 100 TURNS BIFILAR

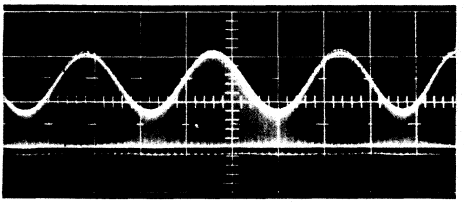
STEREO M.P.X. DECODER



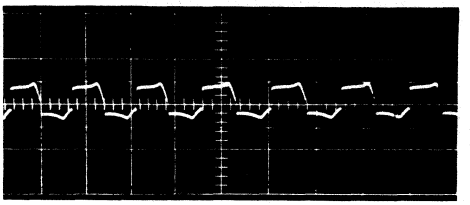
INPUT SIGNAL (1)



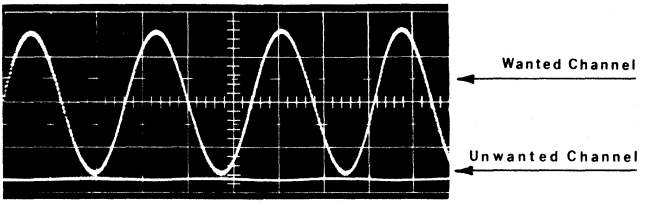
SIGNAL AT POINT (2)



WAVEFORM AT POINT (3)



WAVEFORM AT POINT (4)



RECOVERED AUDIO SIGNAL

APPLICATIONS BRIEF 85

SOME USEFUL SIGNAL PROCESSING CIRCUITS USING FET's AND OPERATIONAL AMPLIFIERS

ABSTRACT

The concept of the operational amplifier, used with a junction FET operating in its linear region, is introduced. The concept is then exemplified in a number of circuits for gain and bandpass control of audio frequency signals, including compressor amplifiers and voltage-tuned filters.

INTRODUCTION

There are two introductions to be performed; the first is that of the μA741[1]. This is an operational amplifier which has its own internal frequency compensation, together with many other excellent features. Its frequency response looks like this

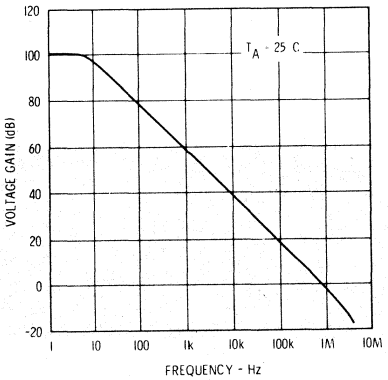


Figure 1: μA741 Open Loop Frequency Response

This means that the only components needed for basic operation are as shown.

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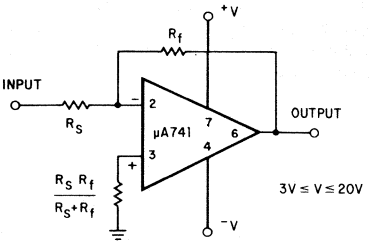
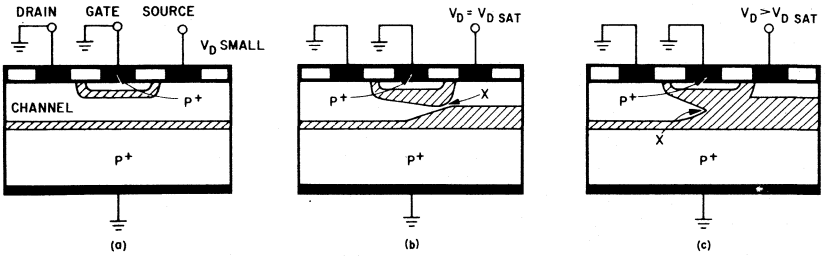


Figure 2: μA741 Basic Configuration

No frequency compensation networks are required; and, of course, as with all operational amplifiers, the gain is given by

$$A = \frac{R_f}{R_s}$$

The second introduction is that of the 2N5163, a depletion type, N-channel, junction FET in an epoxy package. A device of this kind could be depicted as illustrated below.



The shaded areas are the depletion regions surrounding the junctions. Manipulation of the bias voltages will cause the depletion regions to move closer together, thereby, reducing the width of the channel and increasing its resistance. For small values of drain to source bias, the variations of channel resistance with gate to source bias are

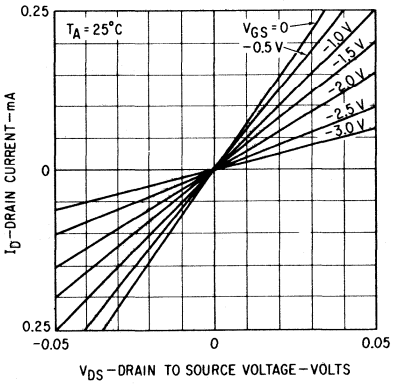


Figure 4: 2N5163 Low-voltage drain characteristics

Thus, for small AC signals applied between drain and source, the device presents a resistance whose value is determined by the gate-to-source voltage. (It is of interest to note here that an FET is often referred to as a unipolar transistor because the current in the channel is made up only of majority carriers; whereas, in a bipolar transistor, the current consists of carriers of both polarities).

The actual value of the channel resistance is given by[2]

$$R_{DS} = \frac{R_o}{1 - \left[\frac{8K_s E_o(\phi_B - V_G)}{qN_D d^2}\right]^{1/2}}$$

where all the symbols have the usual values. However, for our humble purposes, the following approximation is more than adequate

$$R_{DS} = \frac{R_o}{1 - \frac{V_{GS}}{V_p}}$$

where V_{GS} is the gate to source bias, V_p is the gate to source bias for pinch-off or zero conduction and R_o is the value of the channel resistance at $V_{GS} = 0$.

We should close this introduction with a word about distortion. The next figure shows the percentage second harmonic distortion as a function of drain to source signal voltage for various values of gate bias.[3] The ordinate is the percentage of second harmonic in the drain current and the abscissa is the AC voltage applied between drain and source. The running parameter is the gate to source bias voltage .

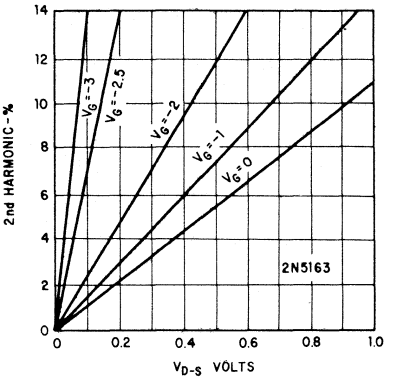


Figure 5: Drain current 2nd harmonic component as a function of operating point.

This shows that to minimize distortion, we should work at the low resistance (low-gate bias) end of the device characteristic and keep the impressed signal voltage as low as possible.

Having introduced the two performers, we can now proceed with the play. Many circuits using operational amplifiers require a variable resistance in order to vary gain or frequency response or whatever. Very often, it is desirable to have this resistance variation controlled from a point far from the op. amp. It is apparent that our FET would suit this purpose admirably since it would obviate the use of long-signal paths and permit more complex control characteristics than possible with ordinary potentiometers. Let us proceed to consider some of these FET op amp combinations.

Gain-Controlled Amplifier

The next figure shows an amplifier whose voltage gain from input to output is given by $A = R_f/R_S$, as mentioned earlier.

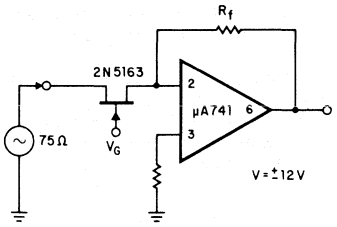


Figure 6: Gain Controlled Amplifier

Now, R_S is the drain-source resistance of the FET and is controlled by V_{GS}, the gate to source voltage. Note that the FET source is always at ground, since this is a feature of the op. amp., thus the gate potential specifies the gate-source bias. The variation in amplifier gain with gate voltage is shown in the next figure.

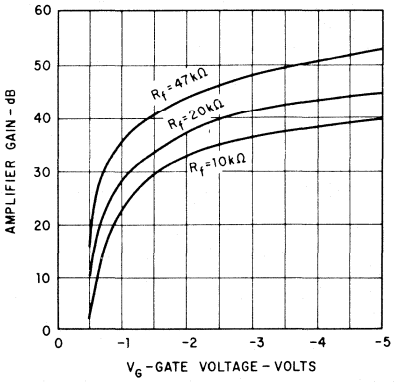


Figure 7: Gain-controlled amplifier characteristics

The following figure shows the variation of gain with temperature.

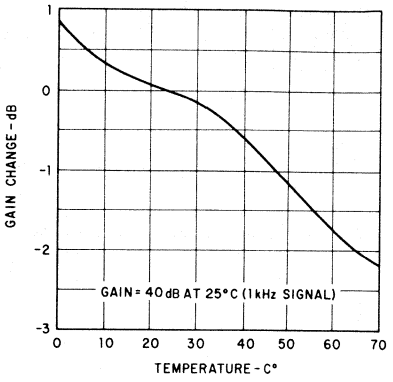


Figure 8: Gain variation with temperature

A Compressor Amplifier

If we now rectify the output of the amplifier, we can derive a d-c voltage which is proportional to the signal level. If this d-c voltage is used as the FET control voltage, the effect will be to stabilize the output level with variations in input. A simple circuit for this function is shown below.

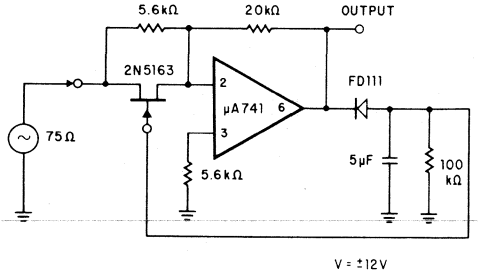


Figure 9: Simple compressor amplifier

At higher input signal levels (where we want lower gain), we reach the distortion condition described earlier. This can be overcome by adding a resistor in shunt across the FET. Now, when the control range of the FET is exceeded, the amplifier performs normally.

The action of the circuit can be considerably tightened up by adding some gain in the feedback loop. The next figure shows a second μA741 used to drive the rectifier while the output is taken from the first one, as before.

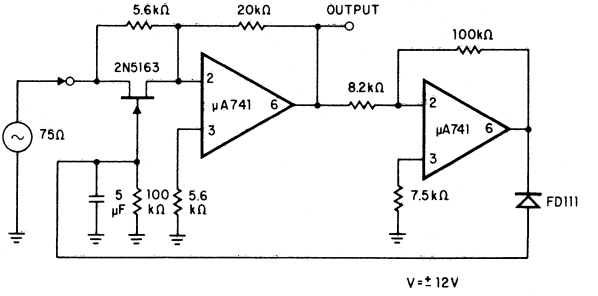


Figure 10: Advanced Compressor Amplifier

This circuit gives 2 dB change in output level for 30 dB change in input. The performance curves for both circuits are shown below.

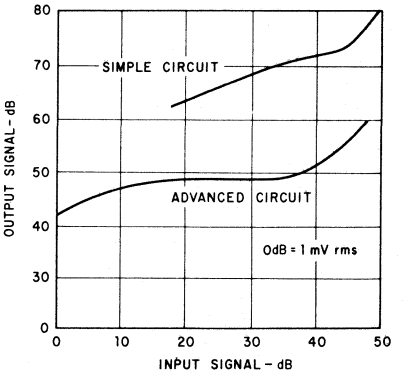


Figure 11: Compressor Amplifier Characteristics

For a more rigorous treatment of this subject, see Reference 4.

A Voltage-Tuned Active Filter

The circuit below is a fairly well-known active-filter configuration.[5]

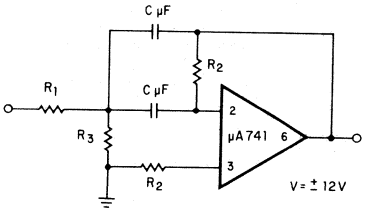


Figure 12: Basic Active Filter

The values of the various components are given by

$$R_1 = \frac{1}{2\pi\Delta AC}$$

$$R_2 = \frac{1}{\Delta\pi\ C}$$

$$R_3 = \frac{1}{2\ \pi C\left[\frac{2f_o^{\ 2}}{\Delta} - \Delta\ A\right]}$$

where Δ is the 3 dB bandwidth in H_z, A is the voltage gain and f_o is the center frequency. The advantage of this particular configuration, from our point of view, is that the center frequency is controlled solely by R_3 (for fixed values of all other components). Thus, by putting our FET in place of R_3, we have a voltage-controlled filter, as shown below.

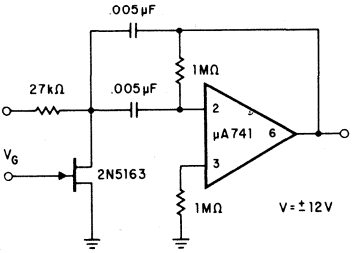


Figure 13: Voltage Tuned Filter

The filter performance for the given component values is shown in the next diagram. Since the bandwidth was fixed at 80 Hz, the Q varied from 2.5 at 200 Hz to 40 at 3.2 kHz. The gain of the filter was 26 dB and the maximum variation in gain over the tuning range was ± 1 dB.

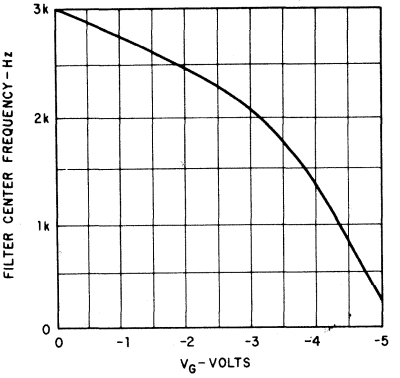


Figure 14: Voltage Tuned Filter Characteristic

When we come to consider thermal stability, the picture changes somewhat. The next set of curves shows the variation in center frequency over the temperature range from 0°C to 70°C for various initial settings.

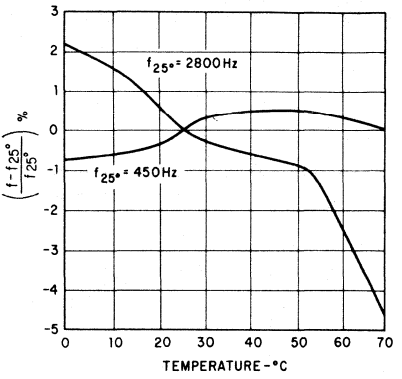


Figure 15: Variation in Center Frequency with Temperature

It can be seen that under some conditions, the circuit would make a good digital thermometer. To understand a little more about these curves, we must look at the temperature response of the FET channel resistance, as shown below.

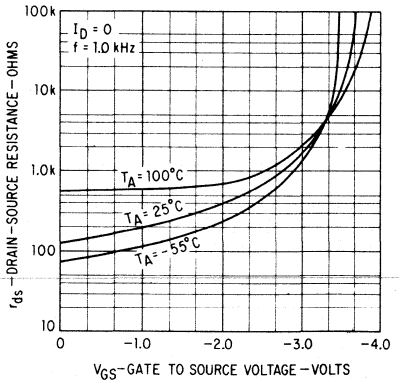


Figure 16: Variation of FET channel resistance with Temperature

Notice that for low-gate voltages the temperature coefficient is positive; closer to pinch-off voltage, the temperature coefficient approaches zero and beyond pinch-off, the drain-source resistance has a negative temperature coefficient. This effect, combined with the non-linear R_{DS} vs. V_{GS} characteristic, makes it very difficult to thermally stabilize the device and still maintain the filter tuning range. To keep the circuit simple, tuning range was sacrificed for thermal stability. If we set our lowest desired frequency at FET pinch-off with a shunt resistor, the upper frequency with a series resistor, as shown in the next diagram, and confine ourselves to a one octave tuning range, we can achieve better results.

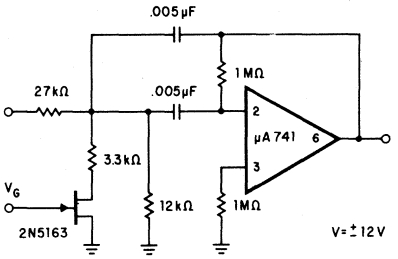


Figure 17: Voltage tuned filter with restricted range for improved thermal stability.

The performance of this circuit was as follows:

	Lower Tuning Freq. (380 Hz)	Upper Tuning Freq. (760 Hz)
Deviation at 0°C	-1%	-2.7%
Deviation at 70°C	+1.8%	+3%

Now it will depend on the application as to how acceptable these figures are. If the deviation is within the bandwidth and the tuning range is sufficient, then the requirements for a stable, tunable filter would seem to be met.

A Voltage Controlled Oscillator

It is a short step from an active filter to an oscillator (too short for some people). If we invert the filter output and feed a suitable portion back to the input we can realize a voltage controlled oscillator or VCO as it is often called.

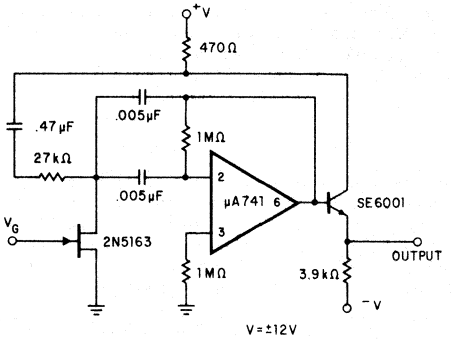


Figure 18: Voltage controlled oscillator

This circuit uses the same frequency determining components as the original filter described above and its output frequency covers the same range. Obviously, a sweep may be generated by applying a ramp at the gate. There is a variation in output amplitude over the range, however, and it might be useful to employ our compressor amplifier as the feedback element here. This would make for a very amplitude-stable VCO. Of course the remarks made earlier about temperature stability would still apply. The latter problems might possibly be over come by the following configuration.

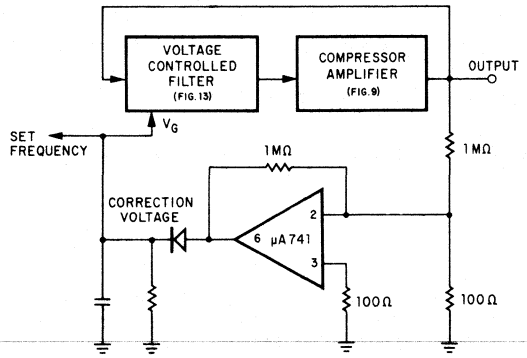


Figure 19: Advanced VCO

Here the compressor block performs the function of amplitude stabilization with a level control also provided. The μA741 is being used as a low-pass Filter (see Figure 1) and its detected output, in conjunction with the frequency set-up voltage, is used to initially

the oscillator output frequency. Any subsequent frequency change due to thermal changes within the loop will generate a DC correction voltage at the gate of the control FET which will tend to pull the frequency back to the set value. As may have been inferred, this system has not yet been tried, but it is suggested here as a logical combination of the basi building blocks described above.

Onward and Upward

A number of circuits for higher frequency operation using the voltage variable resistance concept have previously been written about.[6] In addition the principles involved here may be implemented into the video frequency range by means of a suitable operational amplifier, e.g., the μA702 or μA715. At frequencies where the drain-to-source capacitance of the FET becomes noticeable (above 1 MHz), it may be necessary to tune out this capacitance with a shunt inductance, thereby eliminating any undesirable phase shift over the operating range.

It may also be apparent that the functions discussed here could be achieved using discrete devices as amplifiers. The μA741 is, however, such a simple and stable device that it is well worth using here and it increases the versatility of the configurations many-fold.

Note one further advantage of the configurations employed, namely that no DC drain bias is used with the FET. This means that I_{DSS} (the drain current for V_{GS} = 0) variations are not a consideration and devices may be interchanged easily. The design of the various circuits should however include a consideration of $R_{DS(ON)}$ (the drain to source resistance for V_{GS} = 0) which will vary from device to device.

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1. "Linear Integrated Circuits Applications Handbook, Number 2", Fairchild Semiconductor.
2. Grove, A. S., "Physics and Technology of Semiconductor Devices", Chapter 8 Wiley.
3. Campbell, David L., "Some Characteristics of Junction FET's in the Linear Region" 36th Annual Convention of the Audio Engineering Society, April/May, 1968.
4. Bingham, D., "An Audio Compressor and Expander", Fairchild Consumer Microcircuits Circuit Note No. 3.
5. "Handbook of Operational Amplifier Active RC Networks", Burr-Brown Research Corporatio p. 78.
6. Doyle, N., "Some Ideas for Solid State Color TV Circuits", Fairchild Semiconductor Applications Brief No. 74.

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AN ECONOMICAL D/A OR STAIRCASE GENERATOR USING THE μA739

INTRODUCTION

Electronic systems often utilize digital computers to supply control voltages for process controlling or data display. Such systems sometimes require a BCD D/A converter or a BCD activated staircase generator to buffer the digital computer output to the controlled elements of the system.

BCD type D/A conversion and staircase waveform generation can become quite costly if precision ladder networks, comparators, reference supplies and ladder switches are used to obtain extreme accuracy. But, in many systems where supreme accuracy is not required, a simple circuit based on the utilization of three μA739 dual operational amplifiers can be realized to bring D/A and staircase generator costs down to a reasonable level. The staircase generation feature is a natural fallout from its basic D/A design.

PROBLEM

Design a sub-system to resolve digital BCD information obtained from a "sample and hold" type input signal device to an analog output accuracy of ≤1% full scale (f.s.) assuming 3 digit (twelve bits, 4 per digit) input data is available. The same system should also perform as a staircase generator when the input signal mode is changed to "sampling" only.

SOLUTION

Switch the 3 digit BCD binary inputs to binary weighted summing inverting amplifiers, sum those inverting amplifier outputs with a decade weighted inverting amplifier and buffer that second summation value to the outside world.

The "solution" block diagram is illustrated by Figure 1. Practical circuitry is shown by Figure 2. Component values are listed in Table I. Pin numbers and compensation are indicated in Figure 3.

CIRCUIT PHILOSOPHY (referencing Figure 2)

Since all the summing amplifiers are operating as inverting amplifiers, near or at unity gain, their offset and gain drifts are not critical. Voltage follower "E" and inverting amplifier "F" conveniently provide a common offset reference voltage for all other inverting amplifiers and provide a "bucking" action such that zero drift is minimized.

Transistors Q_1 through Q_{12} are used in the reverse saturated mode to reduce their voltage drops.

The most significant digit (MSD) primarily controls the absolute f.s. accuracy of this D/A converter, thus the only critical elements of the system are the prime weighting resistor ratios of inverting amplifier "C". Properly setting

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these ratios with trimmer potentiometers provides a sufficient safety factor for gain differentials, temperature, ageing and component mismatch effects.

OTHER OPTIONS

This D/A technique is good for 0-999 BCD input data but can readily be expanded to larger input values by either (1) switching all twelve binary inputs to the most significant 3 digits of a 5 or 6 digit BCD output device or (2) paralleling more binary summing inverting amplifiers, one for each desired decade and only switching in the 3 most significant digits at the decade summing point (input to inverting amplifier "D").

STAIRCASE GENERATOR MODE

Setting the BCD input device to a "sampling" condition, rather than "sample and hold" and repetitively applying a swept input of 0 to 1,000 provides the circuit user with five discrete staircase waveforms. Inverting amplifier "A" output will exhibit a positive going staircase waveform of 10 discrete equal steps 100 times per repetition. Inverting amplifier "B" output will perform the same as inverting amplifier "A" but 10 times per repetition. Ditto for inverting amplifier "C" but 1 time per repetition. Their summed output waveform (available at the input of inverting amplifier "D") will exhibit a positive going staircase waveform of 1000 discrete equal steps one time per repetition. Inverting amplifier "D" staircase output waveform will be the same as its input but will be negative going.

Changing the BCD input signal span or repetition rate will vary all of the five staircase waveforms accordingly.

The number of inverting summing amplifiers is flexible. One or more can be used depending on the number of discrete steps required and the complexity or interplay desired.

CIRCUIT DETAILS

Assuming all switches are open (transistors Q_1 through Q_{12} base to collector diodes "off") inverting summing amplifiers "A", "B", and "C" outputs will be at their non-inverted input voltage reference level as this value will maintain a zero voltage differential between the invert and non-invert inputs. In this case the output level is +3.0 volts. Closing any one of the switches (base to collector diode "on") will cause a differential voltage to appear between the inverting and non-inverting inputs of that particular inverting amplifier. (This differential voltage is due to the voltage divider action of the feedback resistor and switched resistor). The negative shift in level at the inverting input causes the output of that inverting amplifier to go further positive until a state of equilibrium is reached when the differential voltage between the inverting and non-inverting inputs is again zero. The magnitude of this positive shift is strictly dependent upon the magnitude of the initial input differential voltage, which in turn is determined by the ratio of the feedback resistor and switched resistor.

BCD TO DECIMAL DECODING

(Reference 1)

Binary Input	R_s (Switched In Resistance)	E_o (Amplifier Output Value)	Voltage Δ from V_{ref}	Decimal Equivalent
0	∞	3.000V	0.000V	0
1	160K	3.375V	.375V	1
10	80K	3.750V	.750V	2
100	40K	4.500V	1.500V	4
1000	20K	6.000V	3.000V	8
1010	*16K	6.750V	3.750V	10

*(20K and 80K paralleled)

The same action occurs when summing the outputs of inverting summing amplifiers "A", "B", "C" and "F" to decimal weight their outputs (at the invert input of inverting amplifier "D") to 0.01, 0.10 and 1.00 respectively.

Transistor Q_1 through Q_{12} voltage drops can be kept down to 2MV or less by using an emitter resistor value of $\geq$20K and by driving the base-collector diode with $\geq$1.4 ma of current.

Trimmer R3 is adjusted to cancel out transistors Q_{10}, Q_{11} and Q_{12} voltage drop differences and the 1:1.333 $R_2/2R$ and 4R resistance ratio error for the most significant digits (MSD) 8 and 6.

Potentiometer R_6 is set to cancel the 10:1 $R5/10R_1$ resistance ratio error.

R14 effectively cancels all system DC unbalances (with transistors Q_1 through Q_{12} in the "off" condition) when it is adjusted to set inverting amplifier "D" output at zero volts.

Trimmer R11 in turn established the maximum desired output swing at E_o for a BCD binary input of 999. In this case the desired output was -99.9 MV.

All ±1% resistors should have a temperature coefficient of $\leq$ 200 ppm/°C.

WORSE CASE ERRORS (referenced to f.s.)

f.s.	$\leq$ 0.2%
0.4 of f.s.	$\leq$ 0.2%
0.2 of f.s.	$\leq$ 0.1%
0.1 of f.s.	$\leq$ 0.2%

All other errors below 0.1 f.s. are $\leq$0.2%.

These values have been calculated with worse case values for all the ±1% resistors.

REFERENCE VOLTAGE SENSITIVITY

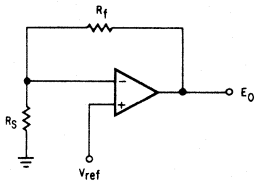
Because the output voltage swing is directly related to V_{ref} (see Reference 1), V_{ref} variations effect full scale accuracy. Therefore, a stable V_{ref} is highly recommended.

CONCLUSIONS

The feasibility of manufacturing a stable $\leq$1% f.s. D/A converter at a reasonable cost has been demonstrated. The circuitry has inherent flexibility; the BCD decoding and decimal weighting schemes can be replaced by any other decoding or weighting values desired by the designer if he wishes to use an existing digital signal for a given system.

REFERENCES

1.



R_f = 20K

$$E_o = \frac{V_{ref}\,(R_s + R_f)}{R_s},$$

$R_s \longrightarrow \infty$, $E_o \longrightarrow V_{ref}$

TABLE I

Q_1 through Q_{12} Inverting Amplifiers	2N3641 1/2 Fairchild μA739
D_1	1N 751
R	20K ± 1%
2R, R_{18}, R_{19}	40K ± 1%
4R	80K ± 1%
8R	160K ± 1%
R_2	19.1K ± 1%
R_5, R_{13}, R_{10}	29.4K ± 1%
R_{17}	27.4K ± 1%
$10R_1$	300K ± 1%
R_8	3.92K ± 1%
R_9	6.04K ± 1%
R_{16}	1K ± 1%
R_3, R_6, R_{11}	2K (wirewound)
R_o, R_{20}	20K ± 5%
$2R_o$	40K ± 5%
$4R_o$	80K ± 5%
$8R_o$	160K ± 5%
$100R_1$	3 Meg Ω ± 5%
R_4	10K ± 5%
R_7	2.2K ± 5%
R_{12}	11K ± 5%
R_{21}	1.1K ± 5%
R_{15}	36K ± 1%
R_{14}	500Ω (wirewound)

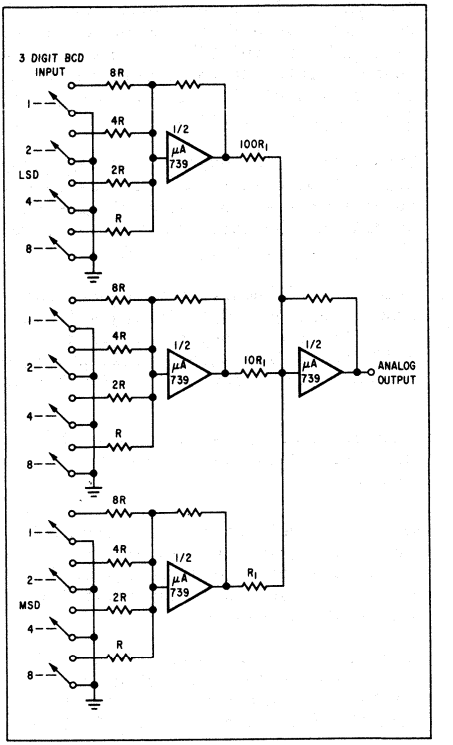


Figure 1.

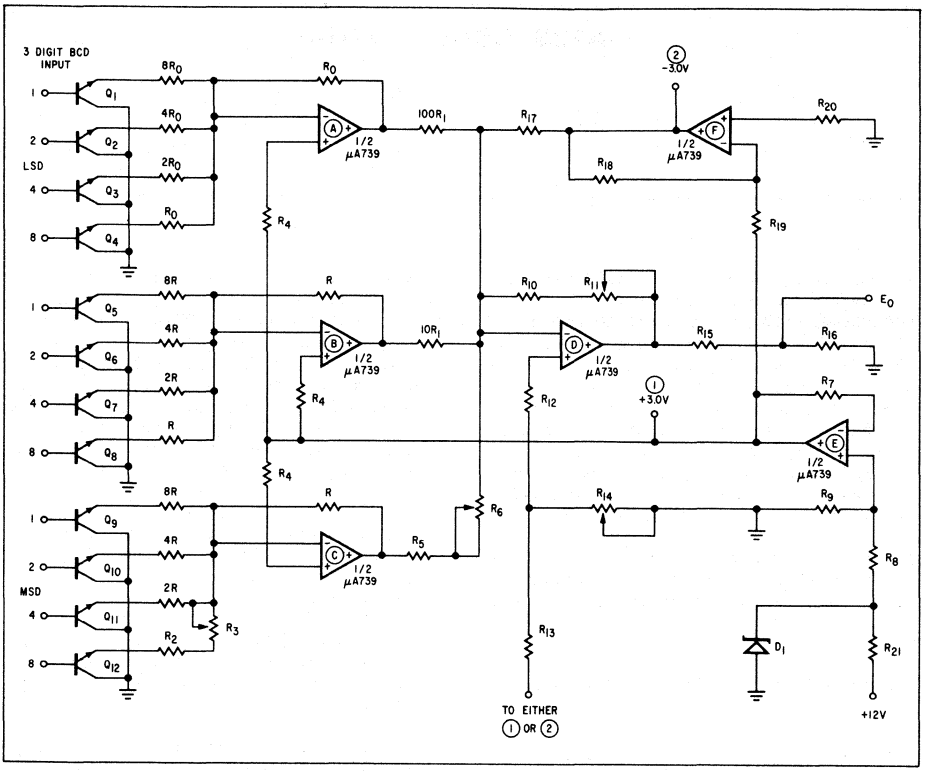


Figure 2.

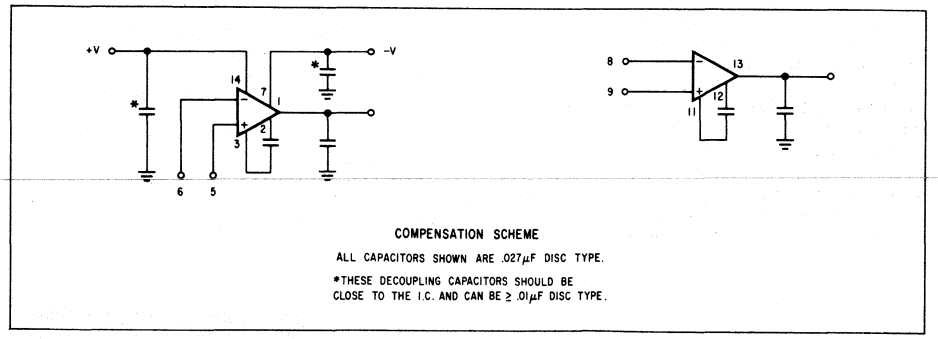


Figure 3.

μA733 OSCILLATORS

The μA733 wideband video amplifier can be used as an oscillator with the addition of three external components. Oscillation can be obtained at frequencies from several Hertz to over 10 Megahertz. Crystal controlled and voltage controlled oscillators are simply obtained and the output signal can drive $T^2\mu L$ or DTμL logic directly. The rise and fall times of the output waveform are less than 10 nsec, due to the wide bandwidth of the μA733 amplifier.

The circuit diagram of the basic oscillator is shown in Figure 1. Positive feedback is supplied by capacitor C and the voltage divider formed by R_1 and R_2.

The period of oscillation, T is given by

$$T \cong 2\,(R_1 + R_2)\,C\,\ln\left[A_v\left(\frac{R_1}{R_1+R_2}\right) - 1\right] \quad (1)$$

The relationship is approximate as the μA733 draws input bias current when the input signal is positive and nc input current when the input is negative. This causes the duty cycle of the oscillation to differ slightly from the ideal of 50%, hence the coefficient of the above equation is not exactly 2.

The division ratio of R_1 and R_2 is constrained to values between about 0.2 and 0.4 for $A_v = 10$. The lower limit is established by the equation for T since the inequality $(A_v)\ \frac{R_1}{R_1+R_2} \geq 2$ must hold for practical solutions. The upper limit is determined by the single-ended output voltage swing and by the input voltage range of the device, ± 1 volt. Figure 2 shows a comparison between the calculated and measured frequency as a function of capacitance.

The frequency of oscillation may be voltage controlled in several ways. R_1 can be paralleled by a field effect transistor and the drain resistance of the FET controlled by varying its gate voltage. Care must be taken to insure that the division ratio restrictions, discussed in the previous paragraph, are met for the combination of R_1, R_2 and the FET.

Another means of controlling frequency is indicated by Equation 1. Since the period of oscillation is proportional to the natural log of the μA733 gain, the frequency can be varied by controlling the gain magnitude with a variable resistance. This can be accomplished by connecting a FET across the gain adjusting terminals of the μA733 as shown in Figure 3. Using a device such as the 2N4360 junction FET as the gain control element will yield a frequency variation of approximately 3:1. The higher the gain the lower the frequency.

Crystal control of oscillations can be

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accomplished, in principle, by replacing capacitor C with a crystal of the desired frequency. While this scheme will usually work, it is possible to excite overtone modes of oscillation in the cyrstal and hence obtain undesired outputs. A tuned circuit included in the feedback circuitry will favor oscillation at the frequency to which it is tuned and suppress spurious modes of oscillation. The operation of the oscillator with crystal control is essentially linear, as opposed to the non-linear RC relaxation mode previously discussed.

A schematic for a crystal oscillator is shown in Figure 4. The voltage division ratio of the capacitors C_1 and C_2 should be greater than the reciprocal of the μA733 gain in order to sustain oscillation. As mentioned previously the μA733 output can be used to drive $T^2\mu L$ or DTμL logic directly thus providing a crystal controlled clock for digital circuitry.

Circuits using the μA733 video amplifier as an RC relaxation oscillator, voltage controlled oscillator and crystal have been discussed. The output levels of the μA733 make it possible to interface directly with $T^2\mu L$ or DTμL logic circuits. The μA733 may be operated from plus and minus 5 volt power supplies allowing the device to share its positive supply with digital circuitry.

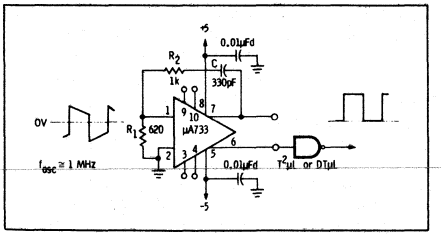


Fig. 1. RC oscillator using the μA733.

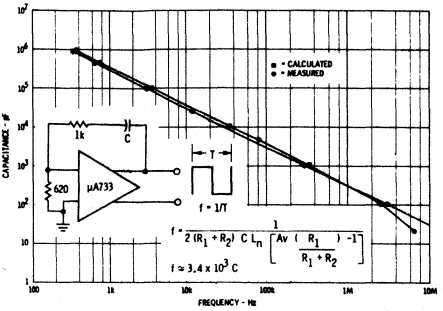


Fig. 2. μA733 oscillator frequency for various capacitor values.

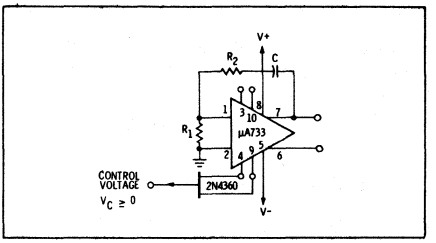


Fig. 3. Voltage controlled oscillator.

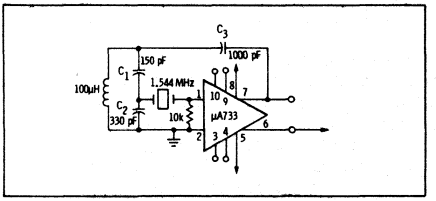


Fig. 4. Crystal oscillator.

THE μA715, A VERSATILE HIGH SPEED OPERATIONAL AMPLIFIER

SUMMARY

This report describes four applications of the μA715 that utilize the superior characteristics of this device to the fullest. They are:

1. An image orthicon head amplifier with a 4-way distribution amplifier designed to feed 75Ω cable.
2. A general purpose video amplifier with 40dB gain, 50Ω input impedance, and 10V p-p output capability.
3. As above, except 60dB gain, and 75Ω input impedance.
4. A 40dB, high input impedance amplifier.

GENERAL DISCUSSION OF THE μA715

The μA715 is a high gain (92dB) monolithic operational amplifier that was designed to have wide bandwidth and high slew rate and thus, high output voltage capability.

It has built in output compensation and four points to which lag or lead-lag compensation can be applied. The μA715 is intended for use in A to D and D to A converters, phase locked loops, sample and holds, multiplexed analog gates, or in other application requiring wide bandwidth. Table I gives electrical characteristics of the μA715. Figure 1 shows the schematic diagram of the device and Figure 2 gives the open loop response with no compensation.

MAXIMUM STABLE GAIN AND BANDWIDTH CONSIDERATIONS

General Concepts:

The expression for overall gain for a feedback amplifier is:

$$A = \frac{-A_O}{1 + BA_O}$$

A_O = Gain without feedback
B = Feedback ratio

For the amplifier to be stable $(1 + BA_O)$ must never go negative. The only way $(1 + BA_O)$ can go negative is if the phase shift in A_O exceeds 180°, thus for a stable system A_O must fall below 0dB before the phase shift reaches 180°. These considerations are related to a typical frequency response without feedback, as shown in Figure 3. The 180° phase shift point occurs about half way down, between the second and third break points.

It must also be remembered that this is a limit condition, it corresponds to zero phase margin. In practice a designer requires at least 45° phase margin. Relating this information to the μA715, the gain with no feedback (and no compensation) is plotted in Figure 2. Minimum closed loop gain for a phase margin of 45° has been superimposed on this graph.

If it is desired to construct an amplifier with less than this overall gain, the basic amplifier characteristic must be altered such that the second break point coincides with the desired gain as shown in Figure 4.

This alteration of the basic amplifier AC performance is called compensation and is required to ensure stability. In the example just quoted, only one dominant phase lag was used to compensate the amplifier. The μA715 has four compensation points brought out on pins 1, 7, 9 and 10. Thus many compensation techniques are possible. Internal lead compensation has been supplied by the R_{21}, C_1 combination. In the amplifier design described, it is possible to empirically optomize frequency performance by observing the square wave response and adjusting the compensation for the best combination of

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rise time, overshoot and ringing. It is possible to get wider bandwidths on individual units. (Ref. 1 and 2).

A HEAD AMPLIFIER FOR AN IMAGE ORTHICON

There are many problems associated with amplifying the signal generated by an image orthicon. The most relevant of these is the frequency compensation for the frequency roll off due to the output capacitance of the image orthicon. Figure 5 shows an approximate equivalent circuit of an image orthicon and the associated input network of an amplifier.

Here, the break frequency will occur at

$$f_B = \frac{1}{2\pi RC}$$

and roll off will be at 20dB per decade.

For R = 50kΩ

$$f_B = 160\text{kHz}$$

There are two main ways to compensate for this roll off. One is to create a comparative boost in the amplifier characteristic. This is done in a great many head amplifiers today, but it has the inherent disadvantage of requiring a set up control to adjust the boost to start at the break frequency. The other approach uses an amplifier with low input impedance and high transresistance. The low input resistance swamps the effect of input capacity, and essentially all the current generated by the image orthicon flows into the amplifier. This is the approach taken in this report.

BASIC AMPLIFIER CONFIGURATION

The operational amplifier is a basic building block to construct many amplifier configurations. One such configuration that lends itself to this application is the transresistance amplifier shown in Figure 6.

$$Z_{in} = \frac{1}{\frac{1}{R1} + \frac{A_o}{R2}} = R1 \text{ in parallel with } \frac{R2}{A} \qquad (1)$$

$$\simeq \frac{R2}{A} \quad \text{if } A_oR1 >> R2$$

$$Z_{out} = \frac{1}{\frac{1}{\frac{R_o(R1+R2)}{A_oR1}} + \frac{1}{R_o}\,\frac{1}{R1+R2}}$$

$$\simeq \frac{R_o}{A_o}, \frac{R2}{R1} \quad \text{if } R1 << R2, \ \frac{R2}{R1} << A_o \qquad (2)$$

$$\text{Transresistance} = \frac{V_o}{I_{IN}} = R_T = \frac{-A_o}{\frac{1}{R_1} + \frac{A_o}{R_2}} \simeq R_2 \text{ if} \qquad (3)$$

$$R_2 >> R_1$$

$$A_oR1 >> R_2$$

CIRCUIT DIAGRAM

Figure 7 shows both the circuit diagram and the frequency response for a typical device under fixed compensation conditions. The circuit diagram shows the μA715 feeding a complementary emitter follower with overall feedback. The overall feedback resistor (R8) establishes the transresistance of the amplifier which is 51kΩ.

ISOLATION BETWEEN OUTPUTS

Isolation (cross talk) between the outputs was measured by applying a signal back into one of the outputs with zero input to the amplifier and measuring the voltage at another output. Figure 8 is a plot of these results. 40dB of isolation would correspond to an output impedance from the emitter follower of .75Ω. As can be seen from Figure 8, the degree of isolation between outputs gets less with the increase of frequency. This is due to the output impedance of the emitter follower becoming higher as the degree of feedback gets less, due to the open loop gain characteristic rolling off at higher frequencies. Equation (2) shows $Z_{out} \propto 1/A_o$ confirming this result.

NOISE

For a nominal input signal of 5mA p-p, the output is 204mV p-p. Noise at the output is about 2.0mVrms or a peak-to-peak signal to rms noise ratio of 42dB under nominal conditions.

The following applications demonstrate the μA715's ability to handle large voltage swings at the output.

40dB AMPLIFIERS – LARGE SIGNAL HANDLING CAPABILITY

The first one of these is a 40dB amplifier with 50Ω input impedance. The schematic, together with the frequency response for three levels of output, is shown in Figure 9. As can be seen from this graph, the frequency response at various levels of output is dependent on the overload capability of the μA715. A plot of maximum voltage output versus frequency is given in Figure 10.

P

This graph was obtained by observing the voltage output such that a 2dB change in voltage input produced a 1dB change in the voltage output. In essense, for large signals the bandwidth of the amplifier is limited by the overload characteristic rather than RC roll off.

NOISE PERFORMANCE

For 10V p-p output, the signal to noise ratio is about 63dB.

75Ω INPUT IMPEDANCE, WIDEBAND, 60dB AMPLIFIER

Figure 11 demonstrates a similar amplifier with 60dB of gain. The higher gain has resulted in a slightly lower bandwidth. This is due to the fact that the high frequency roll off characteristic is governed by the open loop roll off.

A 40dB, HIGH INPUT IMPEDANCE AMPLIFIER

There are many applications for wideband amplifiers with high input impedances. Such amplifiers are used with Sonar, crystal strain gauges, and in biomedical electronics. Such an amplifier with 40dB gain is shown with frequency response in Figure 12. This configuration has a very high input impedance at DC, but it falls with increase in frequency due to the input capacitance of the μA715. This restricts the available bandwidth to about 500kHz/s with a 100k source resistance. Another consequence of the high input impedance configuration is the need for an input offset control. The need for off-set control is created by the presence of input off-set current flowing through the input resistance causing an input off-set voltage. Thus, the higher the input resistance, the higher the off-set.

CONCLUSIONS

These applications for the μA715 are a few of many. They have been chosen primarily for their simplicity in illustrating the capabilities and the techniques for using the μA715.

REFERENCES

1. Fairchild Semiconductor Linear Integrated Circuits Applications Handbook.
2. Frequency Compensation Techniques for an Integrated Operational Amplifier. Fairchild Application Note APP-117, James N. Giles.

TABLE I.

Characteristics of the μA715

Absolute Maximum Ratings	
Supply Voltage	±18V
Internal Power Dissipation	500mW
Storage Temperature Range	−65°C to +150°C
Operating Range	−55°C to +125°C
Lead Temperature (Soldering, 60 sec.)	300°C
Typical Characteristics (V_S = ±15V, T_A = 25°C)	
Input Offset Voltage (Rs ≤ 10KΩ)	1.0mV typ.
Input Offset Current	70nA
Input Bias Current	400nA
Input Resistance	1MΩ
Output Resistance	75Ω
Large Signal Voltage Gain (R_L ≤ 10K, Vout = ±10V)	30,000
Common Mode Rejection	92dB
Supply Voltage Rejection Ratio	70μV/V
Power Consumption	165mW
Unity Gain Slew Rate	20V/μsec.
Unity Gain Open Loop Band Width	65MHz

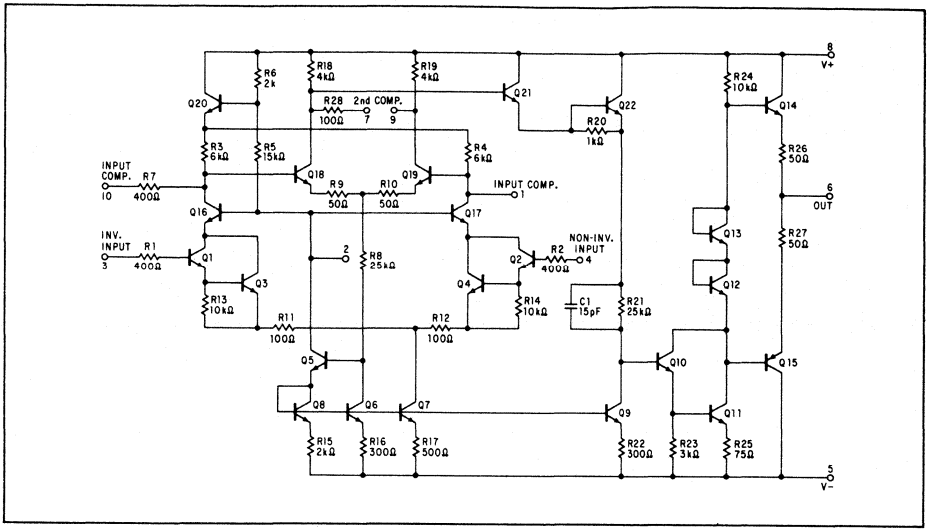


Fig. 1. μA715 schematic diagram.

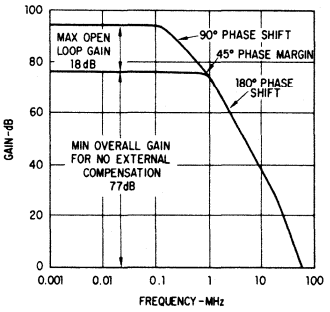


Fig. 2. Open-loop response for μA715 with no compensation.

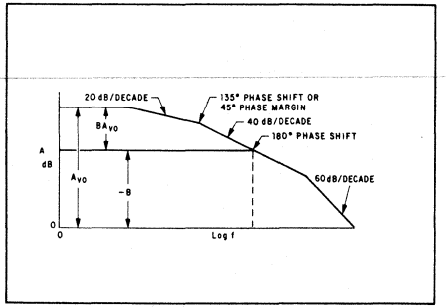


Fig. 3. Typical open-loop frequency response of an operational amplifier.

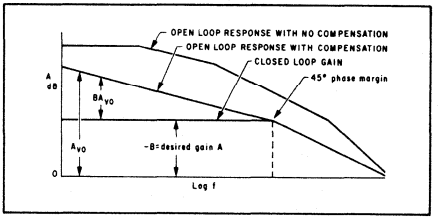


Fig. 4. Change of open-loop resporse when compensation is added.

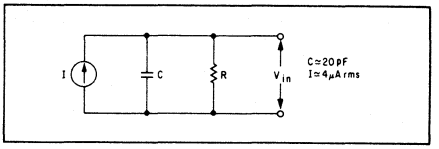


Fig. 5. Equivalent circuit of a vidicon.

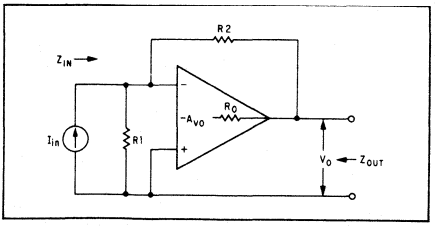


Fig. 6. Transresistance amplifier.

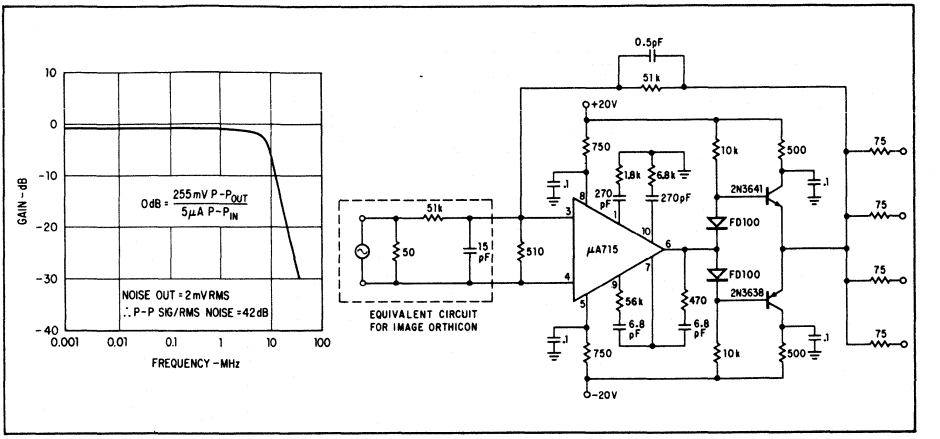


Fig. 7. Typical frequency response for image orthicon head amplifier.

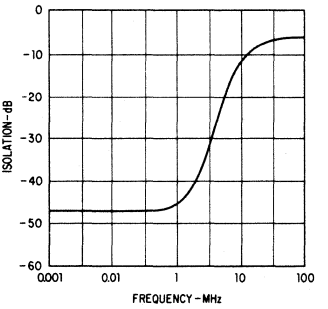


Fig. 8. Typical isolation between outputs for head amplifier shown in Figure 7.

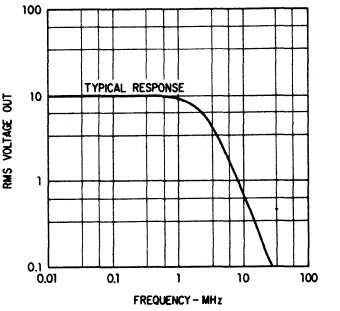


Fig. 10. Maximum output votlage vs. frequency for the amplifier in Figure 9.

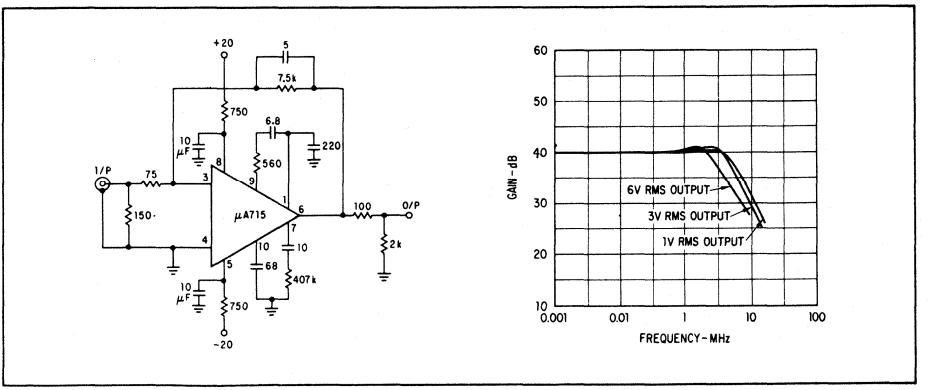


Fig. 9. A high voltage output, 40dB amplifier with 50Ω input impedance.

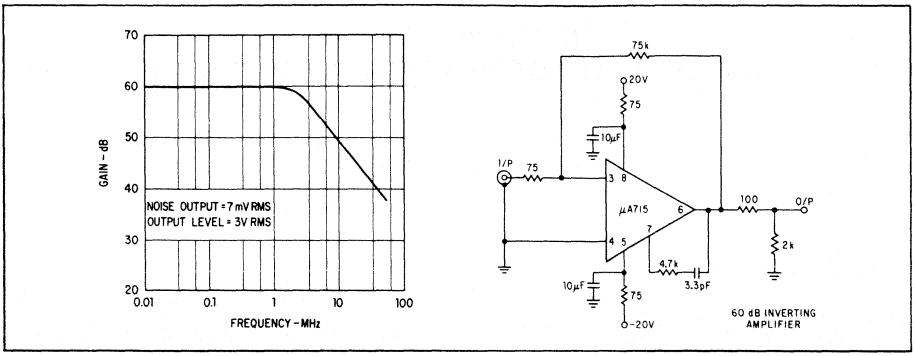


Fig. 11. 60dB inverting amplifier with 75Ω input impedance.

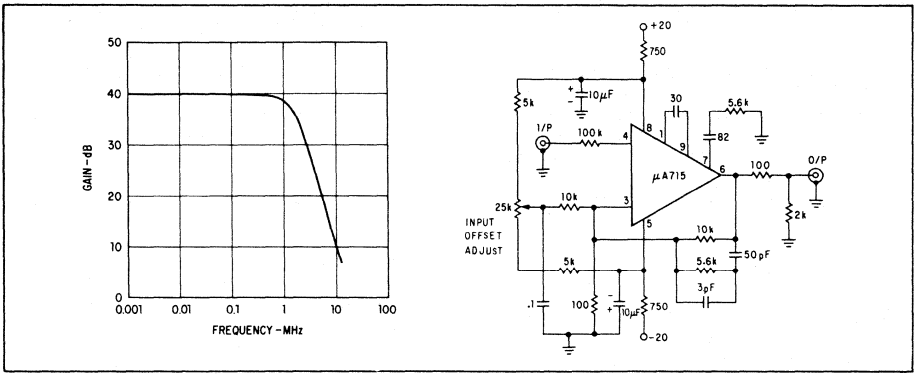


Fig. 12. 40dB non-inverting high input impedance amplifier.

A MICROPOWER MONOLITHIC OPERATIONAL AMPLIFIER

INTRODUCTION

Operational amplifiers used in telemetry and portable instrument applications should be able to deliver several milliamperes to a heavy load, but under standby conditions low battery power drain is required to ensure a reasonably long battery lifetime.

A new monolithic micropower operational amplifier, the μA735, has been designed specifically for low standby power consumption. Recent development of a low noise transistor process that provides high current gain at one microamp collector currents, and development of a compatible high value silicon-chromium resistor process paved the way to the existence of the μA735.

Some of the highlights of the μA735 performance are:

100μW standby power consumption with ±3V supplies
0.4pA/ $\sqrt{Hz}$ input current noise at 10Hz
10MΩ input impedance
Operation over a supply voltage range of ±3V to ±18V
One millivolt input offset voltage

CIRCUIT DESCRIPTION

Components

A new thin film resistor technology was developed which allows the use of resistors with individual values of up to 5MΩ and a total of over 25MΩ of resistance on a chip of reasonable size. This removes one of the basic limitations of integrated circuits, namely, the low maximum resistance (approximately 50kΩ) of diffused resistors. These thin film resistors exhibit excellent matching, good control over absolute resistance values, and have low temperature coefficients. The deposition of the thin film resistors on the silicon wafer does not degrade the performance of the planar surface underneath. As such this technique provides superior AC and DC characteristics to that of employing active loads in the input stage.

The high β transistors used feature essentially constant current gain from 1μA to 1mA collector current. As a comparison, the β of standard process transistors falls by over an order of magnitude when the current level is decreased from 100μA to 1μA.

The process developed has inherently lower noise than other processes presently employed in integrated circuits. This fact combined with the one microampere operating current levels in the input stage results in extremely low input current noise, rendering the μA735 particularly useful for operation from a high source impedance. A photomicrograph of the μA735 is shown in Figure 1.

The Input and Second Stages

The input stage relies on design simplicity and high performance NPN transistors for its excellent performance. It consists of a well-matched, large geometry input pair Q_1 and Q_2 in Figure 2 which are fed from a current source Q_3 and loaded by one megohm matched thin film resistors R_1 and R_2.

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The second stage is similar to the second stage of the μA727 and features a composite PNP/NPN differential pair Q_7, Q_8, Q_9, and Q_{10}. R_{10} stabilizes the voltage gain making it almost independent of operating current levels and ambient temperatures. Emitter followers Q_5 and Q_6 are used to prevent loading of the input stage. The combination of Q_{11} and Q_{12} retains the full differential gain of the second stage while providing the differential to single-ended signal conversion.

The Output Stage

The most stringent restrictions in the design of a micropower operational amplifier occur at the output stage. With ±3V supplies, the operating current in the driver transistor Q_{13} varies from zero to 4μA, while the output transistors Q_{20} and Q_{21} deliver in excess of 2mA under load. Therefore, Darlington-connected output pairs are used to properly isolate the output from the driver and to prevent the reduction of voltage gain and output swing. Because of the micropower nature of the amplifier, the idling current in the output transistors Q_{20} and Q_{21} is limited to 4μA. This current level is determined by a chain of four diodes. The output resistance, R_{out} of the emitter followers is given by:

$$R_{out} = \frac{kT/q}{\sqrt{I_L^2 + 4\,I_i^2}} \qquad (1)$$

where I_L is the current delivered to the load and I_i is the idling current with $I_L = 0$. Therefore, with $I_i = 4\mu A$ and $I_L < I_i$, R_{out} is 3kΩ. This large output resistance (compared to a 1k load) would reduce the open loop gain significantly at low load currents and cause degradation in harmonic distortion of the output waveform. To improve this situation, feedback resistor R_{14} is used to decrease R_{out} by the loop gain of the output stage to approximately 100Ω.

FREQUENCY RESPONSE

The frequency performance of any micropower operational amplifier will be inferior to a general purpose amplifier operating at higher current levels. The causes of the bandwidth reduction are:

(1) The f_T's of the transistors are significantly less at the microampere level than at higher currents.

(2) To obtain the high gain necessary for operational amplifiers, the load resistors for the individual stages are in the megohm range. A 1MΩ resistor in parallel with an 8_pF capacitor gives a pole at 20kHz. The equivalent capacitance at any of the high impedance nodes can easily exceed 8_pF. [1]

The open-loop and closed-loop frequency response curves are shown in Figure 3 and 4. For closed-loop gains of one and ten both input and output compensation is used. For these configurations, the initial low frequency roll-off is provided by C_1. At about 2kHz, the zero furnished by the R_1–C_1 combination stops the input stage attenuation and the output stage pole, due to C_2, takes over.

In the 100 and 1000 closed loop gain configurations one has three alternatives: (1) input compensation only, (2) output compensation only, (3) both input and output compensation. The use of R_1 and C_1 only has the maximum bandwidth but has poorer noise figure. Compensation with R_2 and C_2 only, result in a narrower bandwidth but lower noise amplifier. In order to ensure the bandwidth indicated with R_1, C_1 compensation only in the 1000 closed-loop gain configuration, the stray capacitance between pins 6 and 8 must be minimized.

Table I summarizes recommended compensation values for operation with both ±3V and ±15V supplies. For operation with supplies in between those given, the component values should be interpolated or the conservative ±15V values should be used.

PERFORMANCE

The μA735 features very low power compensation, high input impedance, low temperature drift, low offset voltage, low offset currents, and low noise. It has excellent common mode and power supply rejection, excellent temperature stability and will operate over a wide range of supplies. Performance details are presented in Table II.

CONCLUSIONS

New developments in integrated circuit processing have made the construction of the μA735 possible. Its characteristics, in general, are equivalent to or better than the performance of other general purpose operational amplifiers. The μA735's low standby power consumption and input current noise are unmatched by any other monolithic operational amplifier.

Note 1: At pin 8, for example, the equivalent capacitance is the sum of the collector-substrate capacitance of Q_2, the collector-base and base-emitter capacitances of Q_5, and the stray capacitances from pin 8 to pin 5 and from pin 8 to pin 6, multiplied by the voltage gains from pin 8 to pins 5 and 6, respectively. Active loads more than double this capacitance in addition to adding excessive phase shift from emitter transistion capacitance.

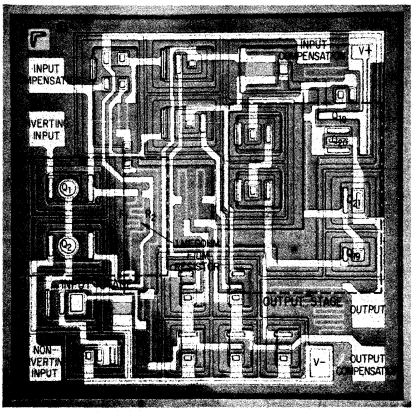


Fig. 1. Photomicrograph of μA735.

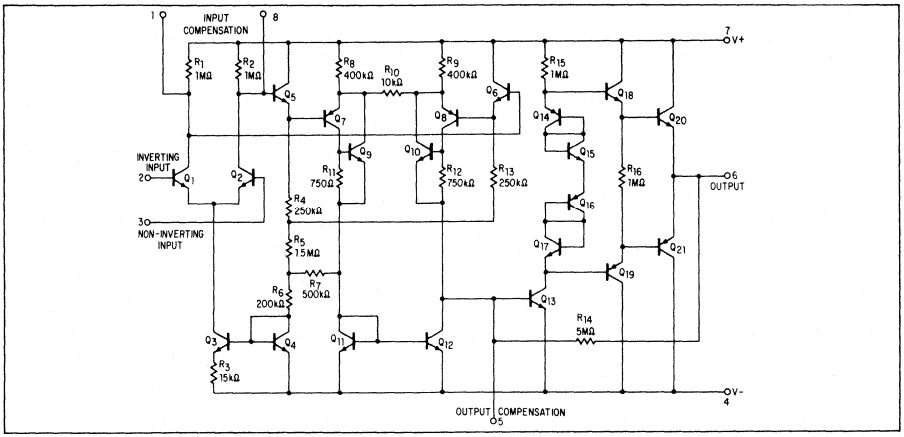


Fig. 2. Equivalent circuit.

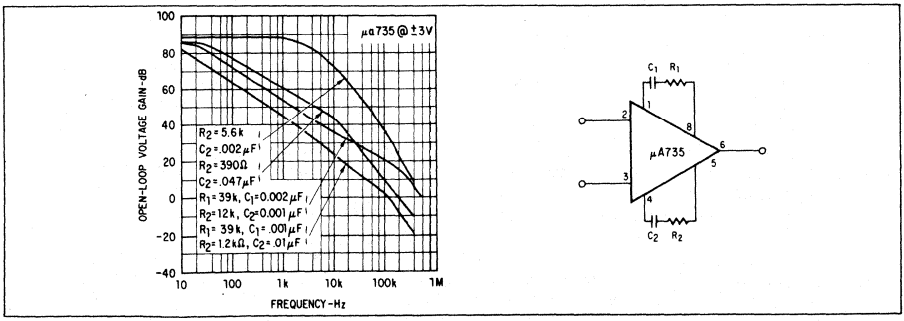


Fig. 3. Open-loop response for various values of compensation.

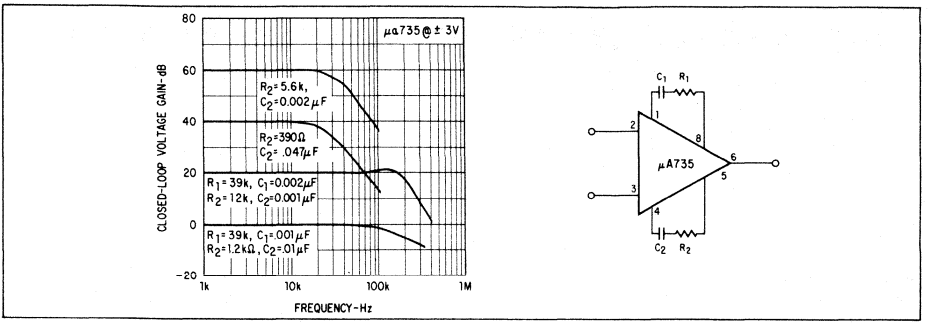


Fig. 4. Frequency response for various closed-loop gains.

TABLE I

μa735 Frequency Compensation

CLOSED-LOOP GAIN	Vs	R_1	C_1	R_2	C_2	C_3
1	± 3	39k	.001μF	1.2kΩ	.01μF	
1	±15	39k	.02μF	100Ω	.0047μF	220pF
10	± 3	39k	.002μF	12k	.001μF	
10	±15	39k	.002μF	1k	180pF	22pF
100	± 3	—	—	390Ω	.04μF	
100	±15	39k	2.20pF	1k	180pF	22pF
1000	± 3	—	—	5.6k	.002μF	
1000	±15	56k	82pF	short	10pF	

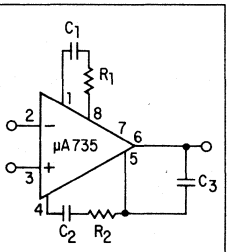


TABLE II

μA735 Typical Electrical Characteristics

	V_S = ±3V	V_S = ±15V
Input Offset Voltage	1mV	1mV
Input Offset Current	2nA	4nA
Input Bias Current	5nA	10nA
Input Resistance	10MΩ	5MΩ
Common Mode Rejection Ratio	90dB	90dB
Power Supply Rejection Ratio	50μV/V	50μV/V
Large Signal Voltage Gain	20,000	40,000
Output Voltage Swing	±1.2V	±12V
Power Consumption	100μW	6mW

THE μA746E COLOUR TV CHROMA DEMODULATOR IC

INTRODUCTION

The μA746E is a monolithic chroma demodulator integrated circuit (IC) for NTSC color TV receivers. Before describing the design of the μA746E, it may be instructive to begin this paper with a brief review of that portion of the NTSC color TV system which relates to the requirements and operation of a chroma demodulator. This will lead into a discussion of the μA746E.

NTSC COLOR TV SYSTEM

The video signal in a color TV broadcast originates from three cameras which are each sensitive to only one of three colors; green, red, or blue. The outputs of the three cameras are added to form a monochrome (luminance) signal in accordance with the following relationship:

$$E_Y = 0.59E_G + 0.30E_R + 0.11E_B$$

where E_Y is the luminance signal and E_G, E_R, and E_B are the three color signals. (The particular contributions of green, red, and blue, 59%, 30%, and 11% respectively, were selected to correspond to the color sensitivity of the human eye. When green, red, and blue light energy is combined to produce what appears to be white to the eye, these same rays, when viewed separately, are not seen by the eye as having the same brightness as might be expected. Rather, green appears twice as bright as red, and between six and ten times as bright as blue.)

The three color signals, E_G, E_R, and E_B are reconstructed in the color TV receiver to drive a color picture tube having three guns, each of which activates only green, red, or blue phosphor dots.

The E_Y signal (luminance) is transmitted as a normal video signal as in a black and white (monochrome) TV broadcast. Color information is carried in the form of color-difference signals on a 3.58MHz-suppressed-carrier subcarrier which is spectrally interleaved with the monochrome signal. Rearranging the luminance expression given above, color difference signals are as follows:

$$E_G - E_Y = 0.41E_G - 0.30E_R - 0.11E_B$$

$$E_R - E_Y = -0.59E_G + 0.70E_R - 0.11E_B$$

$$E_B - E_Y = -0.59E_G - 0.30E_R + 0.89E_B$$

Note that any one of the color-difference signals can be expressed in terms of the other two. For example,

$$E_G - E_Y = -0.51\,(E_R - E_Y) - 0.19\,(E_B - E_Y).$$

This shows that all of the color information can be carried as two color-difference signals (along, of course, with the E_Y signal which is also transmitted.)

The means by which color is carried on a chroma subcarrier can be explained on the basis of $E_R - E_Y$ & $E_B - E_Y$ color-difference signals. The $E_R - E_Y$ and $E_B - E_Y$ signals (after appropriate correction for picture tube characteristics) are fed into separate balanced modulators to modulate two 3.58MHz-subcarriers that are phased in quadrature. The suppressed-carrier outputs of the two modulators are added to form one signal which is commonly referred to as the chroma subcarrier or simply as chroma. The chroma subcarrier can also be described as a suppressed-carrier signal whose amplitude and phase varies according to the saturation and hue, respectively, of the color being transmitted. A phase diagram of the NTSC

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chroma subcarrier is shown in Figure 1.

By synchronous detection of the chroma subcarrier, it is possible to extract color-difference signals, E_G - E_Y, E_R - E_Y, E_B - E_Y, (or any other color-difference signals) by appropriate phasing of the regenerated subcarrier reference signal which is injected into the synchronous detector. (The injected reference signal is obtained from a 3.58MHz-crystal oscillator which is phase-locked to the color burst that is transmitted during horizontal retrace.) As explained earlier, all of the color information is contained in two color-difference signals. Therefore, it is only necessary in the receiver to recover any two color-difference signals. A common approach to chroma subcarrier demodulation is to do basically just that; E_R - E_Y and E_B - E_Y signals are extracted by synchronous detection in two detectors and the E_G - E_Y signal is obtained by adding together appropriate amounts of inverted E_R - E_Y and E_B - E_Y. Alternatively, of course, three synchronous detectors can be used to obtain the three color-difference signals directly.

In actual practice, today's color TV receivers do not demodulate the chroma subcarrier to obtain the exact color-difference signals, E_G - E_Y, E_R - E_Y and E_B - E_Y, which are transmitted according to NTSC standards. Deviations from standard NTSC demodulation angles and relative gains have been necessary to obtain pleasing pictures with present day picture tubes which have green and blue phosphor chromaticity coordinates that differ significantly from those which existed when NTSC standards were originally written. Based on work by Parker (Reference 1), Figure 2 shows the particular set of demodulation angles and relative gains which were selected for the μA746E and its predecessor, the μA737E (Reference 2).

Following demodulation, color-difference signals, E_G - E_Y, E_R - E_Y, and E_B - E_Y are amplified and combined with the luminance signal, E_Y, to obtain E_G, E_R, and E_B drive for the guns of the color picture tube.

μA746E CHROMA DEMODULATOR IC

Figure 3 is a block diagram of the μA746E chroma demodulator. Two synchronous detectors extract normal and inverted E_R - E_Y and E_B - E_Y signals from the chroma subcarrier. (In Figure 3 and hereafter, the chroma subcarrier is reffered to simply as chroma.) The matrix sets the relative gain of E_R - E_Y to E_B - E_Y and adds the inverted E_R - E_Y and E_B - E_Y signals in the correct proportion to produce E_G - E_Y. Demodulation angles and relative gains shown in Figure 2 are obtained when the injected reference "A" and reference "B" signals are applied at phasings of 3 degrees and 106 degrees, respectively. (Burst phase is 180°.) Variations in demodulation angles and relative gains as a function of reference "B" are shown in Figure 4. The curves of Figure 5 show the demodulation linearity and output capability of the μA746E. The non-critical reference amplitude requirements are illustrated in Figure 6.

Examining the μA746E in more detail, Figure 7 shows the basic circuit of one of the doubly-balanced synchronous detectors (balanced to both reference and chroma signals). Opposite-phase chroma signals from the differential amplifier, Q_E and Q_F, are supplied to the transistor switches, Q_A through Q_D. The switches are controlled by a reference signal which is applied to the bases of Q_A and Q_D. Chroma signal currents from the differential amplifier flow into one or the other outputs depending upon the instantaneous state of the individual switches. A study of the synchronous detection process, which is illustrated graphically by the waveforms in Figure 8, shows the detector's sensitivity to both phase and amplitude of the chroma signal. (As mentioned previously, in the NTSC color TV system, phase and amplitude of the chroma signal carry hue and saturation information, respectively.) The doubly-balanced arrangement in the detector provides cancellation of the reference signal, thus eliminating the need for elaborate filtering at the outputs of the μA746E.

The complete schematic of the μA746E integrated circuit is shown in Figure 9. The chroma signal is fed into the parallel connected inputs of the differential amplifiers; Q_{11} and Q_{12}, and Q_{13} and Q_{14}. Reference (color oscillator) signals, which are equal in frequency, but at different phases, are applied to the two sets of switch transistors Q3 through Q6, and Q7 through Q10. A regulated 6-volt supply for the switch transistors is formed by zener diode D_2 and transistor Q_1. This supply is resistively divided and applied to the base of transistor Q_2 to establish a 3-volt supply for the differential amplifiers. Current source transistors, Q_{16} and Q_{17} are controlled by the diode-connected transistor, Q_{15}, which is biased from the supply through zener diode D_1 and a 16kΩ dropping resistor. The current in Q_{16} and in Q_{17} is twice that which flows in Q_{15} due to the two-to-one resistance ratios of the resistors in the emitters of these transistors.

The two outputs from each of the two synchronous detectors are applied to a resistive decoder

matrix where color-difference signals are developed. The particular configuration and design of the matrix was developed to fulfill four primary requirements.

1) The matrix must develop the desired color-difference signals shown in Figure 2.

2) The matrix must not require an unreasonably large chip area (the total resistance of the matrix must be limited).

3) The matrix must have a high-level output signal capability sufficient to drive either vacuum tube or transistor video output amplifiers.

4) The outputs from the matrix, when no chroma signal is applied, must be at equal d-c voltage levels to permit operation in direct-coupled video systems.

These requirements have been met by the matrix in the μA746E. As a compromise between total matrix resistance and output capability, and with the condition that the no-signal d-c output voltage levels must be equal, the maximum capability was made 15 percent less than would have been possible had no consideration been given to total resistance. This compromise in output capability resulted in significant savings in chip area.

The color-difference output voltages from the matrix are fed through emitter follower transistors, Q_{18}, Q_{19}, and Q_{20}. Integrated 250-ohm resistors at each output offer protection against damage from accidental short circuits. To minimize internal power dissipation, the load resistors for the emitter follower transistors are not included on the chip.

The monolithic integrated chip of the μA746E shown in Figure 10 is 50 x 50 square mils. The differential amplifiers are located in the lower right side of the chip; directly above are the switch transistors. The matrix resistors which are in the main isolation region occupy the upper left side of the chip. Adjacent to the matrix on the extreme left side of the chip are the three emitter follower output transistors. Biasing circuitry for the detectors is located in the lower left corner of the chip.

The μA746E chip is assembled in a 9-pin, epoxy covered, ceramic base package, shown in Figure 11, which plugs into standard 9-pin minature tube sockets. Alternatively, the package can be soldered directly into printed circuit boards when this is preferred to socket insertion.

IMPROVEMENTS IN THE μA746E

The improvements in the μA746E relate to its static (DC) characteristics and are of primary benefit in receiver designs that utilize direct-coupled chrominance output amplifiers. The dynamic (AC) performance of the μA746E is unchanged from the μA737E.

The improved biasing network that has been incorporated into the μA746E provides the following advantages for receivers employing direct coupling in the chrominance output amplifiers:

1) Fractional Supply Tracking

The DC output voltages of the μA746E change approximately one-half-volt for a one-volt change in supply voltage, whereas the μA737E output voltages directly track the supply voltage. Fractional supply tracking eases design problems associated with brightness changes in the picture tube due to supply voltage variations.

2) Low Drift

The DC output voltages of the μA746E are very stable with temperature. Drift is typically only -0.3mV/°C which ensures that the chroma demodulator will not be a contributor to brightness change in the picture tube during receiver warm-up.

3) Uniform DC output Voltages

The DC difference voltage between any two outputs, as well as the absolute variation in DC output voltages from device-to-device are both less in the μA746E than in the μA737E. This feature simplifies set-up controls.

CONCLUSION

The μA746E is a chroma demodulator IC which contains two doubly-balanced synchronous detectors and a decoder matrix which produces color-difference signals for NTSC color TV receivers. The excellent static (DC) characteristics of the μA746E makes it well suited to all receiver designs including those which employ direct-coupled chrominance output amplifiers.

REFERENCES

1) N. W. Parker, "An Analysis of the Necessary Decoder Corrections for Color Receiver Operation with Non-Standard Receiver Primaries", IEEE Transactions on Broadcast and Television Receivers; April 1966.

2) Blaser, Bray, and Rennick, "A Monolithic Chroma Demodulator Integrated Circuit for Color Television Receivers", IEEE Transactions on Broadcast and Television Receivers; October 1968.

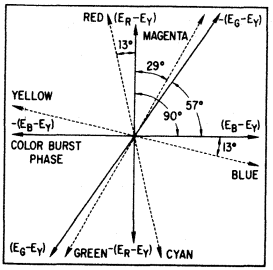


Fig. 1. Chroma subcarrier phrase diagram.

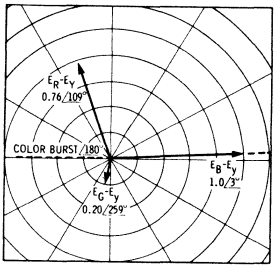


Fig. 2. Demodulation angles and relative gains.

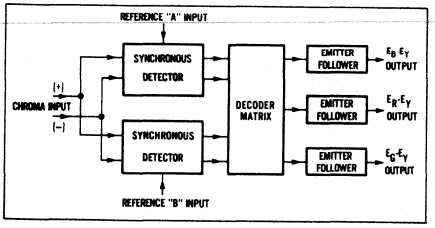


Fig. 3. μA746E block diagram.

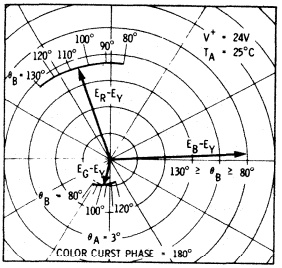


Fig. 4. Demodulation sensitivity to relative phasing of reference signals.

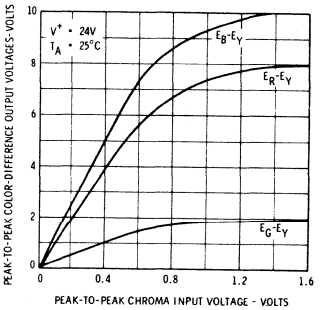


Fig. 5. Demodulation linearity.

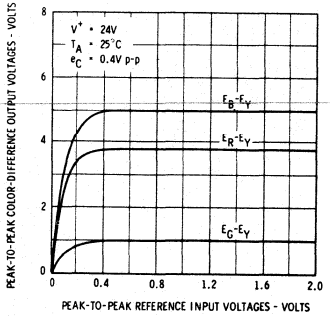


Fig. 6. Demodulation sensitivity to amplitude of reference signals.

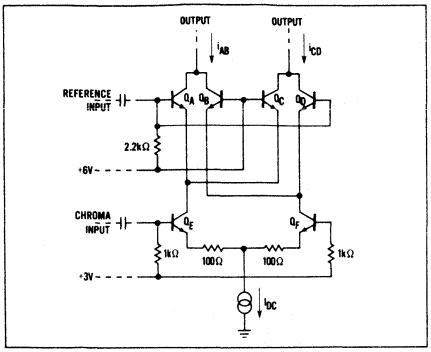


Fig. 7. Synchronous detector.

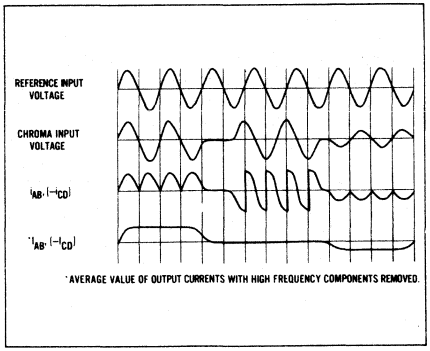


Fig. 8. Synchronous detector waveforms.

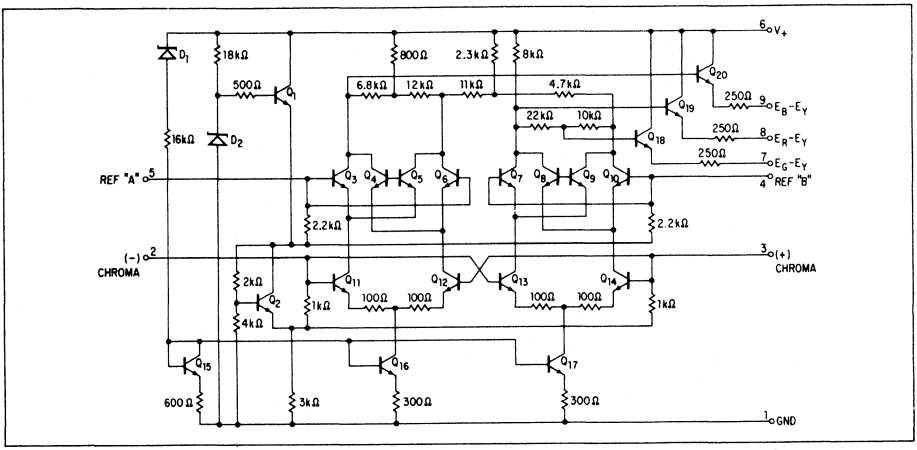


Fig. 9. μA746E chroma demodulator.

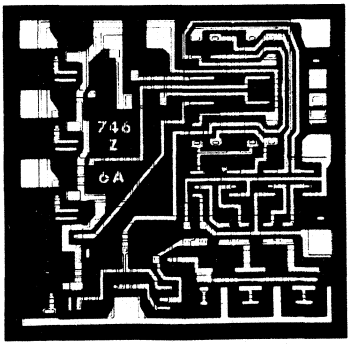


Fig. 10. Photomicrograph of μA746E.

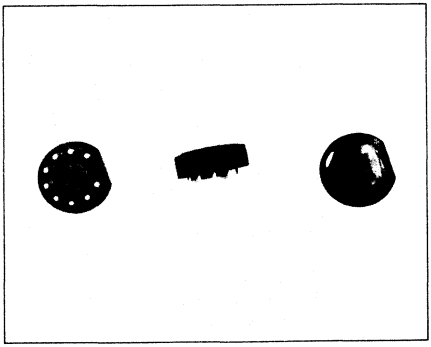


Fig. 11. Chroma demodulator package.

APPLICATIONS OF THE μA749 DUAL OPERATIONAL AMPLIFIER

DUAL COMPARATOR

The μA749 differs from most operational amplifiers in that the output stage is a class A common emitter PNP transistor circuit as shown in Figure 1. Although this raises the output resistance for negative going outputs, it does provide several advantages. One of these is the ability to OR the outputs of the two amplifiers by simply joining them together. When either output transistor is turned on, the output will be high. This technique is used in the dual level comparator shown in Figure 2. The circuit will operate with supply voltages from ±4 to ±15 volts. At ±4 volts, the power drain from the supply is typically only 30mW.

Strobing can be achieved by connecting the output lag pin to a voltage within 0.5 volts of the positive supply. The two outputs can thereby, be independently strobed. The turn-off delay for ±15 volt supply is typically 350ns. This is largely a function of the storage time of the output PNP transistor. One way in which this may be reduced is by shunting the second stage load resistor with a resistor of about 10kΩ, which reduces base drive to the output transistor but also reduces gain. A better way to decrease storage time is to connect two diodes in series across the second stage load resistor. These diodes conduct only when the output transistor saturates, therefore, small signal gain is not affected. For commercial applications where strobing is not required, cost savings can be realized by use of the μA749D.

The output load resistor need not be returned to the negative supply as shown in Figure 2. It may be returned to any desired reference voltage within the output range of the μA749. In the off state, the output voltage will then be equal to the reference voltage.

PEAK DETECTORS

The Class A output stage of the μA749 permits the device to be used as a peak voltage detector, without requiring the use of external diodes, as shown in Figure 3. When the input voltage exceeds the capacitor voltage, the output transistor turns on and charges the capacitor until the inverting input voltage reaches the input voltage. The output transistor is then turned off. During capacitor charge, the circuit operates as a unity gain voltage follower with the capacitor providing frequency compensation. When the input signal falls below the capacitor voltage, the output device is held off and the only drain on the capacitor is the amplifier input current which is typically less than 1μA. Unlike most operational amplifiers, the μA749 will not pull current out of the capacitor, therefore, a discharge resistor may be required across the output. The value of the resistor will depend upon the sampling rate.

A detector for negative peaks is shown in Figure 4. Again the circuit acts as a voltage follower for inputs more negative than the capacitor's positive voltage. The output is, therefore, a positive voltage equal to the negative of the peak input voltage shifted positive by 2 x V_{ref}.

The two peak detectors described above may be combined as in Figure 5 to create a peak-to-peak detector. In this circuit the reference voltage for the negative peak detector B is taken from the output of the positive peak detector A. During capacitor charge amplifier B has a gain of two from

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the non-inverting input. Therefore, the input to the positive peak detector must be divided by two so that its output will be $1/2V_{pos}$. The negative peak will then fall $V_{neg} + 1/2V_{pos}$ below the reference to the second stage. The output from this stage will then be $V_{neg} + 1/2V_{pos}$, which is exactly the peak-to-peak value of the input.

For low input signal levels, the amplifier input offset voltage may cause a significant error. This error may be eliminated by means of the offset null circuit shown in Figure 6. If this option is not required, the 8-pin μA749D may be employed.

CONCLUSION

The circuits described show how the unique output stage of the μA749 expands its versatility beyond that of a regular operational amplifier. It is ideally suited to use as a level comparator, peak detector, absolute value amplifier, etc., where it will reduce the number of additional parts compared with most operational amplifiers.

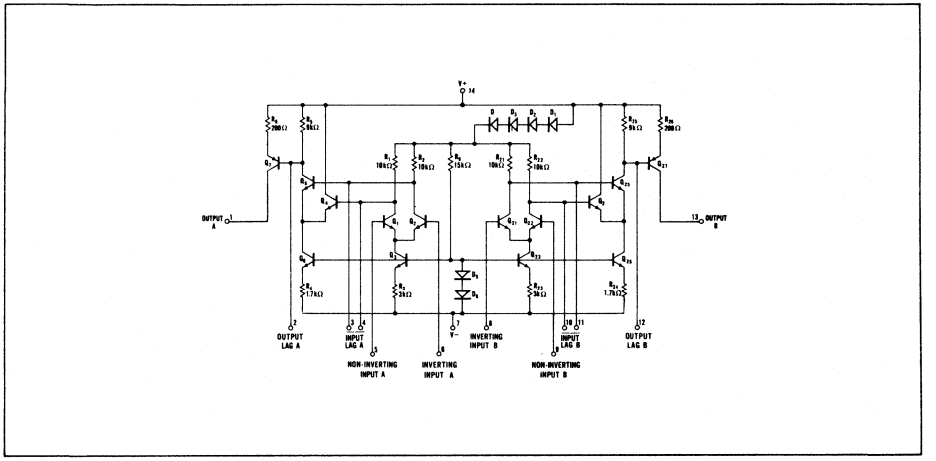


Fig. 1. μA749 schematic.

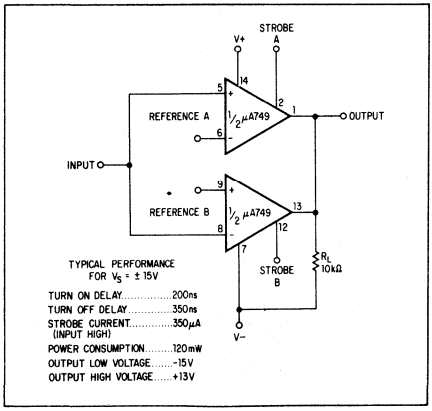


Fig. 2. Dual level comparator.

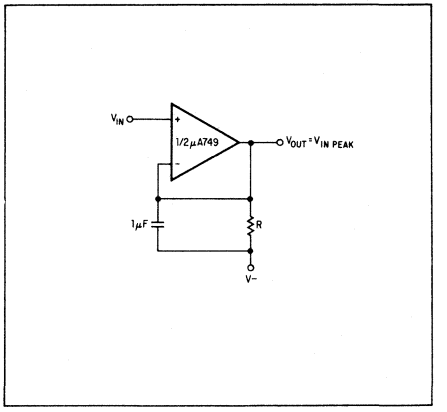


Fig. 3. Positive peak detector.

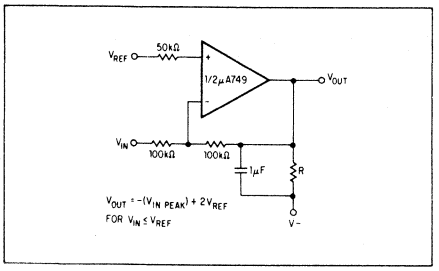


Fig. 4. Negative peak detector.

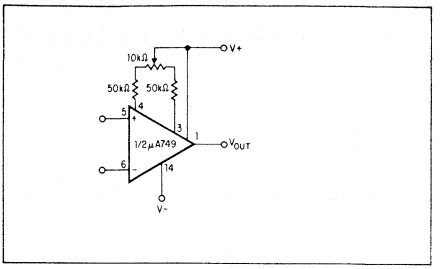


Fig. 6. Offset null circuit.

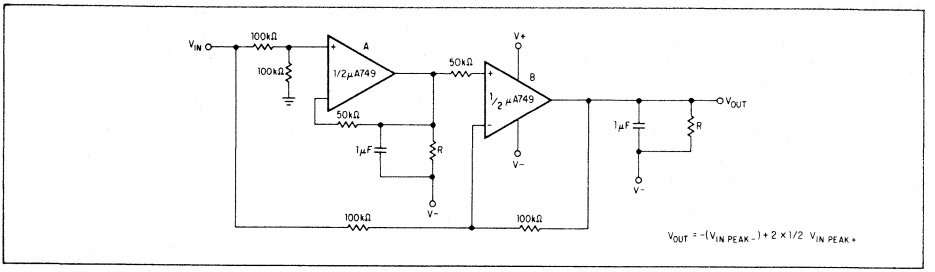


Fig. 5. Peak-to-peak detector.

THE μA749 DUAL OPERATIONAL AMPLIFIER

CONTENTS

Input stage, second stage, output stage, biasing, performance, frequency compensation, compensation points, recommended networks, output capability, supply voltage and temperature effects, general precautions, common mode range, differential input voltage, supply voltage polarity, maximum supply voltage, output short circuit, low voltage operation, typical application.

The μA749 is a dual high gain operational amplifier constructed on a single chip using the planar* epitaxial process. It is useful as a general purpose DC or AC amplifier at frequencies up to 20MHz wherever two or more amplifiers are required.

The circuit features high output swing, stable characteristics over a wide range of supplies and good noise performance. Typical applications include buffered oscillator or multivibrator, dual comparator, stereophonic audio amplifier, pulse-width modulator, active filter, peak-to-peak detector, core memory sense amplifier, etc.

*Planar is a patented Fairchild process.

CIRCUIT DESCRIPTION

The complete schematic is shown in Figure 1. It is seen to be composed of two identical amplifiers with a common DC bias circuit. Each amplifier is composed of three stages: Stage one is a simple emitter-coupled differential stage with transistor current source. The second stage is also a current sourced emitter-coupled pair driven differentially by the first stage providing a single ended output for the Class A, common emitter PNP output stage which provides the level shifting required. Stage three, the output stage, is composed of a lateral PNP transistor and an NPN device as shown in Figure 2. The h_{FE} of integrated lateral PNP devices is low (typically 1-50), so it is necessary to augment the current gain by means of an NPN transistor. The effect is to produce a PNP transistor with h_{FE} approximately equal to the product of the h_{FE}'s of the PNP and NPN transistors. This combination is known as a "composite PNP" and is widely used in integrated circuits.

R_7 is added between emitter and base of the NPN transistor Q_{7B} in order

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to increase the PNP collector current to a level of higher h_{FE} and also to improve the speed of the composite structure. The output stage is completed by external load resistor R_L.

DC bias for the current sources is provided by diodes D_5 and D_6 which are forward biased by the current flowing through R_9 and D_1-D_4 from the positive supply. Due to tne logarithmic character of the V_{BE}/I_C relationship, the potential at Y remains relatively constant for a wide range of supply voltages. The result is that each of the current source emitter resistors has a voltage of one V_{BE} imposed across it. Taking $V_{BE} = 0.6V$, the first stage current source is readily calculated to provide a current

$$I_3 = \frac{V_{BE}}{R_3} = \frac{0.6}{3k} = 200\mu A$$

Similarly, the second stage current source provides a current

$$I_6 = \frac{V_{BE}}{R_4} = \frac{0.6}{1.7k} = 350\mu A.$$

In normal quiescent conditions, the current in the input stage divides equally between Q_1 and Q_2 so that each carries 100μA.

The intrinsic dynamic emitter resistance is given by:

$$r_e = \frac{kT}{qI_e}$$

where:

k = Boltzman's constant
T = Absolute temperature
q = Electron charge
I_e = Emitter current

At room temperature, this becomes:

$r_e = \frac{25}{I_e}$ where I_e is given in milliamperes.

For the first stage then,

$$r_{e_1} = \frac{25}{Ie} = \frac{25}{0.1} = 143\Omega$$

Similarly for the second stage,

$$r_{e_2} = \frac{25}{.175} = 143\Omega$$

The differential gain of the first stage is given by

$$A_{V_1} = \frac{R_L}{r_{e_1}}$$

where R_L is the parallel combination of the load resistors and the second stage input resistance.

Input resistance of second stage $\approx \beta r_{e_2} \approx 16k\Omega$

Load resistance (R_1 and R_2) = 10kΩ

$$R_{L_1} \approx 6.2k\Omega$$

$$A_{V_1} \approx \frac{6.2 \times 10^3}{250} = 25$$

The gain of the second stage is given by $1/2 \frac{R_L}{r_{e_2}}$.

(The factor of 1/2 is required for single-ended output.)

Input resistance of the third stage $\approx \beta$ (Q_7) x $R_6 \approx 40k\Omega$

load resistance (R_5) = 9kΩ

$$R_{L_2} \approx 7.4k\Omega$$

$$A_{V_2} \approx 1/2 \times \frac{7.4 \times 10^3}{143} = 26$$

The output stage gain is given by the ratio R_L/R_6, and in this case

CIRCUIT DESCRIPTION

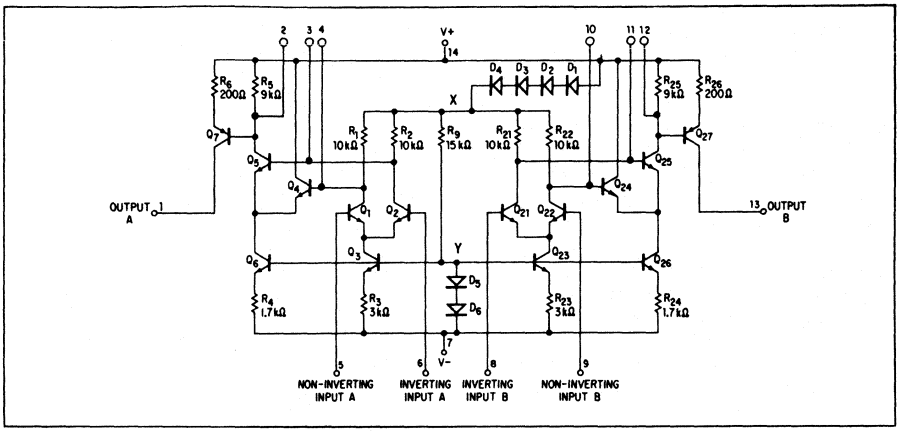


Fig. 1. μA749 schematic.

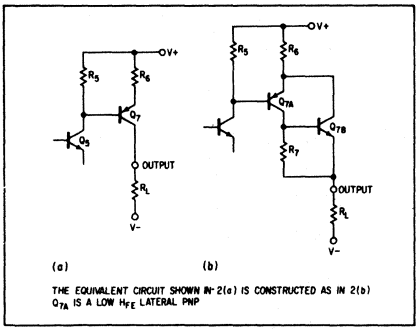


Fig. 2. μA749 output stage.

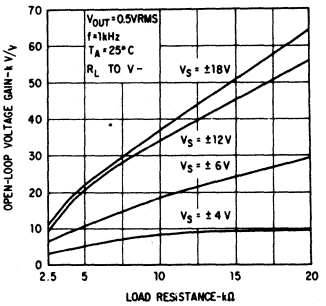


Fig. 3. Open-loop voltage gain as a function of load resistance.

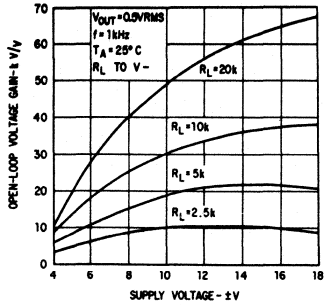


Fig. 4. Open-loop voltage gain as a function of supply voltage.

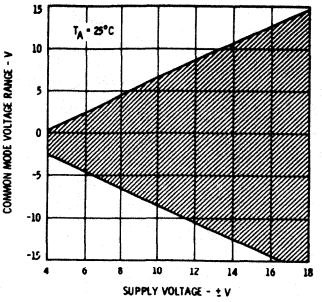


Fig. 7. Common mode range as a function of supply voltage.

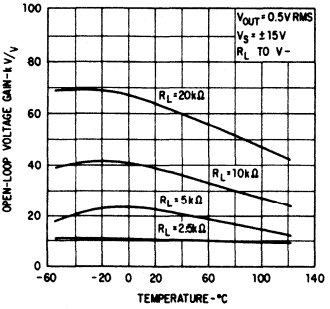


Fig. 5. Open-loop voltage gain as a function of temperature.

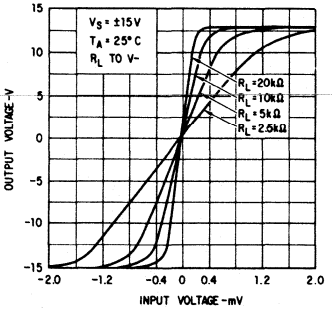


Fig. 6. Open-loop DC transfer characteristics.

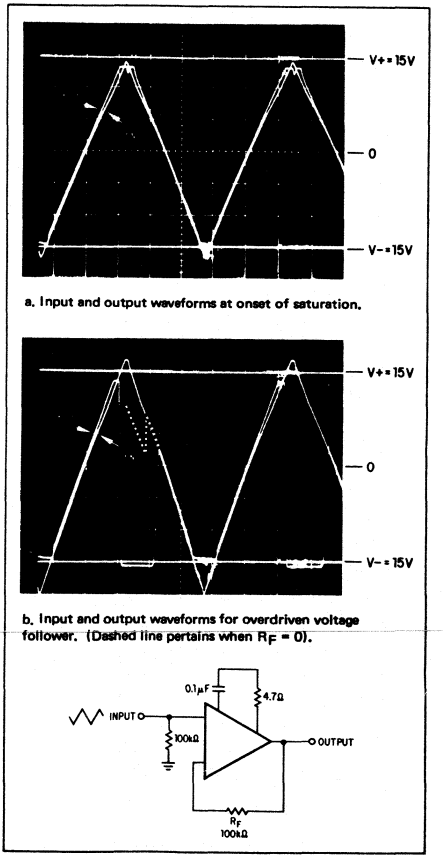


Fig. 8

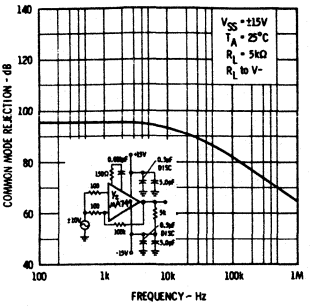


Fig. 9. Common mode rejection as a function of frequency.

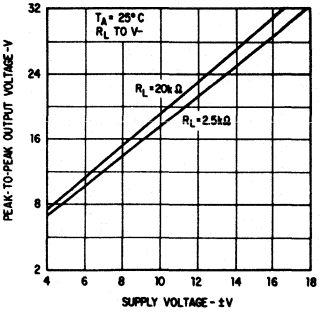


Fig. 12. DC output voltage capability as a function of supply voltage.

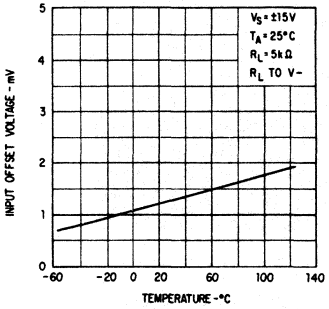


Fig. 10. Input offset voltage as a function of temperature.

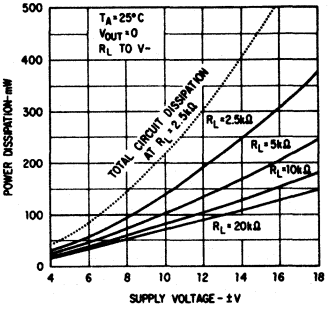


Fig. 13a. Device power dissipation as a function of supply voltage and load.

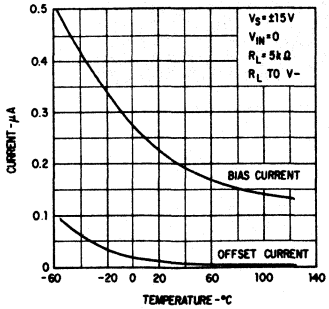


Fig. 11. Input offset current and bias current as functions of temperature.

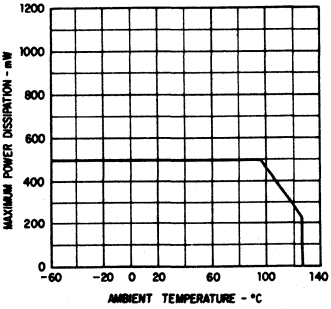


Fig. 13b. Maximum dissipation as a function of ambient temperature.

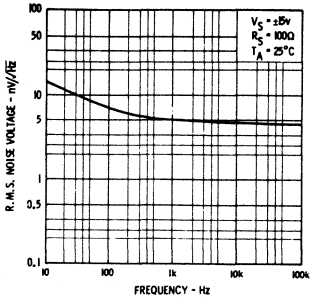


Fig. 14. Input noise voltage as a function of frequency.

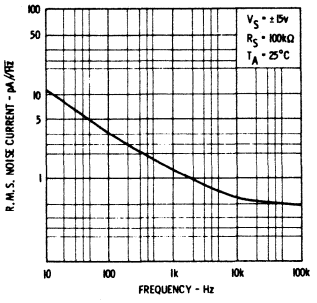


Fig. 15. Input noise current as a function of frequency.

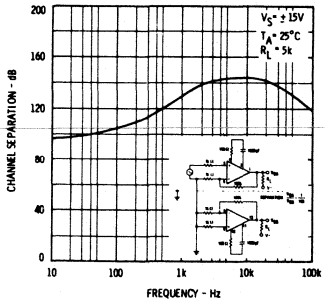


Fig. 16. Channel separation as a function of frequency.

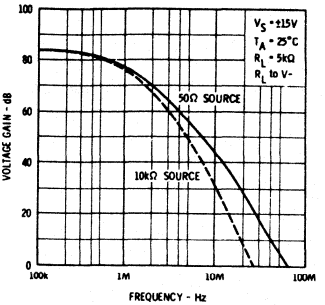


Fig. 17. Uncompensated open-loop frequency response.

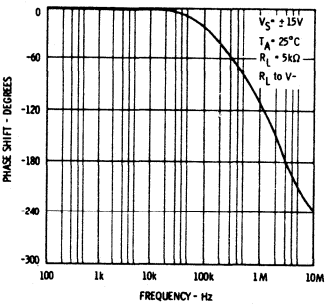


Fig. 18. Open-loop phase shift without compensation.

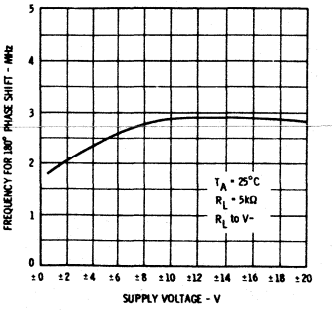


Fig. 19. Open-loop 180° phase shift frequency as a function of supply voltage.

$$A_{V_3} = \frac{5 \times 10^3}{200} = 25$$

Total gain from input to output is, therefore:

$$A_{V0} = 25 \times 26 \times 25 = 16,250 \text{ or } 84\text{dB (Typical)}$$

Note that the gain of the first two stages is relatively constant for wide variations in absolute value of the individual resistors in the circuits. This comes about owing to the proportionality of intrinsic emitter resistance to emitter current, which is in turn inversely proportional to the value of the resistor in the emitter of the current source. Therefore, the gain of the first two stages is determined by the ratio of the current source resistor value to the collector load resistance.

The output stage gain is, however, determined by the ratio of the external load resistance to the internal resistor R_6. The gain will therefore vary with the absolute value of R_6 which may have a spread of approximately $\pm 30\%$. The gain will also be somewhat dependent of the β's of the transistors in the circuit. The data sheet should be consulted for the guaranteed minimum gain.

Figures 3, 4, and 5 show the typical variations of the open loop gain as a function of external load resistance, power supply voltage and temperature.

At this point, it is appropriate to explain the function of the diodes D_1 through D_4.

Consider the DC bias conditions when the output stage is providing say, 10mA into the load. This current will pass through R_6 producing a voltage drop across it of 2 volts. Q_7 is necessarily turned on in these conditions so that its base will be approximately 2.6 volts below the positive supply. To avoid saturation of Q_5, its base must not be significantly higher in potential than its collector. The differential voltage applied to the input of the second stage will be only a few millivolts so that the voltage drop across R_2 will be approximately $100 \times 10^{-6} \times 10^4 = 1$ volt. Therefore, to avoid saturation of Q_5, R_2 must be returned to a voltage not less than 1.6 volts below the positive supply. The four diodes D_1 through D_4 provide a nominal drop of 2.4 volts which is adequate to protect Q_5 from saturation under worst case conditions. If Q_5 were allowed to saturate, the effect would be a sudden reduction in the input resistance to the second stage and a consequent loss of gain. This would produce excessive distortion in high gain circuits for high level outputs.

The resultant excellent linearity of the circuit can be seen in the open loop transfer characteristics shown in Figure 6.

INPUT VOLTAGE RANGE

The maximum differential input voltage is limited by the reverse emitter base breakdown voltage of Q_1 and Q_2. The resistance of the zenered emitter/base junction is very low and, unless externally limited, large input currents may flow causing destruction of the metalization and/or the junction. In any case, reverse bias of this junction may cause substantial degradation in the transistor characteristics.

Common mode input range is limited in the negative direction by saturation of the current source Q_3. If the input voltage falls below approximately $3V_{BE}$ above the negative supply,

Q_1 and Q_2 both turn off, the collectors rise to the potential at X and the output becomes indeterminate.

In the positive direction the input transistors begin to saturate when the input level exceeds the collector voltage, which has been shown to be about 3.4 volts below the positive supply. The output will then depend upon the relative values of the two inputs.

Figure 7 shows the useful common mode input range as a function of supply voltage.

Common mode rejection as a function of frequency appears in Figure 9. Input bias current and offset current are given in Figure 10 and 11 as functions of temperature and supply voltage.

LATCH-UP

In many operational amplifiers, a problem arises when operating in the unity gain voltage follower configuration. A large positive input voltage may cause the input stage to saturate. When the output gets high enough to saturate the inverting input, it may become non-inverting and the output may be held in a high state regardless of the input. Latch-up cannot occur with the μA749 since as soon as the non-inverting input saturates and its collector voltage rises, the output drops until the inverting input transistor base becomes reverse biased to the EB zener voltage. The output is then clamped BV_{EBO} volts below the input and the non-inverting input comes out of saturation.

Figure 8 shows the output with a triangular input (a) at the onset of saturation and (b) at full overdrive.

OUTPUT VOLTAGE RANGE

The negative output voltage range is equal to the negative supply (provided the DC load is to negative supply) since the output transistor is turned off in this condition. Note that the integrated circuit cannot draw a negative output current. Any such current must be drawn by the external load resistor.

The positive output voltage is limited to the saturation voltage of the output transistor plus the voltage drop in R_6 caused by the load current Typical output voltage capability for various loads and supplies is shown in Figure 12.

The maximum output current which may be drawn from the circuit is limited by the available drive from Q_5. Assuming infinite h_{FE} for the output transistor, the maximum voltage across R_5 is: 0.350 x 9 = 3.15 volts. Allowing 0.6 volts for the emitter junction of the output transistor, this leaves 2.55 volts across R_6. This will be produced by a load current of 12.75mA.

This current limiting at the output gives a measure of short circuit protection, however, a small percentage of the production distribution will provide a high enough output current that with a sustained short circuit the dissipation will exceed the maximum for the package, and excessive localized heating will occur. This is why the data sheet indicates a time limit of 30 seconds for any short circuit. Maximum and minimum output currents are guaranteed on the μA749 data sheet.

SUPPLY VOLTAGE

Performance of the μA749 is specified for supply voltages from ±4V to

±15V, and useful performance can be obtained from ±3V to ±18V. Symmetry of power supplies need not be maintained as long as the input common mode range is not exceeded.

POWER DISSIPATION

Typical dissipation of the μA749 with a 30 volt supply is 350mW. Figure 13a gives the device dissipation as a function of load resistance and supply voltage. The dashed line in Figure 13a gives the total circuit dissipation including the loads. These specifications are for an output voltage halfway between the positive and negative supplies - the normal quiescent mode in a linear amplifier circuit. The maximum dissipation for the package is 500mW derated at 9mW/°C above 95°C.

NOISE

The input stage current was selected to give an optimum noise source resistance in the region of 10kΩ The broadband (10Hz - 100kHz) noise figure for such a source is typically 4dB.

Spot noise voltage and current are plotted in Figures 14 and 15.

AMPLIFIER SEPARATION

Although the two amplifiers on the μA749 chip are electrically interconnected (see Figure 1), they display excellent separation characteristics. This is possible since the interconnection is at low impedance common mode points X and Y. Coupling will occur, however, as with any two amplifiers connected to the same supply, if the supplies are not properly decoupled. At high frequencies, capacitance or mutual inductance between pins and more significantly between external connections will cause some coupling as with a discrete circuit.

The kind of separation which may be obtained with the aid of a simple copper screen down the center of the Dual-In-Line package is illustrated in Figure 16.

Note that the total open-loop voltage gain within the single chip is typically 170dB. With this much gain only a small amount of stray feedback can cause instability. Reasonable care should be taken when laying out a circuit to avoid unnecessary strays.

HIGH FREQUENCY COMPENSATION

The open-loop gain and phase responses of μA749 are shown in Figures 17 and 18. The dominant pole at 600kHz is caused by the transit delay in the lateral PNP. Two other major poles at approximately 1MHz and 2MHz are caused by the phase shift at the collectors of the differential gain stages. For very high source impedances, the input capacitance will add a pole as shown by the dashed line in Figure 17. Variation of 180° phase shift frequency with supply voltage is shown in Figure 19. Since the open loop gain of the μA749 is greater than unity at this frequency, external means of rolling off the gain are required to prevent oscillation in a feedback system.

There are many ways in which this may be achieved depending upon the desired results. Figures 20a, b, c, and d show four different schemes. The most convenient compensation is by means of a capacitor connected between the input lag terminals at the collectors of the first stage as in Figure 20a. Typical open and closed loop gains using this type of compensation are shown in Figure 21 and 22. Note the addition of a series

resistor to the compensation capacitor in order to increase phase margin. It is also possible to compensate by means of capacitor from the output lag terminal to V+ as in Figure 20b, or from output to V- as in Figure 20c. Local capacitive feedback around each stage could also be used. An example of this appears in Figure 20d. This is quite useful in the last stage where a small feedback capacitor will help control the PNP stage roll-off as shown in Figure 23. This enables a reduction in the input lag capacitor, increasing slew rate, as shown in Figure 24.

The slew rate can be predicted for any value of capacitor from the equation:

$$\text{slew rate} \quad S = \frac{I}{C} \cdot A$$

where I is the available current to charge the capacitor, C is the capacitor value, and A is the gain from the compensating point to the output.

For example if 0.01μF is used between pins 3 and 4 and I = 200μA, A = 26x25, then S = 13V/μS.

The above responses apply to a load resistance of 5kΩ . Changing the load will change the gain shown in Figure 3 so that the compensation capacitors should be changed in proportion. The only exception to this is when using compensation at the output pin. In this case, the compensation capacitor value does not change with load resistors.

It is possible to compensate the μA749 down to 20dB closed-loop voltage gain using only a series resistor and capacitor from output to V-. This is ideal for use in high gain circuits such as stereo tape amplifiers where the user is able to realize cost savings by use of the μA749D. This version of the μA749 does not bring out any of the compensation points so that only 8 pins are required for the total amplifier, which is packaged in a metal can TO-99.

OUTPUT CAPABILITY

At high frequencies the rate of change of output will be slew rate limited so that the maximum distortionless output will depend upon the compensation used. Figure 25 shows the output capability as a function of frequency for various compensation networks.

CONCLUSION

The μA749 has been shown to be a simple circuit with characteristics comparable to far more elaborate designs. Its high gain and output swing enable its use as a high gain amplifier over a wide range of supply voltages, while the flexibility of frequency compensation permits its use as a unity gain amplifier with a high slew rate. The small chip size and optional packaging will enable considerable cost reductions to be realized in many systems without compromising performance.

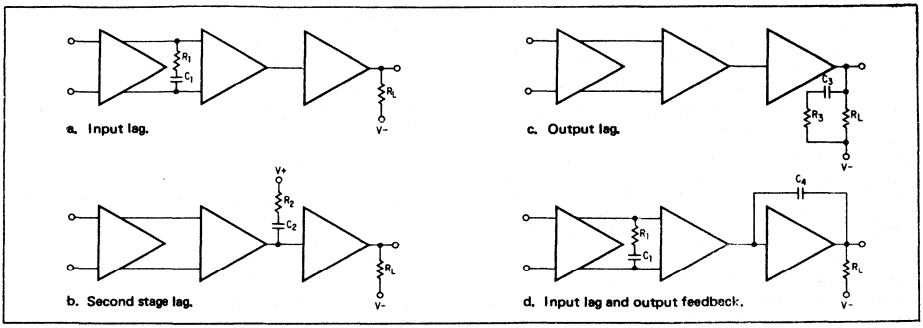


Fig. 20

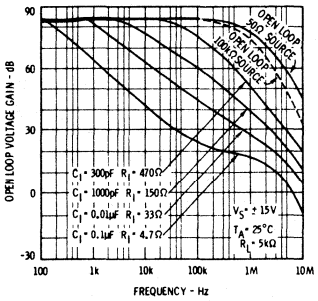


Fig. 21a. Open-loop frequency response using recommended compensation networks.

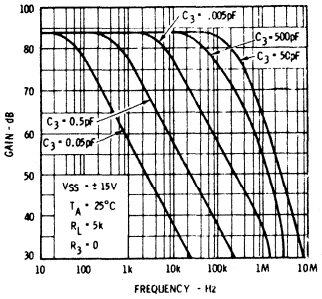


Fig. 21c. Frequency response output compensation — pin 1 to ground.

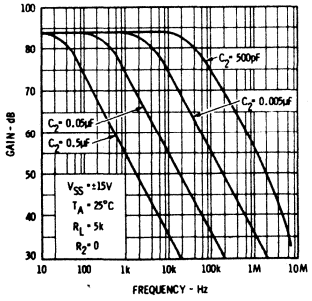


Fig. 21b. Frequency response second stage lag compensation — pin 2 to pin 14.

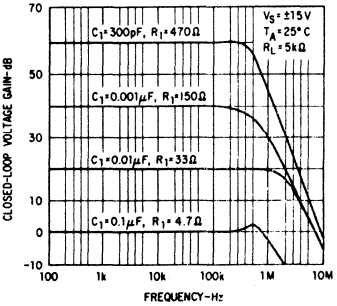


Fig. 22. Closed loop gain as a function of frequency.

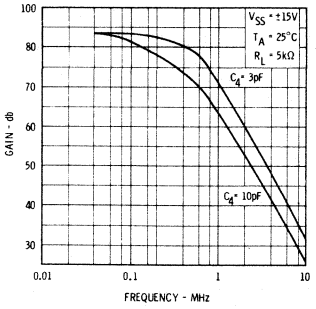


Fig. 23. Frequency response with out put stage feedback only — pin 1 to pin 2.

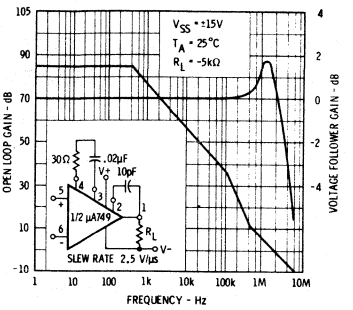


Fig. 24. Maximum slew rate unity gain frequency response.

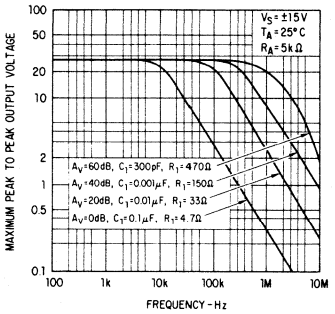


Fig. 25. Output capability as a function of frequency and input lag compensation.

A TRAPEZOIDAL DEFLECTION CIRCUIT FOR USE WITH THE 3250 NUMERIC CHARACTER GENERATOR USING THE μA715

The high slewing rate of the μA715 operational amplifier makes it useful in the generation of complex deflection waveforms for display systems. This application demonstrates how the μA715 may be used in conjunction with the 3250 numeric character generator.

The 3250 is an MOS device designed to control the generation of seven segment numeric characters for CRT display. It accepts a binary coded input defining the number that is to be displayed, generates the appropriate video blanking pulses, and also provides pulses for controlling X and Y axis deflection circuitry. If electrostatic deflection is used to form the display characters, these deflection pulses must be converted to a trapezoidal waveform. The following circuit description outlines one method by which the trapezoidal deflection signals may be obtained.

A schematic of the deflection circuit is shown in Figure 1. The circuit is fundamentally an integrator, with the input voltages to be integrated controlled by the deflection pulses from the 3250. The inputs for the integrator are derived from a voltage divider (R_1, R_2, R_3). The resistors are chosen such that the voltage at point A is about -8 volts and the voltage at point B about -18 volts.

The voltage divider formed by R_4, R_5, and R_6 biases the non-inverting input of the μA715 to a voltage midway between the voltages at points A and B (about -13 volts). R_4 is a variable resistor permitting the voltage at the non-inverting input to be adjusted to the midpoint between point A and point B.

There are three possible input conditions for the integrator:

1. Input from point A
2. Input from point B
3. No Input

The input condition selected is determined by the deflection pulses from the 3250. Switching of the input voltage is accomplished using junction field effect transistors, Q_3 and Q_4. The J-FET's are interfaced with the 3250 through PNP transistors Q_1 and Q_2.

When the deflection pulse outputs from the 3250 are in the "1" state (most negative) then the J-FET switches are off and we have the "no input" condition. When the "+" deflection pulse is in the "0" state then Q_3 is turned on and the output of the integrator is a positive going ramp, the integrator input signal being taken from point B. Likewise, when the "-" deflection pulse is in the "0" state the input to the integrator comes from point A, producing a negative going ramp at the output. The logic design of the 3250 prevents both inputs from being connected to the integrator simultaneously.

A timing diagram for the X deflection pulses is shown in Figure 2, along with the resultant deflection waveform. The 3250 has a maximum segment frequency of 250kHz, thus each deflection pulse is 4 μsec long. Potentiometers R_8 and R_9 provide fc. adjusting the slopes of the output waveform and equalizing the effect of the "on" resistance of Q_3 and Q_4. DC stabilization is provided by the 24k resistor R_7. The μA715 derives its power from the same -27 volts supply used by the 3250.

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To prevent tilt on the flat portions of the trapezoidal waveforms a third J-FET is included in the feedback loop of the integrator. This device, Q_5, is driven from a diode OR gate, comprised of D_1 and D_2, such that it is on only when Q_3 or Q_4 is on; otherwise, Q_5 is off. Thus, unless an input is being integrated the integrating capacitor C is isolated from the DC feedback resistor R7. This prevents the charge on C from leaking off through R7. Figure 3 shows the actual output signal. The tilt due to the input bias current of the μA715 is negligible with the respect to the 6 volt p-p output signal obtained from this circuit.

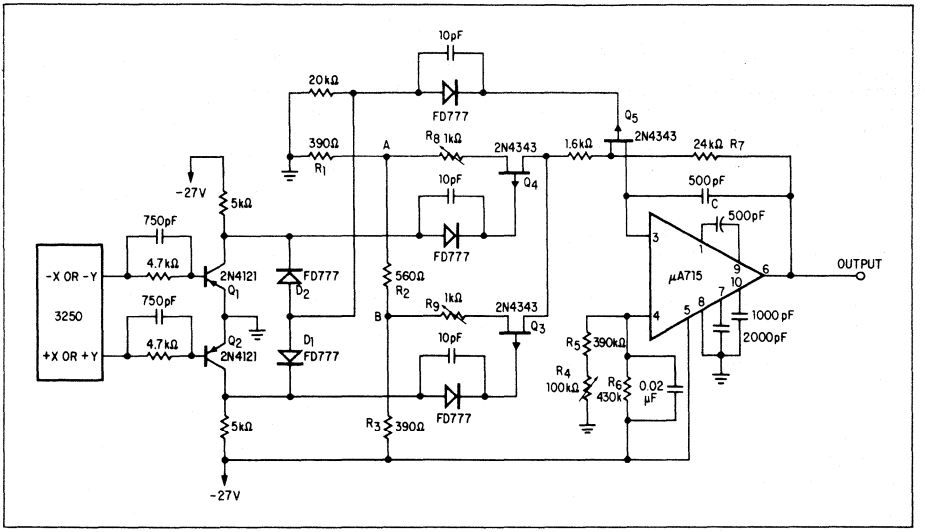


Fig. 1 Trapezoidal deflection generator.

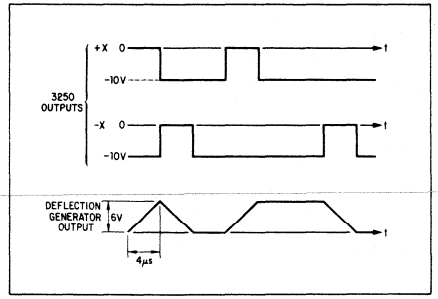
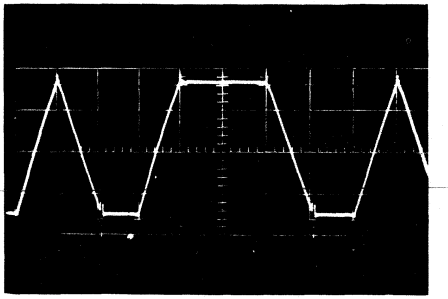


Fig. 2 Input and output signals for the CRT deflection generator.



SCALES:
HORIZONTAL: 4 μsec/cm
VERTICAL: 2 VOLTS/cm

Fig. 3. Output from μA715 deflection generator for use with the 3250 CRT numeric character generator.

A HIGH SPEED SAMPLE AND HOLD USING THE μA715

Many data processing systems require that analog input signals be sampled and that the sample value be held constant for the time necessary to perform an analog-to-digital conversion. The circuit to be described illustrates one method by which this sample and hold function may be accomplished using the μA715 high speed operational amplifier.

A schematic of the basic sample and hold circuit is shown in Figure 1. In the sample mode, the sampling switch Q_1 is turned on and the circuit functions as an inverting operational amplifier with voltage gain given by the negative of the resistor ratio R_2/R_1. If R_1 is equal to R_2 the circuit is a unity gain inverting amplifier and the output is an inverted replica of the input.

When Q_1 is switched off the circuit enters the hold mode. The voltage value of the output at the instant Q_1 is switched off is retained across the holding capacitor C_1. In the hold mode the circuit functions as an operational integrator. With Q_1 off there is no input to the integrator and the output remains constant.

The acquisition time when going from the hold mode to the sample mode is a function of the time constant R_2C_1 and the required accuracy. The time necessary to reach the input level upon switching from hold to sample is given by:

$$t_a = R_2C_1 \ln\left(\frac{100}{\%\ \text{accuracy}}\right) \qquad (1)$$

A practical sample and hold circuit is shown in Figure 2. Included in this figure are the components necessary to compensate for the DC and AC errors inherent to the basic circuit of Figure 1.

The DC offset of the μA715 is adjusted to zero by introducing a controlled imbalance in the 715 input stage collector currents. This is accomplished by connecting a 50k potentiometer (R_4) across the input frequency compensation terminals of the μA715 and returning the wiper of R_4 thru an 82k resistor to V+. The μA715 is frequency compensated for unity gain operation by C_3, C_4, and C_5.

A junction field effect transistor is used as the sampling switch Q_1. Because there is some capacity from the gate to the source of Q_1, a portion of the gate signal to the switch is coupled through the device onto the holding capacitor C_2. Thus, a slight offset voltage is added to the output when switching from sample to hold.

A particular advantage of the operational sample and hold is that the AC offset is independent of the analog signal level. The offset can be compensated by removing a fixed amount of charge from the holding capacitor upon switching into the hold mode. In Figure 2 the offset is bucked out by an opposing signal, coupled by C_2, from the sample pulse input onto the holding capacitor.

During the hold time the output voltage will tend to drift as the holding capacitor integrates the input bias current of the μA715. This drift can be compensated by supplying bias current from a separate source such that there is no current flow through the holding capacitor. In Figure 2 this compensation is provided by R_5, R_6, R_7 and D_1. D_1 acts as a temperature dependent voltage source causing the bias current thru R_5 to decrease with increasing temperature. This provides partial temperature compensation of bias current as the μA715, like other operational amplifiers with a

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bipolar input stage, has a negative temperature coefficient of input bias current.

With a 10 volt step input (±5 volts to ∓5 volts) the settling time to ±0.05% is 10 μsec. This is slightly longer than that given by equation 1 due to the finite "on-resistance" of the sampling switch Q_1. If C_1 is decreased to 100pF the settling time is about 1 μsec. Temperature drift of the output in the hold mode is approximately 0.001% per degree Centigrade for a hold time of 100 μsecs.

An example of where a sample and hold circuit such as the one described can be used is with a sequential approximation A/D Converter. If 9-bit accuracy is required (0.2%) and 0.1% of the overall error is assigned to the sample and hold, the acquisition time for a full scale input change is 10 μsec. This corresponds to the amount of time that must be allowed before the most significant bit can be converted. If subsequent bits are converted at the same rate then the required holding time is 90 μsec to complete conversion of the 9 bits.

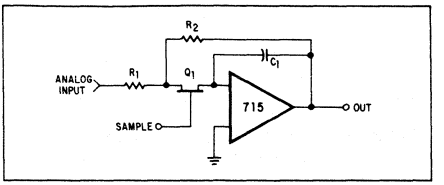


Fig. 1 Basic operational sample and hold circuit.

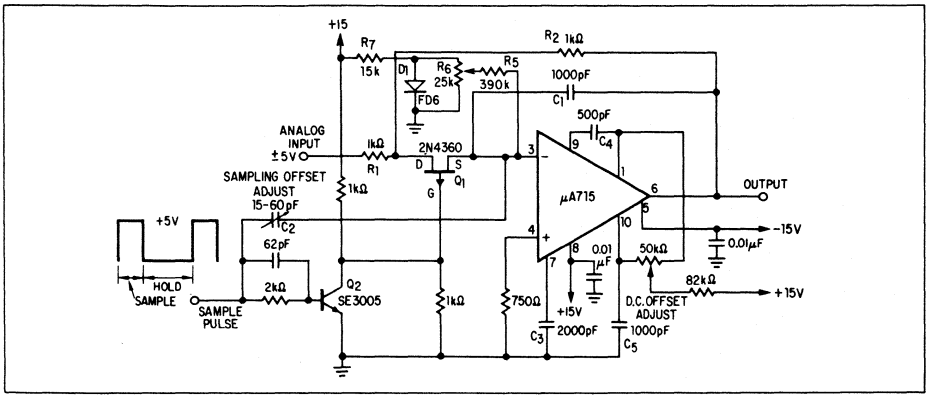


Fig. 2 μA715 Sample and hold circuit.

Q

LOW-PASS ACTIVE FILTER FOR ELECTRONIC IMAGING USING THE μA715

Electronic imaging devices perform the task of converting a pattern of incident light falling upon the surface of a photo sensitive semiconductor into a voltage waveform. This voltage waveform (video signal) is an ordered sequential reproduction of the incident light pattern. Applications include: reconnaissance systems, solid state TV cameras, facsimile reproduction, pattern recognition and many more.

The photo sensor used in this system is a FAIRCHILD linear complex optical array (COA), of monolithic construction, composed of 128 phototransistors. To interpret the video information from the COA, each of its 128 phototransistors is interrogated sequentially by a scan generator (Figure 1).

This scanning function is accomplished by decoding each state of a seven bit synchronous binary counter. The master clock determines the scanning rate. Sixteen MSI 9301 one-out-of-ten decoders are used. Each output of these 9301's is connected to one of the emitters of the COA (Figure 2). When these emitters are sequentially interrogated a sampled video signal appears across the load resistor R_L.

Since the inception of this imaging system the 9311 has become available as another MSI product from Fairchild. This device is designed as a one-out-of-sixteen decoder and hence is the one to be used in this application.

The signal conditioning is accomplished by a Fairchild μA715 used as a third order Chebyshev low-pass filter. The Fairchild μA715 is especially suited for this application, providing the bandwidth and the high slew rate needed for the video signal conditioning.

The scan frequency for this system is f_S = 1MHz. From the theory of sampling we know that the spectrum of the sample pulse is centered at the sampling frequency. Furthermore, we know that the maximum permissible video information frequency is at one half the sampling frequency.

Figure 4 shows an ideal frequency domain representation for a rectangular sampling pulse. It is therefore possible to separate the wanted video information.

The Chebyshev filter (see Figure 2) has a closed loop DC gain of 20dB to provide the necessary amplification. The standard 20dB compensation network is used. The DC voltage gain can be easily calculated:

$$\frac{E_{out}}{E_{in}} = -\frac{R_f}{R_S}$$

$$R_S = R_L + R_1 + R_2$$

$$R_f = \frac{R_5 (R_6 + R_7)}{R_5 + R_6 + R_7}$$

R_L is the load resistor for the COA and also part of the Chebyshev filter, and is returned to a positive DC voltage V_{ref}. The non-inverting amplifier input is also returned to V_{ref} by R3 in order to reject all the common mode noise signals. To cancel a possible output voltage drift due to temperature changes the DC impedance was made equal for both inputs. By making

$$R3 = \frac{R_S R_f}{R_S + R_f} \quad \text{both inputs}$$

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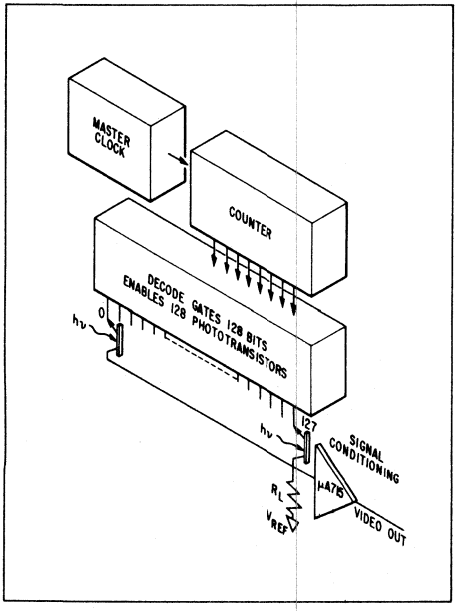


Fig. 1. System block diagram.

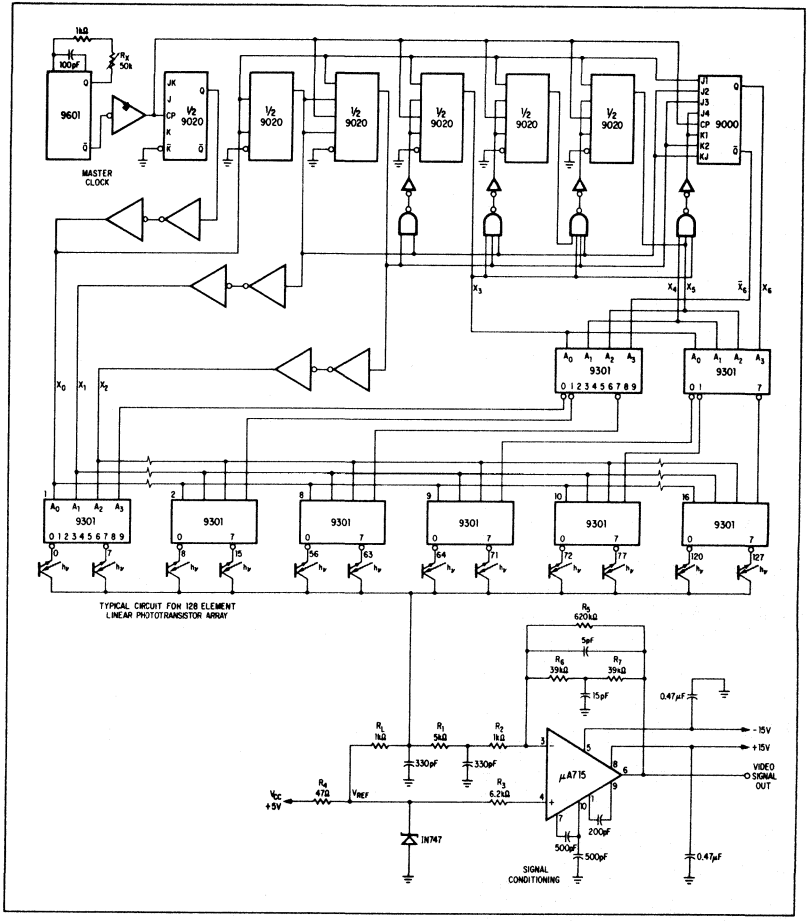


Fig. 2. System circuit diagram.

impedances are equalized. Furthermore, by making V_{ref} equal to the sampling pulse amplitude, the output is zero for a zero input (no light).

Figure 3 shows the frequency response curve. The 3dB-down point occurs at the cutoff frequency f_C = 500kHz equal to one half the sampling frequency. The response curve starts to roll off at a rate of 18dB/octave beginning at f_C.

A detailed article on an active band pass filter can be found in this handbook. A design procedure for an active low-pass filter can be found in the reference.

The output video signal then represents the original incident light pattern sensed by the optical array. The FAIRCHILD μA715 provides a low output impedance. This Chebyshev filter provides an output swing of typically 20 volts peak-to-peak into 2kΩ load up to the cut-off frequency f_C. In this application the output signal is between zero and ten volts according to the light level at the sensor.

For more FAIRCHILD photodevice reference information send a letterhead request to John Brown, MS 4-292, Dept. 26-26, 313 Fairchild Dr., Mountain View, California 94040.

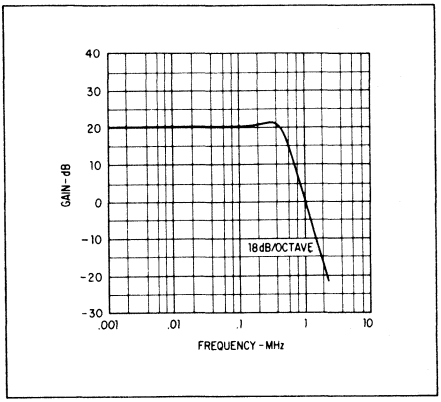


Fig. 3. Frequency response.

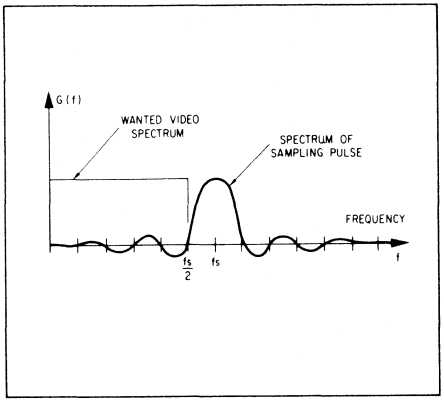


Fig. 4. Idealized frequency plot.

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1. G. P. Weckler, "Operation of p-n Junction Photodetectors in a Photon Flux Integrating Mode", IEEE Journal of Solid-State Circuits, pp. 65-73, September, 1967.
2. A. L. McMullen, C. E. Smeder, "Charts Speed Active-Filter Design", Electro-Technology, pp. 76-78, February, 1968.

μA725 AGC AMPLIFIER

Certain electronic systems require amplifiers capable of handling input signal levels that vary over an extremely wide range and yet provide a relatively constant high fidelity output level. Such amplifier systems are usually driven by a sensor or transducer and is measuring some form of energy (infrared, visible light, sound, pressure, etc.). One sensible way of handling wide ranges of input levels is to use an AGC'd amplifier. The following article describes an AGC'd amplifier using the low noise, high gain μA725 operational amplifier.

Figure 1 shows the block diagram of a proposed AGC'd bandpass amplifier. The input signal is applied to a voltage controlled variable attenuator. The attenuator feeds its output signal to a bandpass amplifier. Another voltage controlled variable attentuator then processes the signal and drives a second AC amplifier. The second AC amplifier output level is converted to a DC control voltage by the output level detector. The DC control voltage is directly related to the E_{out} signal level. Total AC system voltage gain at the center frequency (without AGC action) is 100,000.

Figure 2 illustrates the complete schematic of the AGC'd amplifier. Both voltage controlled variable attentuators consist of a capacitive coupled 10kΩ resistor R_1 (1/2 of the divider) in series with a diode (second 1/2 of the divider). The outputs of both AC dividers are connected to their following amplifier.

It is a well known fact that the AC impedance of a diode, biased ON in its forward direction, will vary over a wide range as a function of the magnitude of its forward current. Most diodes readily change AC impedances by a factor of 100:1 and some > 300:1. We selected a low voltage zener diode, to be used in its forward direction, due to its known "soft knee" characteristics. Higher signal levels can be attenuated with a "soft knee" diode without causing distortion of the signal than with a "sharp knee" type diode.

The first μA725 operational amplifier is a bandpass amplifier. Its center frequency and bandwidth are controlled by the bridged "T" null network placed in its negative feedback loop. The maximum AC gain occurs at the null center frequency, as minimum AC negative feedback will be present at that frequency. The bandpass amplifiers DC gain has been set at unity, thus an offset voltage adjustment control is not required for this stage. This first μA725 operational amplifier then, is used as a combined low noise preamp/active filter with a voltage gain of ≈10. Its output is capacitively coupled through the second voltage controlled variable attenuator to drive the second AC amplifier.

The second μA725 operational amplifier is set up as an AC amplifier with a voltage gain of ≈10,000. Its output is the output signal (E_{out}) of the AGC'd amplifier system and also provides the input signal to the output level detector.

The output level detector consists of a buffer emitter follower stage driving a diode voltage doubler circuit. The DC output voltage of the voltage doubler is filtered and provides the base current for two AGC transistors. The AGC transistors in turn provide the control voltages applied to the two forward biased zener diodes to control the magnitude of their forward currents

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and thus their AC impedances.

Resistor R_t acts as one element of a voltage divider and can be used to set the AGC'd output level to a desired amplitude.

Changing the overall AC gain of the amplifier system $\left(\frac{E_{out}}{E_{in}}\right)$ changes the AGC knee position accordingly (see Figure 4).

The overall amplifier response is shown by, Figure 3.

In summary, two voltage controlled attenuators reduce the signal levels applied to their respective following amplifiers as their DC control voltages increase in value. The DC voltages are derived from the E_{out} signal and is directly related to the absolute value of the E_{out} signal. Thus as the AC signal level at E_{out} tries to rise, the variable attenuators, in turn, try to attenuate the AC signal further and prevent the rise of the E_{out} signal. The total effect is AGC action. Actual system results were plotted and are given in Figure 4.

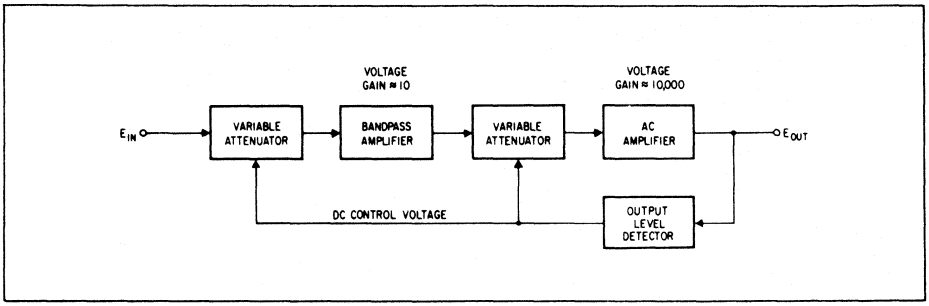


Fig. 1. μA725 AGC amplifier block diagram.

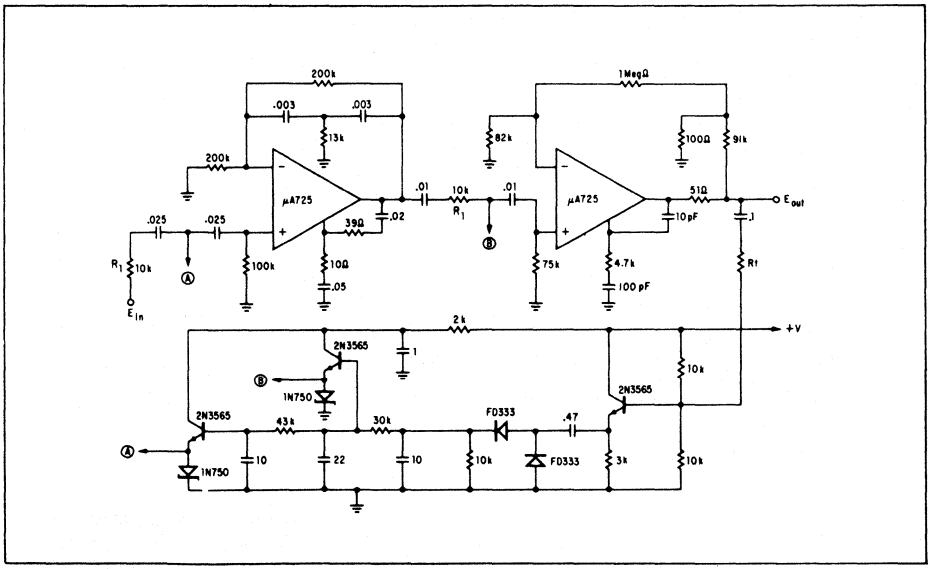


Fig. 2. μA725 AGC amplifier.

TABLE I

SCHEMATIC NOTES

1. All capacitor values are μf d. unless otherwise indicated.
2. R_t is selected for desired AGC'd output level at E_{out}. Typical R_t values are 2kΩ = 4V pk-pk @ E_{out} with 1 vrms @ E_{in} & 12kΩ = 10V pk-pk @ E_{out} with 1 vrms @ E_{in}.
3. The 10kΩ resistor at E_{in} simulates the generator source impedance. Its absolute value is not critical but there are trade-offs between amplifier gain, noise figure and AGC dynamic range if the source impedance value is drastically changed.

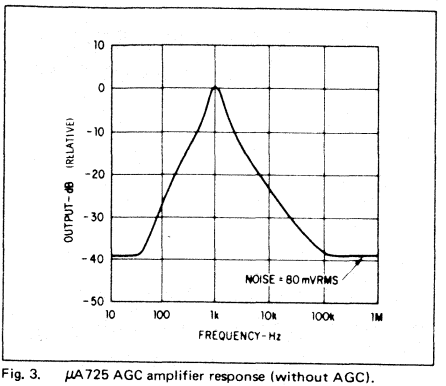


Fig. 3. μA725 AGC amplifier response (without AGC).

TABLE II

TYPICAL PERFORMANCE FIGURES

1. Voltage Gain (@ 1kHz) = 100,000.
2. AGC dynamic range > 100dB. (with total harmonic distortion < 1%).
3. AGC slope = 0.3dB/E_{in} decade.
4. AGC 100dB E_{in} Δ = 2.9dB E_{out} Δ.
5. Equivalent input noise (E_{in} grounded) = 0.8 μvrms.
6. Center frequency = 1.0kHz.
7. Bandwidth = 550Hz.
8. E_{out} AGC'd level (E_{in} = 1 vrms) = 4 vpk-pk.

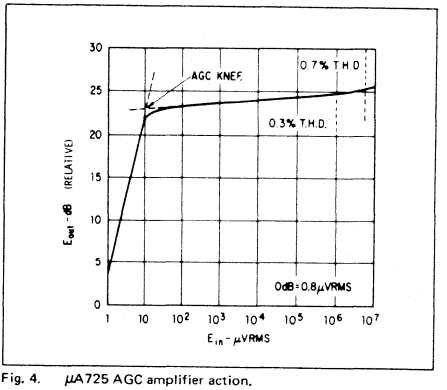


Fig. 4. μA725 AGC amplifier action.

AN ARITHMETIC ANALOG COMPUTER USING μA735 LOGARITHMIC AMPLIFIERS

The design of control systems may require the arithmetic manipulation of analog input signals from transducers or sensors. In complex systems this manipulation can often be handled by converting the analog inputs to digital signals and processing the data with a digital computer. In less elaborate systems, however, where only a few signals are to be processed and the accuracy required is one or two percent, the cost of a digital processor is prohibitive. This is especially true if multiplication or division of the input signals is to be performed.

Logarithmic amplifiers using monolithic operational amplifiers and bipolar transistors as logarithmic feedback elements provide a simple and effective means for realizing analog computers for the generation of arithmetic functions. The following discussion describes the basic operation of a transistor feedback log amplifier and the application of the μA735 micropower operational amplifier to the design of a computing circuit.

Theory

A basic log amplifier circuit is shown in Figure 1. The operation of this circuit is based on the logarithmic relation between the transistor collector current I_C and base-emitter voltage V_{BE}. For values of $V_{BE} > 4\,kT/q$, an excellent approximation of this relationship is given by

$$V_{BE} = \frac{kT}{q} \ln\left(\frac{I_C}{I_S}\right) \qquad (1)$$

where I_S is the saturation current of Q_1.

Equation 1 has been shown to be accurate within about 1 percent over as many as nine decades of collector current.[1]

Because the transistor is operated in the grounded base configuration the output of the basic log amplifier is simply

$$E_{out} = -V_{BE} = -\frac{kT}{q} \ln\left(\frac{I_C}{I_S}\right) \qquad (2)$$

As the inverting input of the operational amplifier presents a virtual ground and a high input impedance, the collector current of Q_1 is given by

$$I_C = E_{in} / R_1 \qquad (3)$$

Substituting (3) into (2) we have

$$E_{out} = \frac{kT}{q} \ln\left(\frac{E_{in}}{R_1 I_S}\right) \qquad (4)$$

or rearranging

$$E_{out} = -\frac{kT}{q}\left[\ln\left(\frac{E_{in}}{R_1}\right) - \ln(I_S)\right] \qquad (5)$$

It can be seen from (5) that the output voltage is a log function of E_{in}, plus a term dependent on the physical characteristics at Q_1.

Circuit Description

As an illustration of how the log amplifier can be used for arithmetic computation, the design of a circuit that generates the function

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$$F = \frac{A-B}{B} = \frac{A}{B} - 1 \qquad (6)$$

will be described. The operational amplifier used is the μA735 micropower amplifier. The advantages of the μA735 are that it has extremely low power dissipation, making it useful in field or satellite applications where limited power is available, and also it exhibits very low input bias current. This low bias current is important, as any current flowing into the input of the μA735 constitutes an error in the value of I_C assumed in Equation (3). Because the μA735 bias current is low, the dynamic range of the log amplifier is extended to very small signal levels without requiring adjustment to compensate for bias current errors.

A schematic of the computing circuit is shown in Figure 2. The circuit operates as follows: The logarithms of the input signals A and B are generated by log amplifiers A_1 and A_2 respectively. The frequency compensation of the amplifiers has been modified to account for the gains of Q_{1A} and Q_{1B} in the feedback loop. The 1k resistors in series with the μA735 outputs serve to limit the loop gain so that the amplifier can be compensated. Diodes D_1 and D_2 limit the positive output swing of A_1 and A_2 to protect the emitter base junction of Q_{1A} and Q_{1B} should the input terminal be left open.

Referring to equation (5) the output of A_1 is

$$E_{OA} = -\frac{kT}{q} \ln\left(\frac{A}{R_1}\right) + \frac{kT}{q} \ln (I_{sa}) \qquad (7)$$

likewise the output of A_2 is given by

$$E_{OB} = -\frac{kT}{q} \ln \frac{B}{R_2} + \frac{kT}{q} \ln (I_{sb}) \qquad (8)$$

if $R_1 = R_2 = R$ and the log transistors Q_{1A} and Q_{1B} are matched such that $I_{se} = I_{sb} = I_s$ we have

$$E_{OA} = -\frac{kT}{q} \ln\left(\frac{A}{R}\right) + \frac{kT}{q} \ln (I_s) \qquad (9)$$

and

$$E_{OB} = -\frac{kT}{q} \ln\left(\frac{B}{R}\right) + \frac{kT}{q} \ln (I_s) \qquad (10)$$

E_{OA} and E_{OB} are applied as two inputs to the three input differential amplifier A_3. The third input, E_C, is derived from the diode connected transistor Q_{2A}. E_C is the base emitter voltage of Q_{2A} and is given approximately by

$$E_c = \frac{kT}{q} \ln \left[\frac{I_C(Q_{2A})}{I_S(Q_{2A})}\right] \qquad (11)$$

The value of $I_C(Q_{2A})$ is set by R_3, R_4 and V+.

The output of A_3 is

$$\begin{aligned} E_{O3} &= E_{OA} - E_{OB} - E_C \\ &= -\frac{kT}{q} \ln\left(\frac{A}{R}\right) + \frac{kT}{q} \ln (I_s) + \frac{kT}{q} \ln\left(\frac{B}{R}\right) \\ &\quad -\frac{kT}{q} \ln(I_s) - \frac{kT}{q} \ln \left[\frac{I_C(Q_{2A})}{I_S(Q_{2A})}\right] \\ &= \frac{kT}{q} \left\{-\ln\left(\frac{A}{R}\right) + \ln\left(\frac{B}{R}\right) - \ln\left[\frac{I_C(Q_{2A})}{I_S(Q_{2A})}\right]\right\} \end{aligned} \qquad (12)$$

simplifying to

$$E_{O3} = -\frac{kT}{q} \ln\left[\frac{A}{B} \frac{I_C(Q_{2A})}{I_S(Q_{2A})}\right] = -V_{BE}(Q_{2B}) \qquad (13)$$

From equation 13 we see that E_{O3} is proportional to the log of A/B.

The antilog of E_{O3} must be taken to obtain the value of A/B. It is at this step that the purpose of E_C becomes apparent. As shown by equation 13, the collector current of Q_{2B} is a function of E_{O3}. This current is given by

$$I_C(Q_{2B}) = I_S(Q_{2B}) \exp (V_{BE}(Q_{2B}) {}^{q}/_{kT}).$$

$$I_C(Q_{2B}) = I_S(Q_{2B}) \exp\left[\ln \left\{\frac{A}{B} \frac{I_C(Q_{2A})}{I_S(Q_{2A})}\right\} \frac{kT}{q} \frac{q}{kT}\right]$$

$$I_C(Q_{2B}) = \frac{A}{B} I_C(Q_{2A}) \frac{I_S(Q_{2B})}{I_S(Q_{2A})}$$

if Q_{2A} and Q_{2B} are matched, the I_S terms cancel yeilding.

$$I_C(Q_{2B}) = \frac{A}{B} I_C(Q_{2A}) \qquad (14)$$

Note that the kT/q temperature dependence associated with the log terms is cancelled by the inverse dependence on q/kT when taking the antilog. Thus, if Q_{1A} and Q_{1B} are at the same temperature as Q_{2A} and Q_{2B}, temperature effects on the circuit are minimized. The temperature differential between Q_1 and Q_2 can be minimized by mounting them together on a common heat sink.

It can be seen that the inclusion of E_C provides compensation of the I_S term associated with the antilog transistor Q_{2B}. The fact that E_C is obtained from a transistor matched to Q_{2B} means

that the compensation will temperature track as long as Q_{2A} and Q_{2B} are at the same temperature. This condition is assured with a dual transistor as both devices share the same package.

The output amplifier A4 performs the final operation of converting $I_c(Q_{2B})$ (now proportional to A/B) to a voltage and subtracting "1" from A/B as required by equation 6. The output from A4 is given by

$$E_{out} = R_6\ I_c(Q_{2B}) \cdot E_D \left(\frac{R_6}{R_5}\right) = R_6\ I_c(Q_{2A})\ \frac{A}{B} \cdot E_D \left(\frac{R_6}{R_5}\right) \qquad (15)$$

Letting $R_5 = R_6 = \frac{1}{|I_c(Q_{2A})|}\ \Omega$ and E_D = 1 volt

we have from (15)

$$E_{out} = \frac{A}{B} \cdot 1 = \frac{A \cdot B}{B} \qquad (16)$$

Calibration

Calibration of the circuit is accomplished as follows. First, the input offset voltage of the log amplifiers A_1 and A_2 must be compensated. This is most easily done with the collectors of Q_{1A} and Q_{1B} disconnected. A 100k resistor should be connected in place of each transistor to provide some DC feedback. With both inputs A and B grounded, the offset control R7 is adjusted until E_{OA} is zero volts. Likewise R_8 is adjusted to make make E_{OB} equal zero. The 100k resistors are now removed and the collectors of the log transistors reconnected.

The next step is to adjust the value of E_D. This is done with the collector of Q_{2B} disconnected from A4. Control R_9 is then adjusted until the output of A4 equals -1 volt; reconnect Q_{2B}.

The final calibration step is the adjustment of E_C. Inputs A and B are connected together and a +1 volt input applied. Control R3 is then adjusted until the output from A4 is zero volts. This completes the calibration.

Performance

The measured performance of the arithmetic computer is shown in Figure 3. The full scale output range for the circuit was defined as -1 volt to +10 volts. Inputs A and B ranged from 10mV to 10 volts. The maximum error observed was less than 2.5 percent of full scale for A = 100mV, B = 10mV. For values of A and B between 100mV and 10 volts the largest error observed was 1.3 percent. This is quite acceptable performance as ±1% resistors were used in the circuit tested.

Conclusion

The log amplifier provides a useful method for the arithmetic manipulation of analog signals. In the design example, division of the input variables was accomplished by subtracting logarithms. Other operations that can be simply performed are multiplication, root extraction, and raising to a power. Inputs are multiplied by adding their logarithms and roots and powers are obtained by multiplying the log by a suitable constant. This can be done by using a voltage divider for roots and a fixed gain amplifier for powers.

The use of dual transistors for log and antilog operations simplifies construction and calibration of the final circuit. The matched characteristics of the devices also provides temperature compensation and eliminate the need for selecting individual transistors for matching.

The accuracy of the arithmetic computer is consistent with that required by many simple control systems. Where a limited number of analog signals are to be processed, it provides an economical alternative to digital arithmetic units and A to D converters.

References

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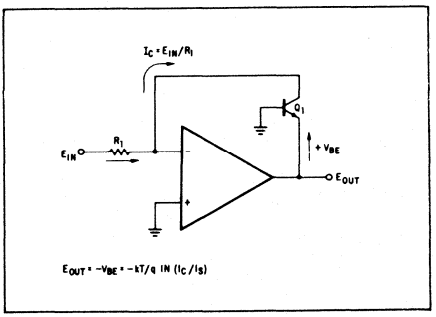


Fig. 1. Basic logarithmic amplifier circuit.

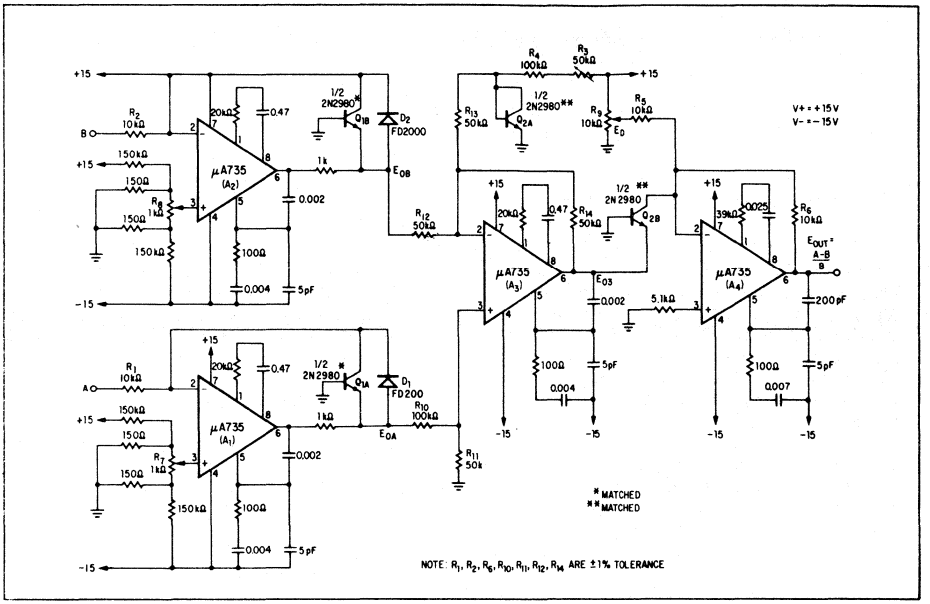


Fig. 2. Analog computer for the function $\frac{A-B}{B}$.

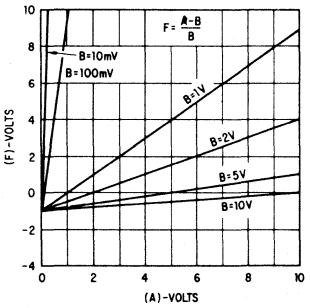


Fig. 3. Measured performance of the arithmetic computer.

ACTIVE FILTERS WITH GAIN USING THE μA725

Most active bandpass filters using operational amplifiers are complex unity gain circuits. This unity gain design technique effectively guarantees stability even with high dB/octave roll-off skirts. But, using the unity gain design approach forces the designer to add one or more additional amplifier stages to establish the system noise figure and to provide system gain.

The development and availability of the low noise, high gain μA725 operational amplifier allows a designer, for the first time, to design stable, low noise active bandpass filters with voltage gains > 1000 and Q's ≥ 10 using only one active device.

Figures 1 through 4 illustrate four such μA725 low frequency bandpass amplifier applications. Average performance characteristics are listed below each active filter design. Measured total harmonic distortion of all four active filters was $< 0.15\%$ at a 10V pk-pk output level. A 2kΩ resistive load was used for all tests. Power supply voltages were ±15V. Maximum current drain was 4.5mA from each supply. An equivalent generator source impedance of 33kΩ was maintained for all four active filters.

Figure 5 illustrates the basic active bandpass filter design approach. A bridged "T" null network is used to establish the center peaking frequency and Q of the bandpass amplifier. Maximum phase shift of a bridged "T" network is always $< 90°$ therefore amplifier stability is assured with the network inserted in the negative feedback loop of the operational amplifier.

Low frequency skirt roll-off is maintained by the input high pass corner CR network while the high frequency skirt roll-off is maintained by the normal compensation elements R_1C_1 and R_2C_2 and by the gain shunt capacitor C_3 located in the negative feedback loop of the operational amplifier. Figure 6 shows the intended bandpass shaping effects of these various RC networks.

Figure 7 is the basic bridged "T" circuit used.

The bridged "T" is actually a high pass corner element (CxRy) paralleled with a low pass corner element (RxCy). Useful null network equations are (reference Figure 7):

$$f_o = \frac{1}{2\pi R_x C_x \sqrt{b}} \quad (1)$$

$$\frac{E_{out}}{E_{in}} @ f_o = \frac{2}{2 + b} \quad (2)$$

$$Q = \frac{\sqrt{b}}{2} \quad (3)$$

If, f_o = null center frequency

$$Rx = Ry$$

$$b = \frac{Cy}{Cx}$$

$$\text{Load} = \infty$$

$$\text{Driving Impedance} = 0\Omega$$

Actually the driving impedance is not critical if it is kept relatively low with respect to the bridged "T" impedances. In the filters presented driving impedance can be $\leq 200\Omega$ with negligible effect on center null frequency or Q of the network. Loading does pull the center null frequency down somewhat to a lower frequency but does not dis-

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turb the Q of the network. This center frequency detuning effect caused by loading can be readily corrected by reducing the values of Rx and Ry slightly.

The bandpass amplifier gain at the center peaking frequency is given by equation (4).

$$\frac{Eo}{Ei} = \left[\text{DC Gain} + \left(\frac{2+b}{2}\right)\right] \bullet \frac{R}{R + \left(Rs\,\frac{1}{2\pi f_o C}\right)} \quad (4)$$

Refer to Figure 5 for R_S, R & C.

Refer to Figure 7 for f_o & b.

The 200Ω resistor in series with the μA725 operational amplifier output provides short proof protection at Eo and prevents high frequency instabilities due to capacitive loading.

If relatively high generator source impedances are desired along with a high input impedance to the bandpass amplifier we strongly recommend the placement of a grounded electrostatic shield between the input and output pins (& socket pins, if used) of any integrated circuit high gain operational amplifier. This will prevent high frequency radiation effects from disturbing the amplifiers noise figure and its high frequency response characteristics.

Center frequency and Q stabilities are controlled by the temperature coefficients of the resistors and capacitors used in the bridged "T". Thus stable components will produce a stable active filter.

Best noise figures will be obtained by using metal film or wirewound resistors for R and R_S (reference Figure 5) and by shielding the amplifier from 60Hz/& or stray RF radiations.

Figures 1 and 3 active filters use an additional attentuator leg in the negative feedback loop to keep the bridged "T" resistor values in a reasonable region.

The AC gain stability of this four active filters are effectively determined by the stabilities of the bridged "T" capacitor ratio $\frac{Cy}{Cx}$ and resistor ratio $\frac{Ry.}{Rx}$

The presented four active filters demonstrate the feasibility of designing stable, low noise active filters with gain, solely using one active component, the μA725.

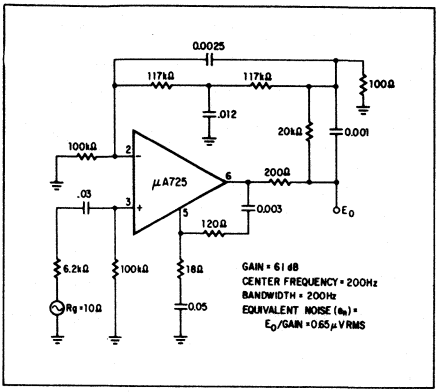


Fig. 1. Active bandpass filter.

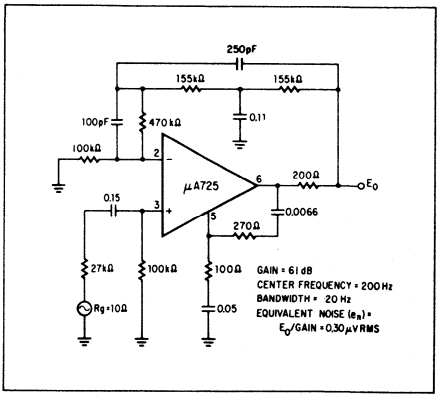


Fig. 2. Active bandpass filter.

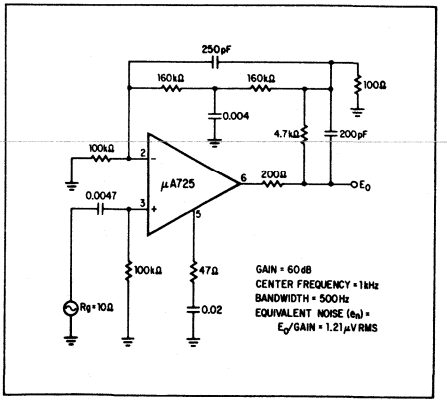


Fig. 3. Active bandpass filter.

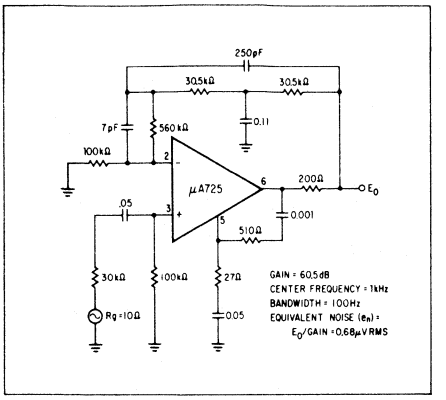


Fig. 4. Active bandpass filter.

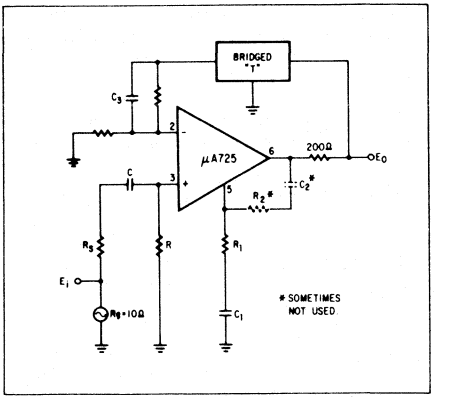


Fig. 5. Basic active bandpass filter.

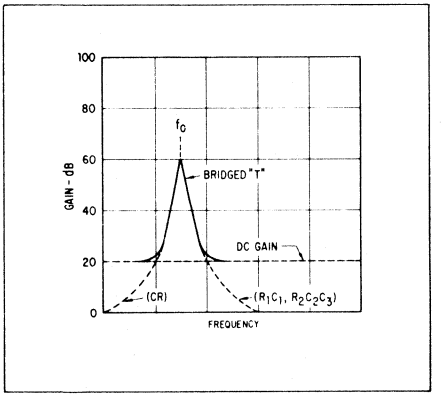


Fig. 6. Bandpass shaping effects.

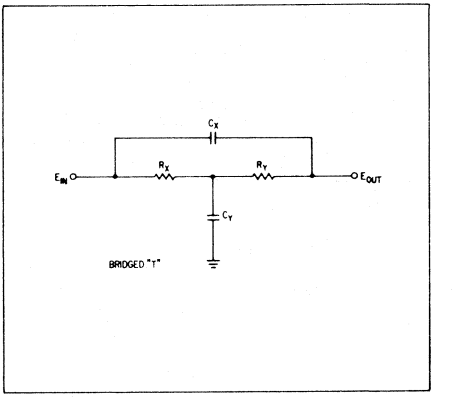


Fig. 7. Bridged "T".

MORE VOLTAGE REGULATOR APPLICATIONS USING THE μA723

FOLDBACK CURRENT LIMITING

As an alternative to the standard current limiting techniques, foldback current limiting may be used to advantage in any power supply situation in which the output device power dissipation under short circuit conditions becomes intolerable due to device and/or heat sink limitations.

A minimum parts cost method for providing the positive feedback necessary for foldback action is shown in Figure 1 and 2. The proper design equations are contained within the figures and apply for the full range of output voltages. This technique introduces the positive feedback by the increased current flow through the R_1, R_2 under short circuit conditions. This tends to forward bias the sensing transistor's base emitter junction, where the final percentage of foldback depends upon the relative current contributions of the voltage drop across R_2, and voltage drop across R_{SC} to the base current of the sensing transistor. Within the active region, in which both the R_2 voltage buildup and the R_{SC} voltage buildup are providing base current to the sensing transistor, recovery of the full output capability will take place whenever a short circuit is removed from the output. As soon as there is no voltage buildup across R_{SC} to provide a portion of the base current, then 100% positive feedback has been realized and a reset is required to restore normal operation once the short is removed.

From the start of base-emitter conduction to the full shut-off of the power supply series pass devices (require) only a two microamp base current is needed by the sensing transistor, which represents a ten millivolt increase in base-emitter voltage over the base-emitter threshold.

The latch condition or 100% positive feedback is generated by any change in the input voltage which increases the voltage drop across R_2 past the ten millivolts window with a short circuit applied, and can only be removed by breaking the positive feedback path by some manual reset to allow the series pass devices to once more be driven in a normal fashion.

The addition of an external transistor as shown in Figure 3 provides the same foldback limiting as Figures 1 and 2 but allows the extension of the active recovery region by several times that of the basic approach.

Since the latch problem comes about by the saturation of the current sensing transistor, the additional circuitry shown operates as an antisaturation circuit by bypassing base current above a value set by the voltage divider R_3, R_4 and the base-emitter threshold of the added device. Set up in this manner, the added transistor acts as a V_{BE} voltage regulator and (assuming a good thermal link) temperature tracks the threshold changes of the current sensing transistor, thus tending to keep the foldback current drive at a constant level.

To use this technique the foldback resistors R_1 and R_2 are calculated using the equation of Figure 3. The 2N3641 used for this application was selected both for a high base-emitter diode conductivity and reasonable beta at two microamp collector current.

Final adjustment under short circuit conditions occurs when P_1 in Figure 3 is set just above the point of minimum output current under short circuit and high AC line operation.

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Another approach to low power dissipation under short circuit condition is shown in Figure 4. This circuit does not follow the decreasing current, decreasing voltage load line which occurs with the standard technique; instead under a short circuit the output voltage decreases in a normal current limiting fashion (i.e. at a constant high output current) until the output voltage is below that necessary to keep the FET pinched off. As soon as the output voltage reaches the pinch-off voltage a low impedance path is established around the drivers and the output device which turns off the compound followers.

Recovery is accomplished by generation of a voltage across the normal load resistor by the bypass resistor R_1 which exceeds the pinch-off voltage of the FET whenever the short is removed.

NEGATIVE SHUNT REGULATOR

Low to medium negative output voltages may be regulated using no external active components, as shown in Figure 5. D_1 may either be a 1N746 zener diode or three forward-biased silicon diodes, depending on the maximum diode power dissipation which must be accommodated. The circuit as shown can handle up to 150 mA continuous current to ground, limited by the internal series pass transistor, and deliver from 9.5 to 40 volts to the load, governed by the minimum voltage required by the device together with its maximum high voltage rating.

THERMAL RESISTANCE

Data to date indicates a thermal resistance of 50°C per watt from junction to case to be a representative number using the die size of the μA723 in the TO-5 package.

Using this value, two forms of the standard thermal resistance relationship may be presented as follows:

$$P_d = \frac{150°C - T_A}{50°C/W + Q_{C\text{-}A}} \qquad (a)$$

or

$$Q_{C\text{-}A} = \frac{150°C - T_A}{P_d} - 50°C/W \qquad (b)$$

Where:

P_d = Power dissipation in watts

T_A = Maximum ambient temperature

$Q_{C\text{-}A}$ = Maximum thermal resistance required from case to ambient for a given power dissipation.

Using the above information either the maximum available power dissipation (eq. a), or the maximum allowable case to ambient thermal resistance (eq. b), may be derived for a given set of ambient conditions using the TO-5 package.

PREREGULATORS

Preregulators for use in power supplies take one of two forms.

(a) Fixed output circuit for use with limited output adjustment range supplies (Figure 6).

(b) Tracking preregulators which maintain a fixed minimum input – output differential (Figure 7).

In both cases the circuitry operates by holding the SCR gates at some DC potential which fires the forward-biased (anode to cathode) device whenever the ripple voltage on the filter capacitor drops to a level sufficient to exceed the gate to cathode threshold of the SCR.

Two precautions should be taken when either of the preregulator circuits is to be applied:

1. Since the firing of the SCR's is done on a DC drive basis this represents a "soft fire" (i.e. no gate overdrive) condition which should be considered when the power devices are selected.

2. R.F.I. should be considered in the application of these circuits as the SCR's operate effectively as phase control devices.

COMPLETE CIRCUITS

Two circuits have been included to show both the combination of several of the circuit techniques previously presented and the versatility built into the basic μA723 voltage regulator.

Figure 8 is a grounded configuration, tracking preregulator design which is adjustable from three volts to twenty-five using the transformer shown with the minimum input-output differential set by the 1N749 zener diode. The power for the regulators control portion is provided by a separate voltage source to insure efficient operation at low output voltages, while maintaining a voltage greater than the 9.5 volts minimum specified for

the μA723 internal circuitry.

Figure 9 again provides a controlled voltage across the series pass device, but due to the floating configuration used, the device is capable of regulation from 0 volts to 150 volts using the specified isolation transformers.

In this example the power for the integrated circuit is provided by the combination of the voltage doubler C_1, C_2, D_1, D_2 and SE7056 transistor buffered zener diode which provides approximately twenty volts for the regulator.

In both Figure 8 and 9 the maximum output capability is limited by the power components, such that the selection of a heavy duty transformer, diodes, SCR's and output devices will allow power capability expansion of the basic circuitry to fit any requirements.

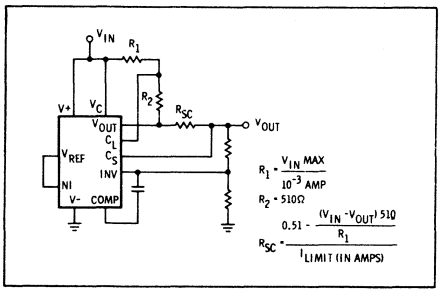


Fig. 1. Foldback current limiting — positive regulator.

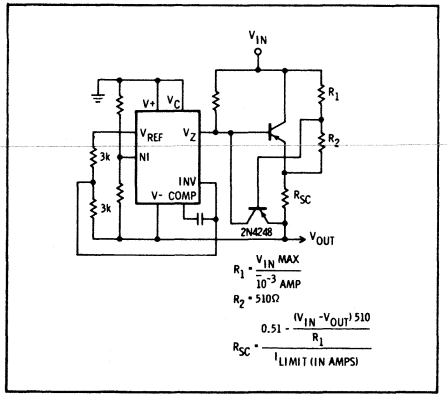


Fig. 2. Foldback current limiting — negative regulator.

CONCLUSION

The μA723 has been accepted as the industry standard for flexibility of application. The circuits presented here will allow the designer to further realize the inherent advantages of the basic device.

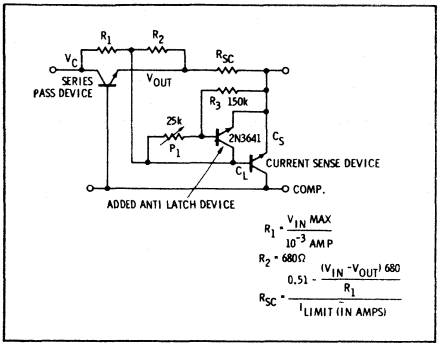


Fig. 3. Antilatch circuitry.

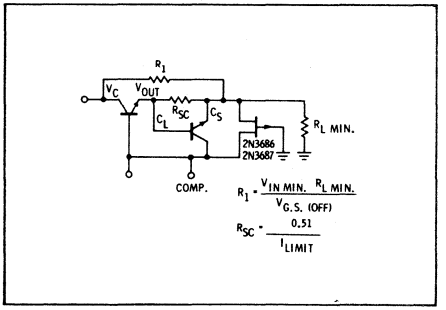


Fig. 4. FET foldback current limit.

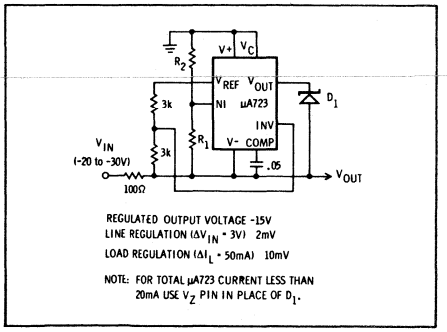


Fig. 5. Negative shunt regulator.

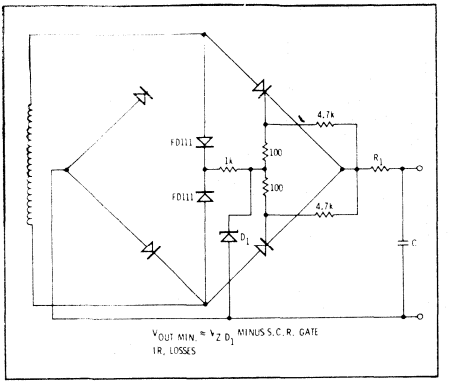


Fig. 6. Fixed output preregulator.

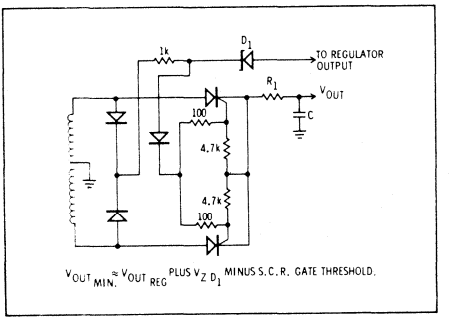


Fig. 7. V_{out} tracking preregulator.

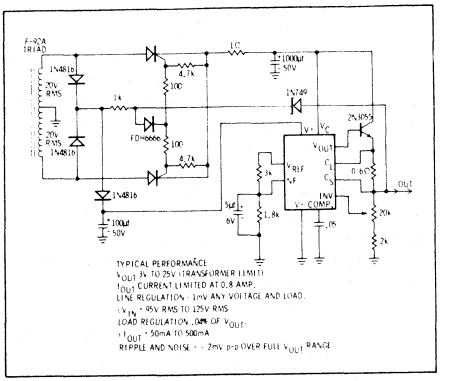


Fig. 8.

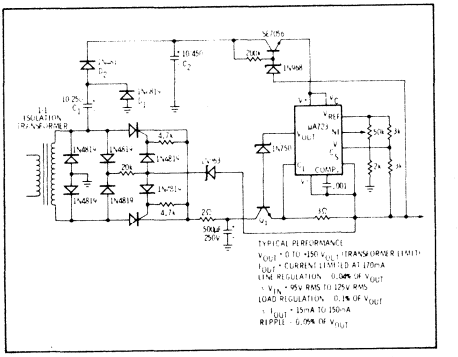


Fig. 9.

THE FREQUENCY DIVISION MULTIPLEX CHANNEL AMOLIFIER WITH THE μA748

THE FUNCTION

The amplifier in a Frequency Division Multiplex Telephone Channel End performs the task of driving the output transformer which powers the head set. The power required varies depending on individual specifications with +17 dBm being adequate for most requirements. The load must be isolated, with 600 ohms the adopted telephone standard.

The amplifier itself is characterized by its terminal impedance and power gain. To perform adequately as a channel amplifer, the circuit used must be capable of satisfying the performance characteristics required over the temperature range of the application. For commercial equipment −10°C to +65°C is adequate, and for the military −40°C to +85°C.

Since both the input and output impedance are 600 ohms, the characteristics of the amplifier response can be easily examined in terms of parameter variation. The circuit performance is described then by deviation from the desired goal.

THE CIRCUIT

The μA748 monolithic amplifier can be configured so that it will meet the channel amplifier requirements in FDM systems. Two circuits are presented; one using the standard −24V office battery, and the other using a balanced ±12V power supply. The IC parameters which are important to this application are:

1. Low power consumption
2. High power supply rejection
3. High gain
4. Good noise performance
5. High output current capability
6. Inherent short circuit protection
7. Flexible compensation

In systems using the standard office battery it is necessary to provide a reference for the positive input of the μA748. Figure 1 shows the basic circuit used in the channel amplifier application for single supply systems. R_1 and R_2 provide the reference, with the ratio of R_1 to R_2 offset slightly to compensate for unequal positive and negative output swing. C_2 has two purposes: 1) It decouples the input reference from power supply signals; and 2) It provides the signal path for transformer primary currents to ground. R_3 provides bias current for the plus input (pin 3). The functions of R_4, R_5, R_6, and R_7 are to bias the minus input (pin 2) and to control the gain and output impedance of the circuit. C_3 is the compensation capacitor (pin 1 to pin 8) which stabilizes the amplifier.

In many newer designs, balanced power supplies are available for channel end systems. The circuit of Figure 2 is then used with a reduction in the total component count in the system. In addition the impedance at the amplifier input and output are better controlled at low frequency.

CIRCUIT PERFORMANCE

The gain stability and frequency response of the circuit are significant performance parameters. Figures 3 and 4 give data on the variation of gain with temperature, and variation of passband fre-

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quency response with temperature. The amplifier linearity is plotted versus output level in Figure 5 for room temperature, and Figure 6 shows variation in signal distortion versus temperature for constant power output. The wideband frequency response is shown in Figure 7 for various temperatures.

Noise output from the circuit is −65dBm at room temperature with a noise bandwidth of 35kHz. The noise output in the voice band 200Hz to 4kHz is nominally −75dBm. Noise output varies approximately ±2dB from −40°C to +85°C.

The power dissipated in the circuit is shown in Figure 8. The class AB output of the μA748 operates at low quiescent bias so that the power dissipation with no signal is low; approximately 55 mW.

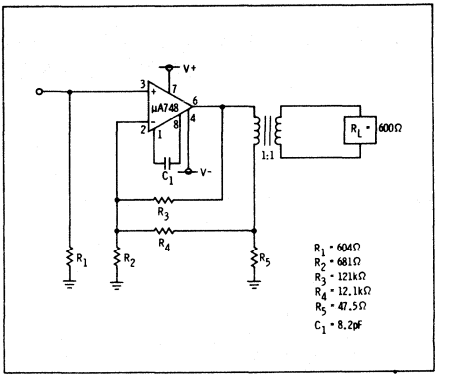


Fig. 2. Circuit for balanced power supply operation.

CIRCUIT ALTERNATES

The circuit shown operates with a gain of 100. For applications, such as PCM systems where a gain of 10 can be used, the compensation can be increased to give completely stable operation as a channel amplifier. Circuit values can then be adjusted to obtain the correct gain and terminal impedances.

In general, the μA748 can be used to supply voice band power in any requirement up to 100 mW peak power. The flexibility of the μA748 gives maximum power bandwidth, low distortion, high efficiency, and low component count.

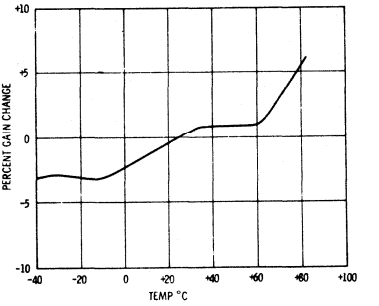


Fig. 3. 1kHz gain variation vs temperature.

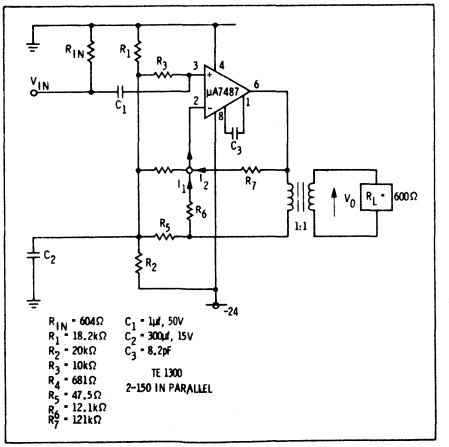


Fig. 1. Channel amplifier schematic.

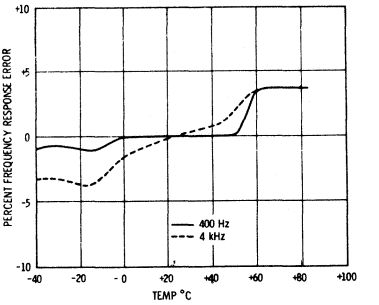


Fig. 4. Frequency response variation vs temperature.

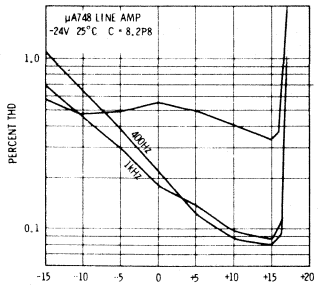


Fig. 5. THD vs P_O.

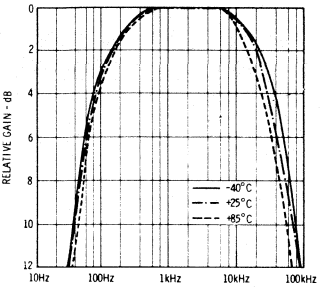


Fig. 7. Wide band frequency response.

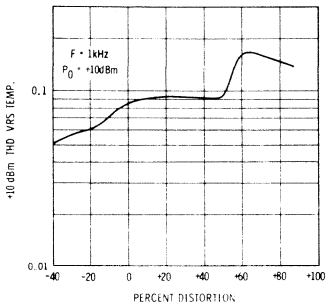


Fig. 6. THD vs temperature.

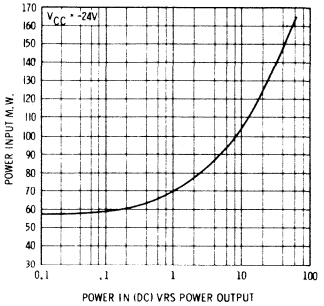


Fig. 8. Power input vs power output.

PERFORMANCE OF THE μA703 IN 100-MHz AND 200-MHz AMPLIFIERS AND 100-MHz HARMONIC MIXERS

ABSTRACT

The μA703 has a useful frequency range extending to slightly above 200 MHz. As such, it may be used either as an amplifier (saturating or non-saturating) or as a harmonic mixer. This Application Bulletin describes the performance of the μA703 in 100-MHz and 200-MHz amplifiers and as a harmonic converter or mixer from 100 MHz to 10.7MHz.

Description of μA703

The μA703 is a linear integrated circuit using two small high-frequency transistors as an emitter-coupled pair for RF amplification. These transistors are similar in some respects to the Fairchild 2N9918 transistors, which are also useful as amplifiers up to several hundred megahertz. Although the emitter-coupled pair has a higher noise figure than a single transistor, the μA703 provides a higher stability-limited power gain and a higher maximum available power gain (MAG). One advantage in integrating an emitter-coupled pair rather than using discrete transistors is a reduced reverse transfer capacitance. This is because each transistor is separated from other components by an isolation area connected to ground. Any bonding pads to which the external leads are connected can therefore lie over an isolation area instead of over the collector region, thus reducing the collector to emitter or collector to base reverse transfer capacitances. Refer to Figure 1.

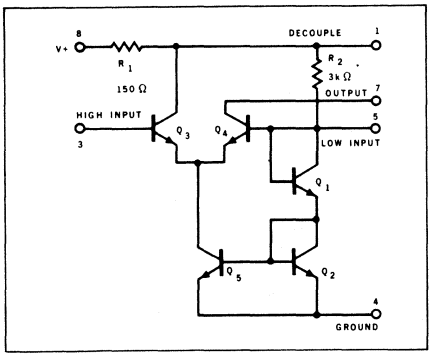


Fig. 1. μA703 schematic.

PERFORMANCE MEASUREMENTS

100-MHz Power-Gain

Figure 2 shows the schematic of the jig designed to measure the power gain of the μA703 at 100 MHz. As with all circuits using the μA703 at frequencies above 30 MHz,

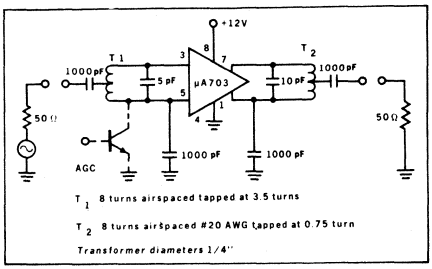


Fig. 2. 100-MHz test jig.

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the low-input terminal (pin 5, Figure 2) should be decoupled to ground. This is necessary for two reasons. First, the two diodes, Q_1 and Q_2 (or saturated transistors) between pins 5 and 4 do not perform as a perfect short-circuit and so do not completely decouple the base of the grounded-base transistor (Q_4) of the emitter-coupled pair. Second, the high-frequency current gain is falling off at 6 db per octave at frequencies above 30 MHz, resulting in more base current at high frequencies and, consequently, more RF current in the two decoupling diodes or external decoupling capacitors.

Without the bypass capacitance at pin 5, both the power gain and the gain figure at 100 MHz for μA703 are decreased by about 8 db under the parameters listed below

TABLE I.
TYPICAL μA703 PERFORMANCE.
(12-volt power supply, f = 100-MHz)

PARAMETER	MEASUREMENT
Power Gain	21.5 db
Noise figure	6 db
Bandwidth (-3 db)	5 MHz
Gain figure	$\left\lvert\frac{Y_{21}}{Y_{12}}\right\rvert^2 = 62$ db
Gain maximum stable	$\left\lvert\frac{Y_{21}}{Y_{12}}\right\rvert = 31$ db

The y parameters at 100-MHz are:

$y_{11} = 1.2 + j\ 3$mmhos

$y_{22} = 0.2 + j\ 1.5$mmhos

$\lvert y_{21}\rvert = 19$ mmhos

$\lvert y_{12}\rvert = 0.015$ mmhos

The μA703 may be used as current mode limiter if the total output admittance including g_{22} is greater than about 0.3 mmho. The power gain using the μA703 as a current mode limiter will be 21 decibels.

Reverse AGC may be obtained by bleeding current from pin 5, thereby reducing the value of the current in the emitter-coupled pair. This can be conveniently accomplished by the use of an external transistor shown in dotted out-line in Fig. 2.

200-MHz Power Gain

The jig (Figure 3) for the measurement of power gain and noise figure at 200-MHz is essentially the same as the one used at 100-MHz with, of course, changes in the values of the tuning components.

TABLE II.
TYPICAL 200-MHz μA703 PERFORMANCE.
(12-volt supply, f = 200-MHz)

PARAMETER	MEASUREMENT
Power gain	14 db
Noise figure	7.5 db
Bandwidth (-3 db)	10 MHz
Gain figure	41.5 db (Ratio of forward to reverse gain.)
Gain maximum stable	20.5 db

The y parameters for the μA703 at 200-MHz are:

$y_{11} = 2 + j\ 6.3$mmhos

$y_{22} = 0.7 + j\ 6.3$mmhos

$y_{21} = 12$ mmhos

$y_{12} = 0.12$ mmhos

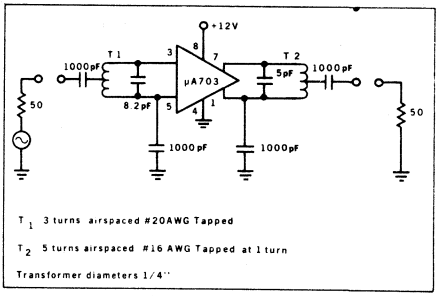


Fig. 3. 200-MHz test jig.

100-MHz Harmonic Mixer

The emitter-coupled pair is ideally suited for harmonic mixer applications but is not suitable for conventional mixing (i.e., where the IF frequency is equal to the sum or difference of the incoming signal and local oscillator signal). The reason for this is due to the unique properties of the g_m. If the emitter-coupled pair has the dc current in each transistor defined by a current source, as is the case of the μA703, then the g_m can be represented by the following expressions.

$$g_m = \frac{\frac{A i_k}{2}\, e^{-AVin}}{(e^{-AVin} + 1)^2} \qquad (1)$$

where $A = \frac{q}{kT} = 40$ (approx), and i_k = current defined by current source in milliamperes.

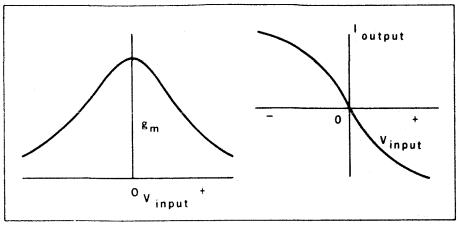


Fig. 4. Output current and g_m plotted against input voltage.

For mixer action to occur, the injected oscillator signal has to convert the g_m into a time-varying function. Therefore, if the injected oscillator voltage, $V_0\cos\omega_0 t$, is substituted in Equation 1 for V_{in}, the g_m becomes

$$g_m = \frac{-Ai_k e^{-AV_0\cos\omega_0 t}}{(e^{-Ai\cos\omega_0 t} + 1)^2} \qquad (2)$$

or

$$g_m = \frac{-Ai_k e^{-AV_0\cos\omega_0 t}}{(e^{-AV_0\cos\omega_0 t} + 2e^{-AV_0\cos\omega_0 t} + 1)} \qquad (3)$$

Expanding the exponential terms into power series,

$$g_m = \frac{-Ai_k\left(1 - AV_0\cos\omega_0 t + \frac{A^2V_0{}^2\cos^2\omega_0 t}{2!}\right.}{\left.4 - 4AV_0\cos\omega_0 t + 3A^2V_0{}^2\cos^2\omega_0 t - \frac{5A^3V_0{}^3\omega_0 t}{3} + \cdots\right)}$$

$$= i_k(B_0 + B_1V_0{}^2\cos^2\omega_0 t + B_2V_0{}^4\cos^4\omega_0 t + \cdots\cdots\cdots) \quad (4)$$

Equation 4 can be expressed by

$$g_m = a_0 + a_2\cos + \omega_0 t + a_4\cos 4\omega_0 t + \cdots\cdots\cdots\cdots \qquad (5)$$

The resultant g_m has a time-varying component at twice the oscillator signal frequency but no component at the oscillator frequency. Empirically, it has been verified that this second harmonic term increases as the square of the applied oscillator signal until about 50 mVs rms, then increases only slightly to about 100 mVs rms, after which it decreases.

The output current from the harmonic mixer is the product of the input signal and the time-varying g_m (assuming that the input signal is very small).

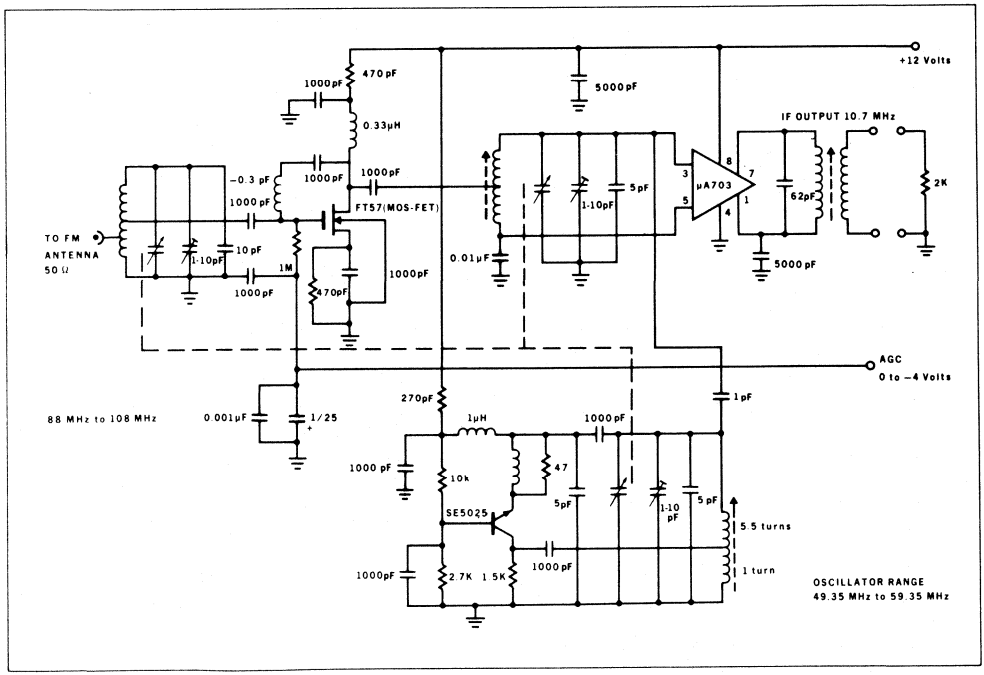


Fig. 5. FM tuner with μA703 harmonic mixer.

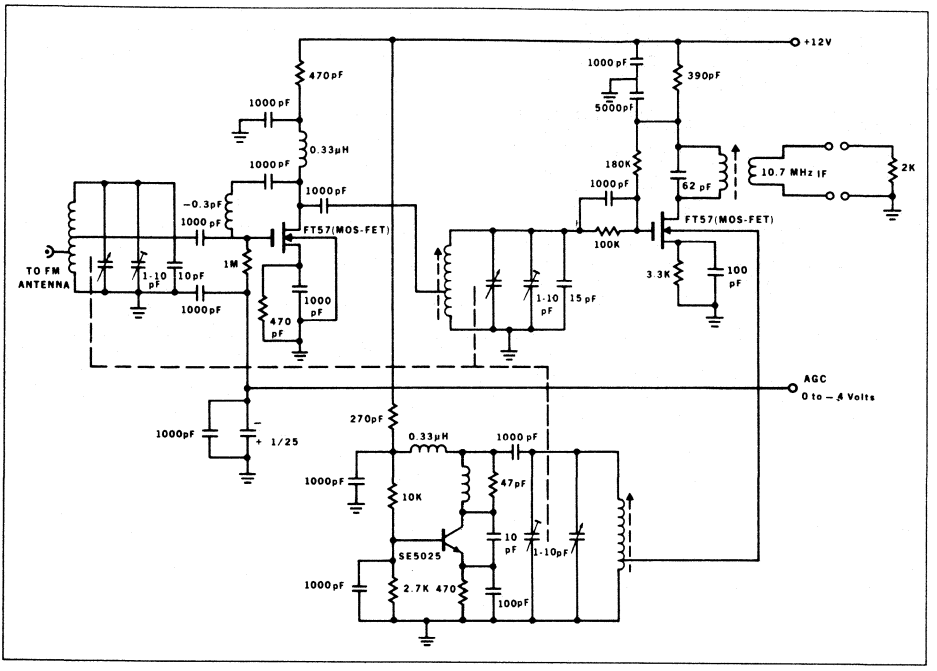


Fig. 6. FM tuner using MOS-FET transistors (FT 57).

Therefore, the output current,

$$I_{out} = g_m V_{in} \text{ (desired)}$$

$$= \acute{a}_0 \cos\omega_1 t + \acute{a}_2 \cos 2\omega_0 t \cos\omega_1 t + \acute{a}_4 \cos 4\omega_0 t \cos\omega_1 t + \text{--}. \quad (6)$$

Where $V_{in} = a \cos\omega_1 t$,

$$I_{in} = \acute{a}_0 \cos\omega_1 t + \frac{\acute{a}_2}{2} \cos(2\omega_0 + \omega_1)t + \cos(2\omega_0 - \omega_1)t + \frac{\acute{a}_4}{4} \left\{ \cos(4\omega_0 + \omega_1 t + \cos(4\omega_0 - \omega_1)t \right\} + \text{-----} \quad (7)$$

Equation 6 has some interesting implications which, at first sight, would appear to be applicable to FM tuners; namely, that the spurious responses should be zero, with the exception of the image response and that, since there are no third or odd harmonic terms, cross-modulation products should not exist. However, two assumptions were made in the analysis:

1) The transistors were assumed ideal.

2) The input signal would always remain small with respect to the injected oscillator signal (which) is not greater than 100 mV).

If the desired input signal is very large, the emitter-coupled pair will act as a switch and the mathematical complexity becomes extremely involved. Therefore, an FM tuner was used to evaluate the performance of the μA703 and to compare it for the consumer market with a MOS-FET in the mixer position.

Figures 5 and 6 show the FM tuner using both the μA703 and the FT57 MOS-FET. In both cases, the same RF amplifier and interstage transformer were used. The oscillator was modified to the minimum extent. The input admittance of the μA703 with about 100 mVs of oscillator signal injected is approximately 0.1 mmho; thereby allowing the μA703 to be coupled directly across the RF interstage transformer. For convenience, the oscillator voltage is injected into the "high" input of the μA703 through a 1-pf capacitance.

The gross overload of the tuner with the FT57 mixer is defined when the oscillator frequency is pulled by more than 10 KHz by the input signal to the tuner. The overload phenomenon with the μA703 mixer is due to the very rapid falloff of the conversion of g_m when the RF signal approaches and exceeds the oscillator signal in value. This action prevents the normal AGC from acting on the RF stage, because the falloff of mixer gain is at least as rapid as the increase in signal to the input of the tuner.

TABLE III.
COMPARATIVE PERFORMANCE DATA.
(With FM IF Amplifier and Conventional AGC Circuit)

PARAMETERS	TUNER WITH FT57 MIXER	TUNER WITH μA703 MIXER
Power Gain	20 db	31 db
Spurious rejection (IHF)	> 90 db	~70 db
Oscillator injection	600 mV	90 mV
Gross overload*	>200 mVs	~15 mVs

*Defined as maximum input signal to tuner prior to a limiting phenomenon.

The voltage gain from the antenna to the input of the μA703 mixer is between 25 and 30 db. It can be seen, therefore, that input signals in excess of 3 mVs will have an amplitude at the input of the μA703 similar to that of the oscillator.

The estimated power gain of the μA703 as a harmonic mixer in the FM tuner is about 14 db. No attempt was made to optimize the power gain by changing the output circuit matching.

As an experiment, the μA703 was operated as a conventional mixer to determine how closely theory agreed with practice. With an oscillator injection voltage of 100 mV to 200 mV at 110.7 MHz (IF frequency 10.7 MHz) and the desired signal at 100 MHz, the minimum insertion loss of the mixer was found to be about 15 db.

CONCLUSION

The μA703 has very useful power gain to frequencies in excess of 200 MHz and very low noise figures for an emitter-coupled pair configuration. In general, the μA703 is stable in any conventional small-signal amplifier at any frequency with conjugate input matching, and output matching either conjugate or less than 30,000 ohms, whichever is lower. The noise figure starts to increase at frequencies in excess of 50 MHz from about 4 db and is typically only 7.5 db at 200 MHz. Due to the inherent characteristics of an emitter-coupled pair of transistors, conventional sum and difference mixers are not possible. However, the μA703 is ideally suited for harmonic mixer applications to about 200 MHz, with good conversion gain and low noise.

ACKNOWLEDGMENT

The author gratefully acknowledges the analysis of the harmonic mixer by Hermann Ebenhoech.

APPENDIX

Equation 3 is rewritten here:

$$g_m = -Ai_k \left[\frac{e^{-AV_0\cos\omega_0 t}}{e^{-2AV_0\cos\omega_0 t} + 2e^{-AV_0\cos\omega_0 t} + 1} \right]$$

Dividing numerator and denominator by $e^{-AV_0\cos\omega_0 t}$ yields:

$$g_m = \left[\frac{Ai_k}{2 + e^{-AV_0\cos\omega_0 t} + e^{+AV_0\cos\omega_0 t}} \right]$$

since $e^{-AV_0\cos\omega_0 t} + e^{+AV_0\cos\omega_0 t} = 2\cosh(AV_0\cos\omega_0 t)$,

the result can be expressed as:

$$g_m = \frac{-Ai_k}{2} \left[\frac{1}{1 + \cosh(AV_0\cos\omega_0 t)} \right] \qquad (3a)$$

The cosh function is sketched in Figure 6. Let $\cos\omega_0 t$ go from +1 to -1 and back. It is not difficult to see that at $\cos\omega_0 t$ equal to -1, the cosh function has the same value as for $\cos\omega_0 t$ equal to +1. Therefore, $g_m(t)$ will have the same value in both cases. This means that g_m will twice attain the value corresponding to $\omega_0 t$ equal to zero, while $\omega_0 t$ varies from zero to 2π. Therefore, the g_m is periodic in $2\omega_0 t$.

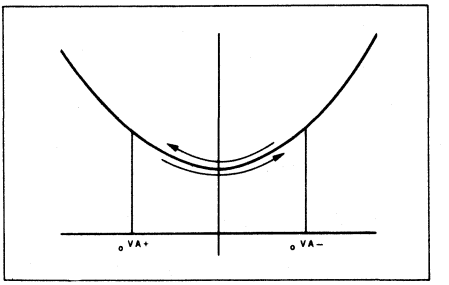


Fig. 7. Cosh function.

Let us call $2\omega_0 t = \omega_1 t$. Then the Fourier expansion of g_m will contain all harmonic frequencies of ω_1, or (in terms of ω_0), $2\omega_0 t$, $4\omega_0 t$, $6\omega_0 t$, ...

Therefore, no odd-order harmonics of ω_0 will appear in the output.

A LOW-DRIFT, LOW-NOISE MONOLITHIC OPERATIONAL AMPLIFIER FOR LOW LEVEL SIGNAL PROCESSING

INTRODUCTION

The field of low level signal processing and precision analog computation has been the exclusive domain of high-priced, discrete, chopper-stabilized operational amplifiers. A new monolithic amplifier, designated the μA725, with superior input characteristics, has been designed to compete with these discrete devices. It features low offset voltage and low current drift with temperature and time, low noise, high power-supply rejection, high common-mode rejection and range and extremely high open-loop gain. A closed-loop gain of 1000 ±.03% is possible.

A new process has been developed which offers transistors with high β (for both NPN's and lateral PNP's), low noise, excellent β linearity at low currents, and low output conductance. The combination of new process and circuit techniques makes the μA725 ideal for the instrumentation and low level signal processing fields. Additional attributes of the μA725 are: output and input short circuit protection, offset voltage nulling capability, no latch-up when common-mode range is exceeded, operation over a wide range of supply voltages (±3V to ±20V, with a gain of 250,000 at ±3V).

CIRCUIT DESCRIPTION

Input Stage

The circuit diagram of Figure 1 illustrates the main design philosophy of the input stage: *There is no substitute for simplicity where matching of devices is a primary criterion*. The number of transistor junctions in the input signal path must be kept at a minimum for best input offset voltage and current matching and for lowest input noise figure. Thus, PNP-NPN input stage configurations as well as "punch-through" or cascode configurations must be avoided since they increase the number of sources of input error. In addition, active collector loads must be avoided since they do not exhibit the matching or temperature tracking of resistive loads and may be subject to g_m modulation from substrate current variations.

The μA725 utilizes the simplest input configuration: two differentially connected transistors with well-matched resistor loads. The two input transistors shown in Figure 1 are each physically two parallel connected devices, Q_{1A}, Q_{1B}, Q_{2A}, Q_{2B}. They are biased by current source Q_3 and loaded by matched resistors R_1 and R_2. The placement of the input quad is in a criss-cross fashion as shown in Figure 2. This configuration substantially reduces thermal gradient effects. The importance of this configuration is obvious if one considers that variations occuring in output stage power dissipation or in the location of the heat generating components can cause thermally induced input errors.

As an example, for a heat source at point P in Figure 2, the effective temperature differential between the cross-connected input pairs is 2a/b (or 16 times less for the μA725) than between two input devices (say Q_{1A}, Q_{2B}) only. Although the Q_{1A}-Q_{2B} temperature differential is minute, it should be remembered, that even a .01°C difference is equivalent to a 25μV change in offset voltage because $\Delta V_{BE}/\Delta T \cong -2.5$mV/°C for silicon transistors. Since the aforementioned ±.03% closed-loop gain stability is achieved by

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keeping the open-loop gain over one million under all conditions (i.e. less than 10μV produces a 10V output), a 25μV change in input would be disastrous. This temperature gradient effect is practically eliminated by the unique geometrics employed in the μA725.

An additional bonus of the large area input quad arrangement is that the matching of input devices is significantly improved. Therefore, the performance of matching dependent parameters such as input offset voltage, input offset current, common-mode rejection, and power-supply rejection are superior to that hitherto obtainable.

The presence of the input quad introduces the concept of three dimensional matching. Just as first order thermal gradients are eliminated by the quad pair, first order diffusion variations (the third dimension) are also removed because the effective "centers of gravity" of Q_{1A}, Q_{1B} and Q_{2A}, Q_{2B} coincide, while centers of neighboring pairs are separated by six mils or more.

Second Stage

The major consideration in the design of the second stage is to diminish its influence on input noise, offset, and drift. Although the gain of the first stage attenuates second stage effects, careless layout and high second stage current levels can result in considerable error contributions at the input. Therefore, the current levels are low and emitter followers Q_6 and Q_9 are used to limit the loading of the first stage; Q_7, Q_8, and Q_6, Q_9 are carefully matched. Current sources Q_{10}, Q_{16}, and Q_{17} maintain constant V_{BE} match in the second stage and provide constant impedance load to the first stage. The combination of Q_{11} and Q_{12} retains the full differential gain of the second stage, while converting from differential to single-ended output. The high impedance load in the second stage provides high gain and allows frequency stabilization at a single compensation point (pin 5).

Driver and Output Stage

The minimum current in the driver transistor Q_{22} is fixed by current source Q_{13} and results in a highly linear output swing. Transistors Q_{18} and Q_{19} provide the proper bias for class AB operation of the output power transistors Q_{21} and Q_{26} and prevent cross-over distortion in the output. In addition Q_{19} is connected in an emitter follower configuration providing low output resistance even with h_{FE} variations in Q_{26}.

Short Circuit Protection

The output current limiting is provided by Q_{23} which prevents overload of Q_{21} and current source Q_{25} limiting the base current drive of Q_{26}. The currents in Q_{22} and Q_{25} are limited by the normally off transistor Q_{24}, which becomes active when the output is overdriven and removes the base drive.

FREQUENCY COMPENSATION

The open-loop and closed-loop frequency response curves are shown in Figures 3 and 4 for the various gain configurations. Note that the μA725 does not require compensation at the input. The advantages are the reduction in the number of external components required for frequency stability and the elimination of noise pickup and stray feedback from the output to the collectors of the input quad.

The requirement for low current levels in the second stage and the capacitance required for single terminal compensation reduce unity gain slew rate. However, this is not a disadvantage since this amplifier is designed for low level signal processing applications where high closed-loop gain configurations are used. At high gains the μA725 slew rate is over 5V/μS as shown in Figure 5, better than other general purpose operational amplifiers available today.

PERFORMANCE

Typical electrical performance is summarized in Table I. Three of the parameters are of special interest because they have been obtained using new concepts in operational amplifier design. These are offset voltage drift with temperature (TCV_{OS}), closed-loop gain stability, and common-mode rejection ratio (CMRR).

Minimizing Offset Voltage Drift With Temperature

It is a well known property (see Reference 1) of differential amplifiers, such as shown in Figure 6, that:

$$TCV_{OS} = \frac{V_{OS}(T)}{T} \qquad (1)$$

or $TCV_{OS} = 3.3\mu V/°C$ for every millivolt of offset voltage at 25°C

It follows from eq. (1) that if V_{OS} is adjusted to zero by some nulling procedure, TCV_{OS} will be zero. The offset nulling resistor is external and its temperature coefficient (TC) may differ significantly from the diffused resistor TC's. A parameter Θ can be defined as the difference between the nulling resistor's TC and the diffused resistor's TC. If R_{X1} is used externally to null the amplifier as shown in Figure 8, it can be shown that:

$$TCV_{OS} \cong [V_{OS}\ (\text{unnulled}) \times \Theta] + [V_{OS}\ (\text{nulled}) \times 3350\ \text{ppm/°C}] \quad (2)$$

Although the V_{OS}/T term of Eq. (1) is indeed eliminated by nulling, a new drift term is introduced. If Θ = 2500 ppm/°C which is typical for film resistors, TCV_{OS} is reduced by only 25% – an insignificant improvement over the initial unnulled drift.

Similarly, if R_{X2} is the nulling potentiometer:

$$TCV_{OS} \cong \frac{R_{X2}}{R_{X2} + 2(R_1 + R_2)} \times V_{OS}\ (\text{unnulled}) \times \Theta \quad (3)$$

This procedure is used to null several of the operational amplifiers available today. Since $R_{X2} >> R_1 + R_2$ because of other design considerations, the drift is basically the same as in the previous case.

If R_p is used to null in Figure 8, two degrees of design freedom are introduced: the ratios R_1/R_2 and R_p/R_2. The only restriction on these ratios is the capability to null out all possible offset voltages. Depending on the values used, TCV_{OS} can range from $-V_{OS}$ times Θ to $+V_{OS}$ times Θ. Thus a value can be determined such that the drift is zero. A computer evaluation of the rather involved functional relationship between TCV_{OS} and V_{OS} with R_1/R_2 and R_p/R_2 as parameters yields the optimum values shown in the circuit diagram of Figure 1, and ensures that the effect of the TC differential Θ is negligible. A more detailed discussion of temperature drift is presented in Appendix I.

Closed Loop Gain Accuracy

The closed loop gain (A_{CL}) of an amplifier may be expressed as:

$$A_{CL} = -\frac{\alpha}{\beta}\left[\frac{1}{1 + \frac{1}{\beta A_{OL}}}\right] \quad (4)$$

where: A_{OL} = open loop gain
α = attenuation factor
β = feedback factor
α/β = "ideal" gain

In this expression α/β is the ideal gain. For best noise figure and lowest drift alpha should be as close to one as possible. Expanding the bracketed expression above in a power series, the accuracy of A_{CL} can be found to be:

$$\epsilon(\%) \cong \frac{100}{\beta A_{OL}} \quad (5)$$

thus if β = .001 and the desired ϵ is 0.1% then A_{OL} = 1,000,000 min.

Common Mode Rejection

One of the most important parameters of operational amplifiers is common mode rejection ratio (CMRR). If, for example, we wish to amplify a 100μV differential voltage superimposed on a one volt common-mode signal and the amplifier only has a 100μV/V (80dB) CMRR, the output voltage can be zero. This is not an uncommon requirement, yet most operational amplifiers today do not guarantee more than 80dB CMRR. Thus very high common mode rejection of over 110dB is required in instrumentation applications.

It can be shown that CMRR, in volts/volts, in terms of circuit parameters is:

$$CMRR = \frac{kT}{q}\ \Delta\gamma \quad (6)$$

where γ is the current normalized output conductance of the input devices Q_1 and Q_2 and $\Delta\gamma$ is the difference between the two γ's. Eq. (6) holds if the output conductance of current source Q_3 is significantly less than that of Q_1 and Q_2 and if the voltage drop across R_1 and R_2 is much larger than any possible second stage offset voltage. The typical 120dB CMRR for the μA725 has been obtained by the following:

(1) developing a process which features high β, low noise, and low output conductance of the input transistors (gamma);
(2) closely matching the input quad and thereby obtaining a low value of $\Delta\gamma$.

Additional details on CMRR theory that include the constraints on eq. (8) are presented in Appendix II.

APPLICATIONS

The μA725 has been designed specifically for low level signal processing applications such as signal conditioners, instrumentation amplifiers, precision measuring equipment, data acquisition systems, telemetry and process controls.

In these applications, it is recommended that stable precision thin film resistors be used to take advantage of the full capabilities of the μA725. In applications where CMRR is important, the input resistor bridge ratios must be trimmed to better than 10 ppm to prevent imbalances and the resulting degradation of CMRR. In addition, the input capacity on each input must be balanced to within 1pF in order to obtain good CMRR with frequency.

Ground lands and shields should be used as extensively as possible to prevent coupling unwanted signals from the output to the input. If remote zero adjust is desirable (more than 2 inches), pins 1 and 8 should be decoupled with 0.1μF capacitors to V^+ and cables to the remote null pot should be shielded to reduce noise pick up and prevent unwanted coupling to null pins.

CONCLUSIONS

A new instrumentation operational amplifier has been built which makes extensive use of Second Generation technologies. The low offset drifts, low input currents, low noise performance and massive open loop gain make the device an ideal choice for low level signal processing applications.

APPENDIX I
MINIMIZING OFFSET VOLTAGE DRIFT WITH TEMPERATURE IN MONOLITHIC OPERATIONAL AMPLIFIERS

INTRODUCTION

It is a well known property of differential amplifiers, such as shown in Figure 7', that input offset voltage (V_{OS}) drift with temperature (TCV_{OS}) is substantially reduced by operating the two transistors with equal base-emitter voltages (V_{BE}) instead of with equal collector currents (I_C). To illustrate this simply, the starting point is the standard equation relating I_C to V_{BE}

$$I_C = I_S\, e^{(q\, V_{BE}/kT)} \qquad (1)$$

from which

$$V_{diff} \cong V_{BE1} - V_{BE2} = \frac{kT}{q} \ln\left(\frac{I_1}{I_2} \times \frac{I_{S2}}{I_{S1}}\right) \qquad (2)$$

and

$$V_{OS}(T) \cong V_{diff}(T)_{\,I_1 = I_2} \qquad (3)$$

Differentiating (2) with respect to temperature yields:

$$TCV_{OS} \cong \frac{dV_{diff}}{dT} = \frac{V_{diff}}{T} + \frac{kT}{q} \frac{\frac{d}{dT}(I_1/I_2)}{I_1/I_2} + \epsilon \qquad (4)$$

where ϵ is an error term. If $I_1 = I_2$, then $\frac{V_{OS}}{T}$ dominates the equation for TCV_{OS}. The significance of ϵ will be discussed later. Therefore, if V_{diff} is forced to zero by making $V_{BE1} = V_{BE2}$, TCV_{OS} is diminshed. This statement hinges on the assumption that the second term of (4) is negligible.

When V_{diff} is set to zero by some external adjustment of the input stage of a monolithic operational amplifier the second term of eq. (4) does become appreciable. The nulling network must optimize for minimum TCV_{OS}. This appendix presents the details of obtaining this optimum nulling method.

NULLING METHODS

The nulling is usually accomplished by shorting the inputs together and therefore forcing V_{diff} to zero. The resulting collector current mismatch is approximately

$$e^{\left(\frac{qV_{OS}}{kT}\right)}$$

or 4% for initial V_{OS} of 1mV. This is cancelled by adjusting the resistors loading the differential pair to make the input voltage to the following stages zero. This implies that:

$$I_1 R_a = I_2 R_b \text{ at } T_o \qquad (5)$$

where R_a and R_b are equivalent resistances loading Q_1 and Q_2, respectively; T_o is the temperature at which the nulling is performed usually room temperature.

From eqs. (2), (3), and (5)

$$V_{diff}(T_o) = 0 = \frac{kT_o}{q} \ln \frac{I_{S2} I_1}{I_{S1} I_2} = \frac{kT_o}{q} \times \ln \left[\frac{I_{S2}}{I_{S1}} \frac{R_b}{R_a} \times (T_o) \right] \quad (6)$$

and

$$V_{OS}(T_o) = \frac{kT_o}{q} \ln \left(\frac{I_{S2}}{I_{S1}} \right) = \frac{kT_o}{q} \ln \left(\frac{R_a}{R_b} \right) \approx -\frac{kT_o}{q} \times \frac{\Delta R}{R_b} \left(1 + \frac{\Delta R}{2R_b} \right) \approx -\frac{kT_o}{q} \frac{\Delta R}{R_b} \approx -\frac{kT_o}{q} \frac{\Delta R}{R_a} \left(1 - \frac{\Delta R}{2R_a} \right) \approx -\frac{kT_o}{q} \frac{\Delta R}{R_a} \quad (7)$$

where $\Delta R = R_b - R_a$ and $V_{OS} << \frac{kT}{q}$

If the error term of (4) is neglected, then

$$TCV_{OS} = \left. \frac{dV_{diff}}{dT} \right|_{T = T_o} = \frac{kT_o}{q} \times \frac{R_a}{R_b} \times \frac{d}{dT} \left(\frac{R_b}{R_a} \right) = \frac{kT_o}{q} \times \frac{R_a}{R_b} \times \frac{d}{dT} \left(\frac{\Delta R}{R_a} \right) \quad (8)$$

Figure 8 shows three different means of nulling operational amplifiers. R_X, R_Y, and R_P are external nulling potentiometers; the R_L's are well-matched diffused resistors. The temperature coefficients (TC) of the potentiometers and diffused resistors will differ significantly; a new parameter Θ can be defined as this TC difference:

$$\Theta = (\text{TC of } R_L) - (\text{TC of nulling potentiometer}) \quad (9)$$

Θ is typically 2500 ppm/°C for diffused silicon resistors and a thin film potentiometer. If R_X is used to null, and Θ is assumed constant with temperature, then:

$$\frac{R_b}{R_a}(T_o) = \frac{R_L}{R_L \parallel R_X} = 1 + \frac{R_L}{R_X} ; \frac{\Delta R}{R_a} = \frac{R_L}{R_X} \quad (10)$$

and

$$\frac{R_b}{R_a}(T) = 1 + \frac{R_L(1 + \Theta (T - T_o))}{R_X} \quad (11)$$

$$\frac{d}{dT} \left[\frac{R_b}{R_a} (T) \right] = \frac{R_L}{R_X} \times \Theta \quad (12)$$

from eqs. (7), (8), (10), and (12), nulling with R_X yields:

$$V_{OS} \cong -\frac{kT_o}{q} \times \frac{\Delta R}{R_b} \approx -\frac{kT_o}{q} \times \frac{R_L}{R_L + R_X} \quad (13)$$

if $R_X >> R_L$

$$TCV_{OS} = \frac{kT_o}{q} \times \frac{R_X}{R_L + R_X} \times \frac{R_L}{R_X} \times \Theta \approx -V_{OS} \times \Theta \quad (14)$$

Although the dominant $\frac{V_{OS}}{T}$ term of eq. (4) is indeed eliminated by nulling with R_X, the new drift term due to the resistor TC differential reduces the initial, unnulled drift by only 25%. If R_Y is the nulling potentiometer, an involved but elementary calculation results in:

$$TCV_{OS} \approx -\frac{R_Y}{R_Y + 2R_L} \times V_{OS} \times \Theta \quad (15)$$

Equation (15) is obtained by finding the equivalent expressions to (10), (11), and (12) and then substituting into the general equations (7) and (8). Nulling with R_Y is the method used for several of the operational amplifiers available today. Since $R_Y >> R_L$, the drift is essentially the same as in the previous case.

THE OPTIMUM NULLING NETWORK

If R_P is used to null, two degrees of design freedom are introduced, namely the ratios R_1/R_2 and R_P/R_2; in the previous two cases there are no degrees of freedom at all. The only constraint on these ratios is the capability to null out all possible offset voltages. An explicit relationship between TCV_{OS} and V_{OS} in the form of equations (13) and (15) is difficult to obtain, but (7) and (8) can be utilized to develop expressions for V_{OS} and TCV_{OS}. After some considerable algebra, the results are:

$$V_{OS} = \frac{kT}{q} \times \frac{a - 2z}{z[1 + (b + 1)(a - z)] + b(1 + a)} \quad (16)$$

$$TCV_{OS} = \Theta \times \frac{kT}{q} \times \left[f(a - z) - f(z) \right] \quad (17)$$

where

$$f(z) = \frac{z}{(1 + z)[b(1 + z) + z]} \quad (18)$$

and

$$a = \frac{R_P}{R_2} ; b = \frac{R_1}{R_2} ; z = \frac{R_{Pb}}{R_2} \quad (19)$$

A computer can then evaluate (16) and (17) with z as the independent variable and a and b as parameters and plot TCV_{OS}/Θ vs. V_{OS} for various values of a and b. Depending on the parameter values, TCV_{OS} can range from $-V_{OS}\,\Theta$ to $+V_{OS}\,\Theta$. Thus a and b may be selected such that the nulled drift closely approaches zero.

Figures 9 and 10 illustrate the TCV_{OS} variations with V_{OS}, a, and b. Only positive offset voltages are shown; the curves are symmetrical about the origin. If a is between 1.5 and 4, and b lies within 1 and 5, the TCV_{OS}, in general, will be less than 1.0μV/°C.

DEVIATIONS FROM THEORY

The error term ϵ of eq. (4) represents the difference between the actual TCV_{OS} and that predicted by theory. In functional form

$$\epsilon = \frac{kT}{q}\frac{d}{dT}\left(\ln\frac{I_{S2}}{I_{S1}}\right) + TCV_{OS}\,(\Delta TCR_L) + TCV_{OS}\,(V_{OS2}) + TCV_{OS}\,(I_{OS2}) \qquad (20)$$

The definitions and particulars of the various terms of eq. (20) are as follows:

(a) $\frac{kT}{q}\frac{d}{dT}\left(\ln\frac{I_{S2}}{I_{S1}}\right)$ arises from the differentiation of (2) and is typically less than ±0.5μV/°C.

(b) $TCV_{OS}\,(\Delta TCR_L)$ is due to the temperature coefficient mismatch of diffused resistors R_L (ΔTCR_L). From (8)

$$TCV_{OS}\,(\Delta TCR_L) \approx \frac{kT_o}{q} \times \Delta TCR_L \qquad (21)$$

Therefore, a one percent mismatch in TCR_L yields a 0.6μV/°C drift (25 mV x 0.01 x 2500 ppm/°C ≈ 0.6μV/°C).

(c) $TCV_{OS}\,(V_{OS2})$ is the effect of the offset voltage of the second stage (V_{OS2}) which is attenuated by the gain of the input stage, A_{V1}

$$A_{V1} = \frac{qI_1}{kT} \times R_{eq} \qquad (22)$$

where R_{eq} is the equivalent resistance loading Q_1. Hence, from (4)

$$TCV_{OS}\,(V_{OS2}) = \frac{TCV_{OS2}}{A_{V1}} \approx \frac{V_{OS2}}{T} \times \frac{kT}{qI_1 R_{eq}} \qquad (23)$$

For typical operational amplifiers $V_{OS2} < 5$ mV, $I_1 R_{eq} > 500$ mV, therefore $TCV_{OS}\,(V_{OS2}) < 0.8\mu V/°C$.

(d) $TCV_{OS}\,(I_{OS2})$ is the contribution of the offset current drift of the second stage (TCI_{OS2}) reduced by the first stage gain

$$TCV_{OS}\,(I_{OS2}) = \frac{TCI_{OS2}R_{eq}}{A_{V1}} = TCI_{OS2}\,\frac{kT}{qI_1} \qquad (24)$$

A survey of the more popular monolithic operational amplifiers indicates that typical values for $TCV_{OS}\,(I_{OS2})$ range from 0.3μV/°C to 0.8μV/°C.

If an operational amplifier with 1.0μV/°C or less TCV_{OS} is required, the error component ϵ is obviously not negligible and can easily exceed 1.0μV/°C. With very careful chip layout and second stage design, these error terms cannot be disregarded but can certainly be reduced. Yet ϵ was neglected in (4). The justification for this is that ϵ is random; consequently, no functional relationship can be established between TCV_{OS} and ϵ at the design stage as shown in Figure 11. The general equation for TCV_{OS}, equation (8), and the curves of Figures 9 and 10 still provide the best available estimate for TCV_{OS}.

CONCLUSION

We have shown that arbitrary nulling does not provide the desired results to compensate externally for changes in input offset voltage with temperature. Optimum nulling networks can be devised to minimize this effect. First and second amplifier stages can be designed very close to ideal conditions necessary to match an external nulling scheme. An amplifier that provides this superior performance with temperature is the μA725.

APPENDIX II
IMPROVING THE COMMON-MODE REJECTION OF OPERATIONAL AMPLIFIERS

One of the most important parameters of operational amplifiers is common-mode rejection ratio (CMRR). If, for example, amplification of a 100μV differential voltage is superimposed on a one-volt common-mode signal and the amplifier has only a 100μV/V (or 80dB) CMRR, the output voltage could be zero. This is not an unreasonable application, yet most operational amplifiers today do not have more than 80dB

CMRR. CMRR has been the unwanted stepchild parameter of operational amplifiers. Designers aim for other improvements and accept the resulting CMRR. Probably the main reason for this is that simple, workable design formulae have not been developed for CMRR in terms of transistor and processing parameters.

In Reference 4 an expression was developed for CMRR of a differential amplifier as shown in Figure 12. An extension to include the effects of the load resistor mismatch, ΔR_L, result in

$$CMRR = \frac{g_o}{g_m}\left[\frac{\Delta g_m}{g_m} - \frac{\Delta g_o}{g_o}\right] x\left[1 + \frac{R_L}{2R_{o3}}\right] + \frac{1}{2R_{o3}g_m}\left[\frac{\Delta g_m}{g_m} + \frac{\Delta R_L}{R_L}\right] \quad (1)$$

where:

CMRR is in volts/volt
R_{o3} is the output resistance of current source Q_3
g_o, g_{o2} are the output conductances of Q_1 and Q_2, respectively
$\Delta g_o = g_{o2} - g_o$
g_m, g_{m2} are the transconductances of Q_1 and Q_2, respectively $\left(\cong \frac{qI_c}{kT}\right)$
$\Delta g_m = g_{m2} - g_m$

R_L, R_{L2} are the loads on Q_1 and Q_2, respectively, including the input resistance of the second stage. R_L may be a resistor or the output resistance of an active load
$\Delta R_L = R_{L2} - R_L$

Reducing this rather unwieldy equation to a clear, precise form, one may proceed as follows:

Since g_m = constant x I

then:

$$\frac{\Delta g_m}{g_m} = \frac{\Delta I}{I} \quad (2)$$

where

$$\Delta I = I_2 - I$$

From Figure (1)

$$V_{OS2} = I R_L - I_2 R_{L2} \quad (3)$$

or

$$\frac{V_{OS2}}{I R_L} = 1 - \frac{(I + \Delta I)(R_L + \Delta R_L)}{I R_L} \approx \frac{\Delta I}{I} + \frac{\Delta R_L}{R_L} \quad (4)$$

An expression for g_o can be derived using the fact that

$$I = I_c \text{ and } I_c \approx \frac{1}{W_B} \quad (5)$$

and

$$W_B = W_{BM} - X_{dE} - X_{dC} = (W_{BM} - X_{dE}) - \sqrt{\frac{2K_s\epsilon_o}{q}\frac{N_C}{N_B^2}(V_{CB} + V_D)} \quad (6)$$

where

W_B is the effective base width;
W_{BM} is the metallurgical base width;
X_{dE} is the reduction in base width due to the emitter depletion region;
X_{dC} is the reduction in base width due to the collector depletion region (step junction approximation);
$K_s\epsilon_o$ is the permittivity of silicon;
N_C and N_B are the collector and base concentrations, respectively;
V_{CB} is the collector base voltage;
V_D is the built-involtage of the collector-base junction.

From (5) and (6) and since W_{dE} does not change at constant V_{BE}:

$$g_o \left.\frac{dI_C}{dV_{CE}}\right|_{V_{BE} = \text{constant}} = \left.\frac{dI_C}{dW_B}\frac{dW_B}{dV_{CE}}\right|_{V_{BE} = \text{constant}} = \frac{dI_C}{dW_B} x \frac{dW_B}{dV_{CB}} = \frac{I_C}{W_B}\sqrt{\frac{K_s\epsilon_o N_c}{2qN_B^2(V_{CB} + V_D)}} \quad (7)$$

If a new parameter γ, the current-normalized output conductance, in volts^{-1}, is defined as

$$g_o = \gamma I$$

$$g_{o2} = \gamma_2 I_2$$

$$\Delta\gamma = \gamma - \gamma_2 \quad (8)$$

$$\gamma = \frac{1}{W_B}\sqrt{\frac{K_s\epsilon_o N_C}{2qN_B^2(V_{CB} + V_D)}}\ ; \quad (9)$$

then

$$\frac{g_o}{g_m} = \frac{kT}{q}\gamma \quad (10)$$

From (2) and (8)

$$\frac{\Delta g_m}{g_m} - \frac{\Delta g_m}{g_o} = \frac{\Delta I}{I} + \frac{\Delta\gamma}{\gamma} - \frac{\Delta I}{I} = \frac{\Delta\gamma}{\gamma} \quad (11)$$

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Substitution of (4), (10), and (11) into (1) yields

$$CMRR = \frac{kT}{q} \times \gamma \times \frac{\Delta\gamma}{\gamma} \times \left[1 + \frac{R_L}{2R_{O3}}\right] + \frac{V_{OS2}}{I\,R_L} \times \frac{1}{2R_{O3}g_m} \tag{12}$$

The output resistance of the current source Q_3 is

$$R_{O3} = \frac{\left(1 + \frac{qI_3}{kT} \times R_3\right)}{g_{o3}} \approx \frac{1 + \frac{qI_3}{kT} \times R_3}{2g_o} \tag{13}$$

where g_{o3} is the output conductance of transistor Q_3. $g_{o3} \approx 2g_o$ because $I_3 \approx 2I$, however, this relationship is only approximate since the collector-base voltages of Q_3 and Q_1 are unequal. Therefore, in (12)

$$\frac{R_L}{2R_{O3}} << 1$$

even if R_L is the output resistance of an active load, and consequently its value approaches $1/g_o$. This is true because usually $\frac{qI_3}{kT} R_3 > 1$ in (13).

Also from (10) and (13):

$$\frac{1}{2R_{O3}}\ g_m \approx \frac{g_o}{g_m\,(1 + qI_3 \times R_3)} = \frac{kT}{\left(1 + \frac{qI_3}{kT} \times R_3\right)} \times \frac{kT}{q}\gamma \tag{14}$$

For well designed operational amplifiers $V_{OS2} < 5$ mV, $I\,R_L > 500$ mV. Hence:

$$\frac{V_{OS2}}{I\,R_L} \times \frac{1}{2R_{O3}\,g_m} = \frac{V_{OS2}}{I\,R_L} \times \frac{1}{1 + \left(\frac{qI_3}{kT}\right) R_3} \times \frac{kT}{q}\gamma << \frac{kT}{q}\gamma\,\frac{\Delta\gamma}{\gamma} \tag{15}$$

even if $\Delta\gamma/\gamma = 0.01$, which is about the best γ matching one can expect. Therefore, (12) further reduces to the simple form

$$CMRR = \frac{kT}{q}\Delta\gamma \tag{16}$$

CONCLUSIONS

The following can be concluded from eq. (9) and eq. (16):

1. CMRR is independent of operating current if conditions of (9) and (16) are met.
2. Increasing transistor β by narrowing the base width seriously degrades CMRR[1].

From statement 2 above, "punch-thru" or collector starvation techniques, which yield "super beta" transistors, will degrade CMRR. But from statement (1), devices may be operated at very low collector currents without degrading CMRR, thus allowing operation with low input currents. The μA725 makes use of the above facts and obtains its low input currents by operating input devices at low collector currents and by using a process which increases, bulk lifetimes and eliminates emitter-base pinch-off in the input devices, thus maintaining constant beta at these low current levels.

The excellent CMRR performance has been obtained without the use of complex circuitry such as cascodes or CMRR feedback by developing a low $\Delta\gamma$ process. The resulting simple differential pair also provides excellent input offset voltage and current matching.

1 This occurs because $\gamma \approx 1/W_B$ and the γ matching of two adjacent transistors deteriorate. For example, a 0.1 micron W_B mismatch is 10% for $W_B = 1$, but is five times as much for $W_B = 0.2$. Figure 13 illustrates the experimental results which indicate that:

$$CMRR \cong \beta^{-1.25}.$$

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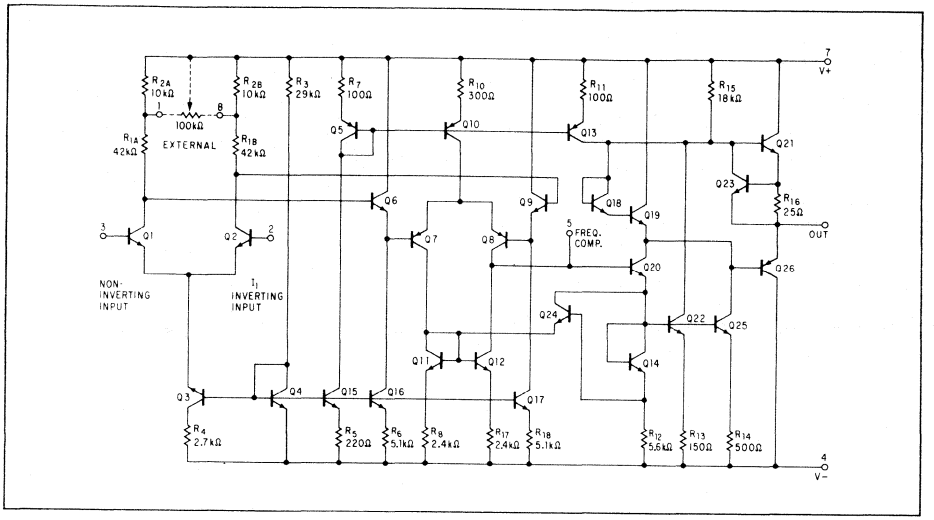


Fig. 1. Schematic diagram of the μA725.

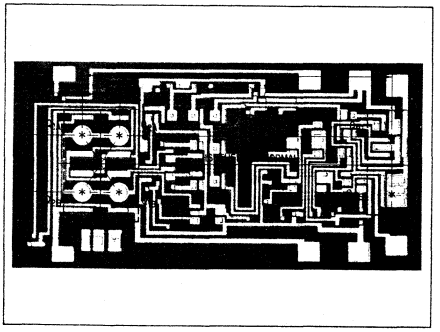


Fig. 2. Overlay of μA725 die.

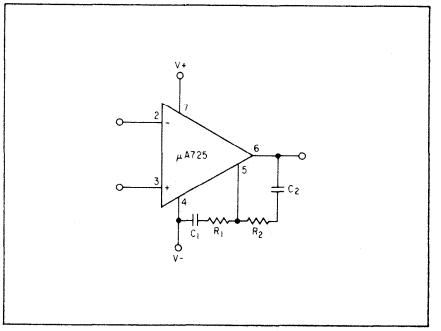


Fig. 4. Frequency compensation connection diagram.

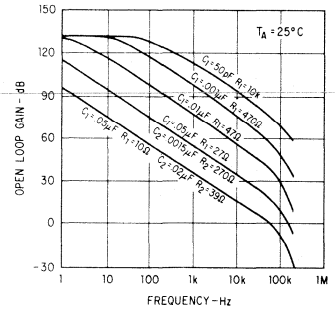


Fig. 3. Open loop response for various values of compensation.

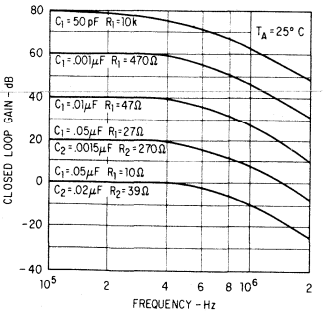


Fig. 5. Frequency response for various closed loop gains.

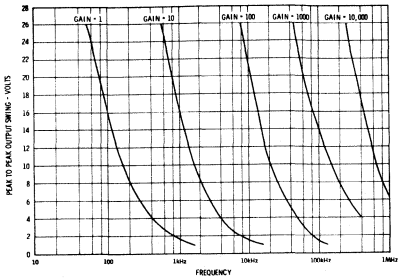


Fig. 6. μA725 maximum undistorted sinusoidal output vs. frequency.

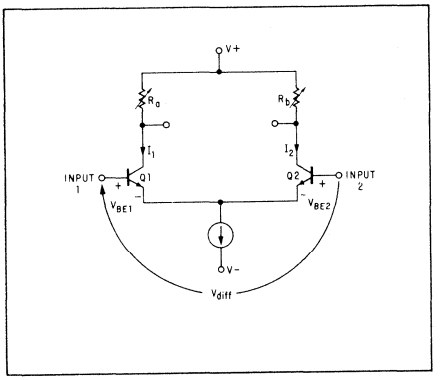


Fig. 7. Differential amplifier.

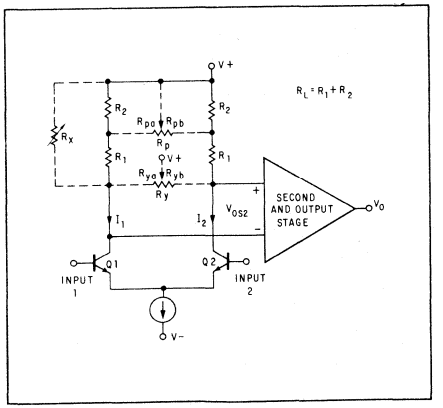


Fig. 8. Three ways of nulling operational amplifiers.

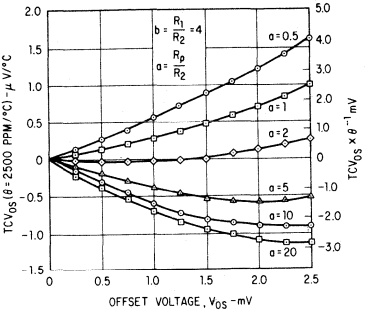


Fig. 9. Temperature drift of input offset voltage as a function of input offset voltage.

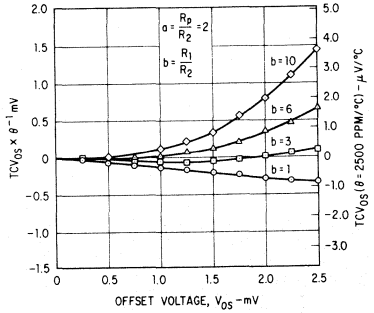


Fig. 10. Temperature drift of offset voltage as a function of input offset voltage.

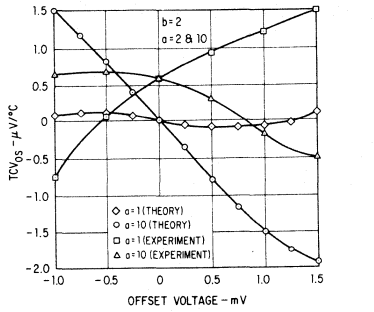


Fig. 11. Theoretical and experimental offset voltage drift.

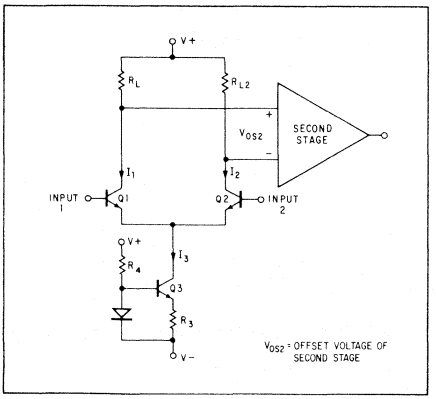


Fig. 12. Operational amplifier input stage.

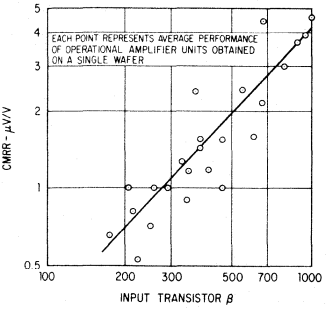


Fig. 13. Common mode rejection ratio of operational amplifiers as a function of input transistor beta.

Table I

Typical Electrical Characteristics T_A = +25°C V_S = ±15V unless otherwise specified			
Parameter	Conditions	Value	Units
Input offset voltage	$R_S \leq 10k\Omega$	0.6	mV
Temperature coefficient	External nulling	0.6	μV/°C
Drift per day		1.5	μV
Input offset current		3	nA
Temperature coefficient		10	pA/°C
Input bias current		45	nA
	T_A = −55°C	115	nA
Large signal voltage gain		$4x10^6$	
Closed loop gain stability	$R_L \geq 2k\Omega$	1000±.06	%
Common mode rejection ratio	$R_S \leq 10k\Omega$	120	dB
Power supply rejection ratio	$R_S \leq 10k\Omega$	120	dB
Output voltage swing	$R_L \geq 2k$	±13	V
Common-mode input voltage		±14	V
Input noise current	f_o = 10Hz ΔF= 1Hz	.7	pA
voltage	f_o = 10Hz ΔF = 1Hz	11	nV
Input resistance		1.6	MΩ
	T_A = −55°C	.5	MΩ
Output resistance		130	Ω
Slew rate gain: 10,000	$R_L \geq 2k$	40	V/μsec
gain: 1,000	$R_L \geq 2k$	6	V/μsec
Bandwidth (Closed loop gain = 1)		600	kHz
(Closed loop gain = 1000)		500	kHz
Power dissipation, quiescent		90	mW

μA725 INSTRUMENTATION APPLICATIONS

INTRODUCTION

Any designer with an instrumentation application requiring a transducer to voltage conversion scheme needing sensitivity, stability and simplicity should closely examine the capabilities of the μA725 instrumentation amplifier. The high gain, low drift and low noise features of the μA725 make it an extremely attractive integrated circuit for transducer/system interfacing.

The following paragraphs describe some typical μA725/transducer applications.

PHOTO-AMPLIFIER

A photomultiplier tube and its inherent disadvantages such as high price, stable high voltage supply requirement, aging effects, and large physical volume can be replaced with a PIN photodiode/μA725 combination. Matching a PIN photodiode with the μA725 integrated circuit supplies the user with a low noise, linear photo-detection system only requiring low voltage power supplies. This new detection system is capable of replacing photomultiplier tubes now used in laboratory instruments such as photofluorometers, colorimeters, photelometers, spectrophotometers, photo-nephelometers, flame photometers and other light sensing applications.

Figure 1 shows the schematic of such a photodetection system using the μA725. Figure 2 illustrates the implementation of an actual photofluorometer design.

Capacitor C_1 in both designs controls the bandwidth of the low-pass filter amplifier and can be selected as required by the designer.

The PIN photodiode indicated on the schematic has a useable spectrum range from less than 400 millimicrons to over 1,050 millimicrons. The PIN photodiode could also be capacitively coupled to the μA725 for photo-chopping applications with the μA725 set up as a low noise, high gain bandpass amplifier with or without AGC (see Application Briefs #132 "Active Filters With Gain Using the μA725" and #130 "μA725 AGC Amplifier").

PIEZO-ELECTRIC TRANSDUCER AMPLIFIER

Realizing that a trade-off exists between loading and required following gain for a piezo-electric transducer, one feasible design approach is presented in Figure 3. This μA725 circuit DC couples the crystal transducer and then provides a stable gain of 1000 over a 40kHz bandwidth. Equivalent noise as referenced to the input was 14.3 μV rms.

BRIDGE AMPLIFIERS

Figures 4 and 5 are schematics of general μA725 low frequency bridge amplifiers suitable for strain gauge, thermistor, photo-conductive cells or any other variable resistance sensor application.

The Figure 4 circuit has been designed for a sensitivity of 15Ω/volt output or a 3% change/volt and readily provides a linear ±10V swing into 2k resistive load. Its bandwidth is DC to 620Hz.

The Figure 5 circuitry has a sensitivity of 1.5Ω/volt output or a 0.3% change/volt with the same load and output swing capability of the Figure 4 circuit. The bandwidth has been set at 3kHz.

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SEMICONDUCTOR

Equivalent input noise as referenced to the input was Figure 4 was 0.19μV rms and Figure 5 was 0.57μV rms.

THERMOCOUPLE AMPLIFIER

The low noise μA725 amplifiers shown by Figures 6 and 7 provides low frequency stable gains of 100 or 1000 with −3dB bandwidths of approximately 600Hz. This circuit configuration is also suitable for other low impedance, millivolt source transducers. Equivalent input noise referenced to the input was 0.24μV rms.

GENERAL μA725 DESIGN CONSIDERATIONS

Other gains, bandwidths, and source resistance values can be easily obtained with the μA725. Those presented in this report were selected to demonstrate the versatility of the μA725 in low pass amplifier configurations.

The μA725 noise figure is near optimum with a source resistance of about 100kΩ. Care should be exercised in layout of components, wiring, and shielding when using high source resistance values with any high gain operational amplifier. Unwanted radiation feedback can effect the amplifiers noise figure and high frequency response characteristics.

All circuits presented in this article have been tested with a 2kΩ resistive load and provides an undistorted 10 volt peak-to-peak signal over their specified bandwidths. The μA725, unlike other integrated circuit operational amplifiers having Class AB output stages, has no cross-over distortion characteristic due to an exclusive output stage design.

Figures 1 through 3 illustrate a technique of obtaining high feedback ratios by using a two-stage voltage divider. This provides stable gains even with high source resistance values.

Capacitive bypassing of the supply pins of the integrated circuit is highly recommended, especially if there is any appreciable lead length between the integrated circuit and its power supplies.

A 100kΩ, metal film offset potentiometer between pins 1 and 8 with the wiper connected to 7 is recommended for the μA725 if offset nulling and/or exceptional DC stability is required.

SUMMARY

The μA725 provides the circuit/system designer with an excellent instrumentation amplifier for interfacing to any type of low/high level transducer, especially when reliability and stability are important features of the design.

Common mode and power supply rejection ratios of 120dB and 2μV/V respectively of the μA725 are excellent and provide good DC stability and excellent linearity for all user circuits.

Reliable ±1% metal film resistors with temperature coefficient of less than 200ppm/°C are recommended if gain and drift stability is required by the circuit designer.

High resistance carbon composition resistors are notorious "leakers" above 100kHz and their usage in feedback gain control loops will seriously effect the high frequency stability and response characteristics of any operational amplifier. Non-inductive wirewound resistors have sufficient stray capacitance to affect the high frequency response of any operational amplifier when used in gain control feedback loops, and as such, their use should be avoided.

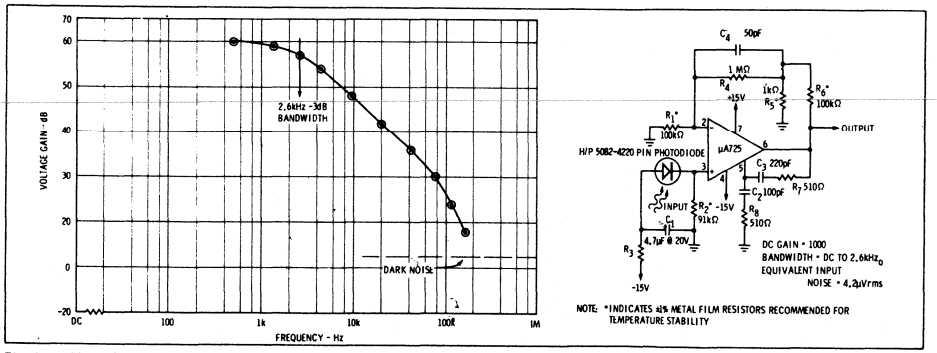


Fig. 1. Simplified PIN photodiode amplifier. Frequency Response.

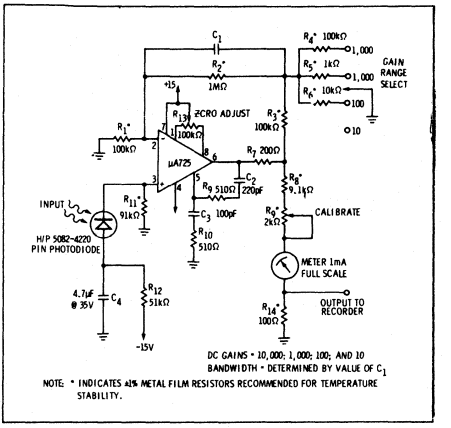


Fig. 2. Complete PIN photodiode amplifier.

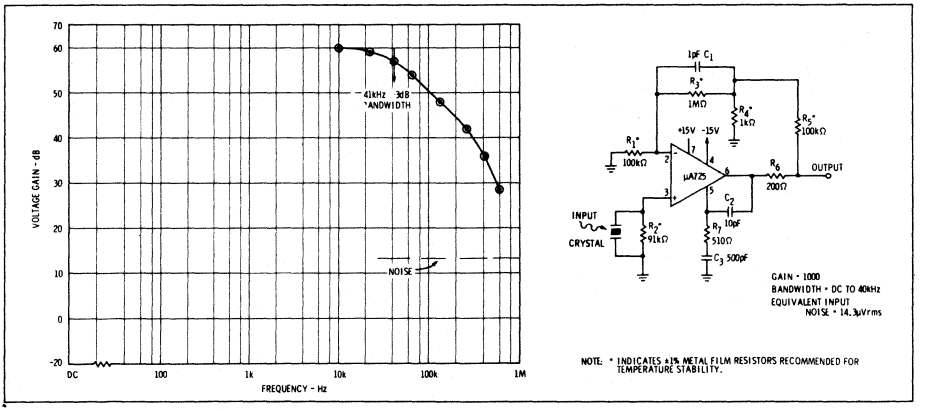


Fig. 3. Piezo-electric transducer amplifier. Frequency Response.

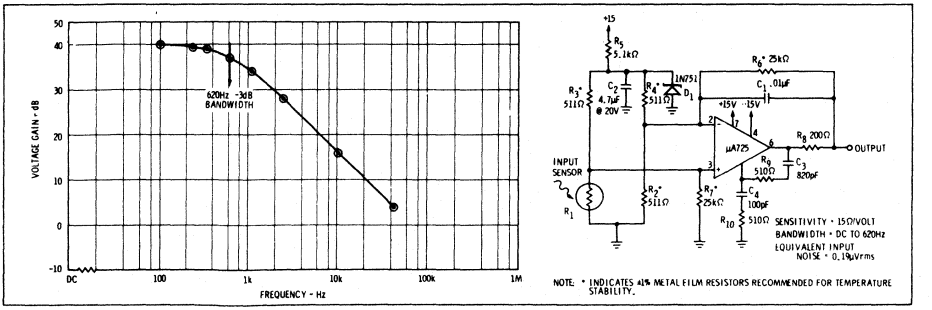


Fig. 4. Bridge amplifier #1. Frequency Response.

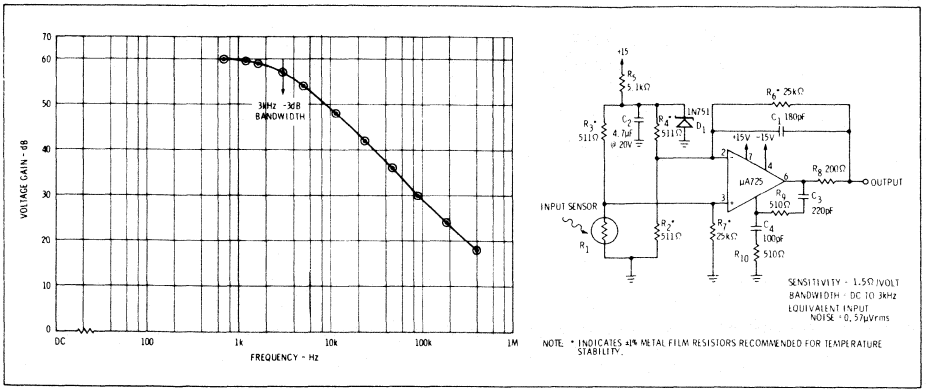


Fig. 5. Bridge amplifier #2. Frequency Response.

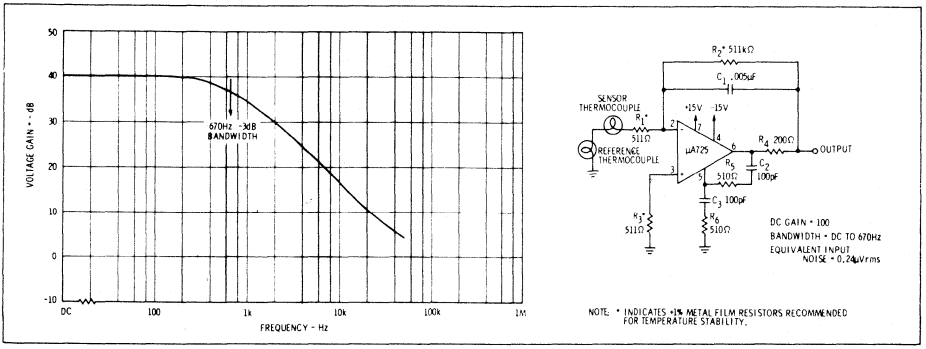


Fig. 6. Thermocouple amplifier #1. Frequency Response.

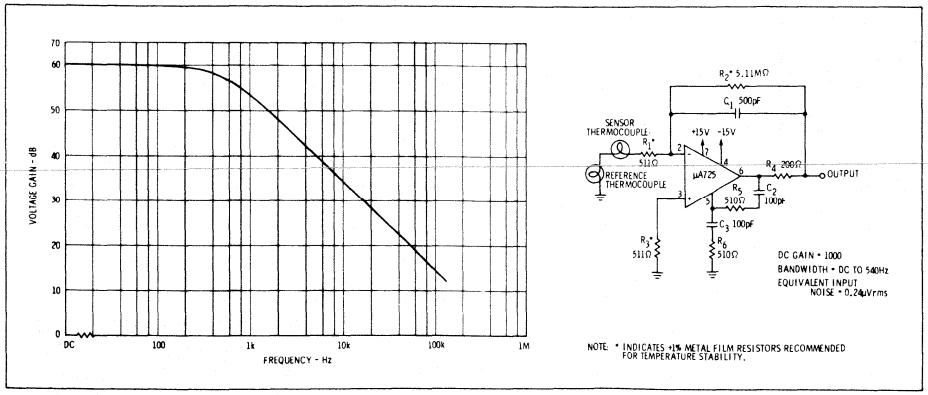


Fig. 7. Thermocouple amplifier #2. Frequency Response.

A MINIMUM COMPONENT μA749 VOLTAGE-TO-FREQUENCY CONVERTER WITH 1% ACCURACY

Instrumentation and control systems often face the following problem: Sensors that monitor physical system conditions produce a d-c output level which must be transmitted some distance to display or central processing equipment. Unfortunately, the analog signal can be altered in transmission by effects such as capacitave loading, transmission losses, and noise pickup. The result is a reduction in system accuracy.

These deficiencies can be circumvented by converting the D.C. signal level into a pulse train whose frequency is a linear function of the analog input level. This digital signal is then easily transmitted from the sensor location to the control system and reconverted to an analog voltage by clipping and integrating the pulses.

The voltage-to-frequency converter described here is both simple and accurate. It provides better than ±1% accuracy over a wide range of frequencies while using only two active components: the μA749 and an NPN transistor.

BASIC OPERATION

The first stage of the dual-wideband operational amplifier circuit (see Figure 1) is an integrator which produces a negative ramp proportional to the applied V_{in} (a positive voltage). This ramp is applied to the (-) input of a comparator whose (+) input is held at -4 volts. As soon as the integrator output reaches -4 volts, the comparator output switches into the ON state and transistor Q_1 has the multifunction role of providing an output pulse, resetting the ramp generator's integrating capacitor, and defining the beginning of the following negative ramp by holding the comparator (+) input at zero volts until the end of the reset interval. The circuit is then free to begin another cycle.

Because the reset interval is very rapid when compared with the ramp, the repetition rate (frequency) of the output pulse is defined almost entirely by the integrator's ramp period, leading to the circuit's excellent overall conversion accuracy.

TIMING INTERVAL

At the beginning of the timing interval:

1. The integrator output = 0 volts.
2. The comparator output is OFF.
3. The comparator (+) input is at -4 volts due to the R_5, R_6 divider.

The ramp generator output forms a negative slope with this relationship:

$$\frac{\Delta V_{out}}{\Delta T} = \frac{V_{in}}{R_1 C_1} \qquad (1)$$

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The timing period ends when the comparator's (-) input reaches its (+) input trip voltage (-4 volts), and the comparator output switches ON. The length of the interval is therefore defined by:

$$T_1 = \frac{4R_1C_1}{V_{in}} \qquad (2)$$

RESET TIME

At the beginning of the reset interval:

1. The integrator output = -4 volts.
2. The comparator output and Q_1 are ON.

When the comparator output switches ON, Q_1's emitter current causes the comparator's (+) input reference voltage to switch from -4 volts to approximately zero volts. At the same time, the collector current sinks the integrator's summing junction, thus causing the ramp generator's output to reset at a rate approximately defined by equivalent resistor R*.

This represents the sum of all the major current limiting components in the integrating capacitor discharge path:

$$R^* = R_{\text{pin 1 output stage}} + R_9 + R_{CE\ Q1} + R_6 \qquad (3)$$

$$= 250\Omega + 100\Omega + 25\Omega + 1300\Omega$$
$$= 1675\Omega$$

If this is inserted into the timing formula given in (2), with R_1 replaced by R* and V_{in} by -15 volts, then:

$$T_2 = \frac{4\ R^*C}{V_{\text{-supply}}} = \frac{4(1675)\ (0.1)\ 10^{-6}}{15}$$
$$= 44.5\ \mu S \qquad (4)$$

(This value has been experimentally confirmed.)

The primary limitation on the rate of discharge is set by R_6 (1.3KΩ). R_9 controls the collector path current at the moment of turn OFF (at the end of the reset interval) so that the comparator will always switch back OFF at exactly zero volts. In this sense, the first, second and third terms in (3) form a divider with R_6 during reset.

When C_1 has been discharged so that the comparator's (-) input is again zero, the comparator output switches OFF. This interrupts base drive to Q_1, turning if OFF and permitting the comparator's (+) input to return to -4 volts. At the same time, the interrupted collector current removes the ramp generator's summing junction current sink.

TOTAL TIMING CYCLE

The total period for each cycle is the sum of T_1 and T_2. Stating this in terms of the components:

$$T = T_1 + T_2 = \frac{4R_1C_1}{V_{in}} \quad \frac{4R^*C_1}{15} =$$

$$4C_1 \left(\frac{R_1}{V_{in}} + \frac{R^*}{15} \right) \qquad (5)$$

For most practical situations the term with R* should be sufficiently small to ignore. If this is true, then the V/F conversion may be stated by rearranging (2):

$$\frac{H_z}{V_{in}} = \frac{\frac{1}{T}}{V_{in}} = \frac{1}{4R_1C_1} \qquad (6)$$

The circuit shown has a conversion factor of 50 Hz/volt.

ACCURACY

There are three reasons for the circuit's excellent accuracy:

1. An extremely linear ramp is generated because of the μA749's large input impedance (typically 150 kΩ) and high open loop gain (20,000).

2. Both switching voltages for the comparator are stably defined. The beginning of the T_1 interval (at zero volts) is accurate-

ly held by the low offset and drift of the comparator section (V_{os} = 1 mV, I_{os} = 50 nA), while the -4 volt limit for the end of the timing ramp is repeatedly set by the R_5, R_6 voltage divider. (Note, however, that the second limit voltage does require a low drift negative power supply).

3. Integrating capacitor reset is very rapid due to the high slewing capability of the μA749 amplifier.

Of these factors, the rapid reset capability is probably most significant. For example, consider the Figure 1 component values. When V_{in} = 5 volts, this circuit operates at 250 Hz.

$$T = \frac{1}{f} = \frac{1}{250} = 4000\mu S = T_1 + T_2$$

$$\text{reset \% error} = \frac{T_2}{T_1 + T_2} \times 100$$

$$= \frac{45\ \mu S}{4000\mu S} \times 100 = 1.12$$

Experiment indicates that reset times down to 20 μS (using a smaller integrating capacitor) are possible, implying a limitation of about 1 kHz for ±1% accuracy. Fortunately, the error can be largely corrected by trimming the -4 volt threshold for absolute midscale accuracy. This will improve accuracy by at least 0.5% over most of the range.

Power supply rejection is an additional source of error. The basic circuit is good in this respect if V_{in} is near + 4 volts and derived from the same (+) and (-) balanced power supply as the comparator -4 volt reference voltage. However, changes in the (-) supply which are independent of the input voltage will appear to the circuit as a change in the comparator threshold, causing potentially large errors in the output frequency. This problem can be easily circumvented by using slaved (+) and (-) power supplies in which one supply polarity's reference voltage is held to track closely with the second by a unity gain inverting amplifier. (Refer to the μA747 data sheet for an example of this technique). The V/F converter should also exhibit reasonable temperature stability, although the circuit has not been tested for this characteristic. The desired temperature spread and accuracy should be kept in mind when specifying C_1, R_1, R_2, R_5, and R_6.

ACKNOWLEDGMENT:

This is an updated version of a circuit idea which first appeared in Application Bulletin APP-124, by R. J. Widler and J. N. Giles. Breadboard checkout of the present modification was conducted by R. E. Tuttle.

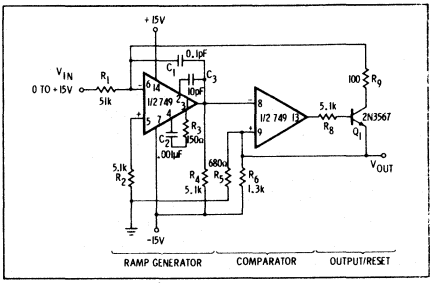


Figure 1. μA749 Voltage To Frequency Converter

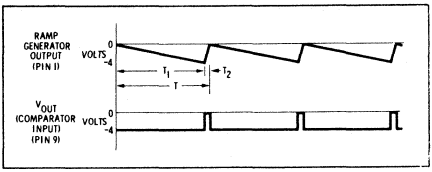


Figure 2. Waveshapes

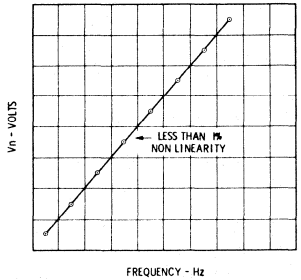


Figure 3. μA749 Voltage To Frequency Converter

COLOUR TELEVISION CHROMA REFERENCE SYSTEMS USING THE μA703

INTRODUCTION

Accurate reproduction of a televised color image requires the regeneration at the receiver of a 3.58-MHz subcarrier frequency in exact phase with the color burst reference signal transmitted by the station during a portion of the horizontal blanking time.

Three methods are used to re-establish the 3.58-MHz subcarrier in present color receivers: (1) the voltage controlled crystal oscillator in an APC loop; (2) the injection locked crystal oscillator; and (3) the narrow bandpass crystal-ringing circuit. The most familiar is the crystal oscillator in an APC loop. This system has a wide pull-in range, excellent phase stability, and high noise rejection, but requires an external phase detector and frequency controlling element such as a reactance transistor or varicap. The simpler injection-locked oscillator system does not require an APC loop. In this system, the burst is transformer-coupled directly into the oscillator to lock it. The injection locked system, however, compromises phase stability and noise immunity.

For good noise immunity, the circuit Q must be extremely high, which requires that the crystal oscillator have lower drift than is required in the APC system for acceptable phase stability. Because the system has an output level which is disturbed during burst injection, the circuitry that it drives must be able to accommodate amplitude variations of the reference signal. The ringing system relies on a high Q crystal filter which is energized during the burst period. It continues to ring during the remainder of the horizontal period until reinforced by the next burst. Of the three systems, it is the only one which does not require a killer, since there is no demodulation drive in the absence of a burst. However, because it has no output in the absence of a burst, it is not suitable for driving certain types of demodulators.

* As originally published in EDN, March 1967.

Designs of voltage-controlled and injection-locked crystal oscillators using the μA703 integrated circuit are described in the paper.

INTEGRATED CIRCUIT μA703

The μA703 integrated circuit has been specifically designed for self-limiting applications. In an oscillator circuit, the output voltage level is determined by the load and is independent of the feedback signal, provided that this signal is sufficiently large. Biasing is incorporated within the device, so that a minimum of external components are required in either amplifier or oscillator applications. The device is described in greater detail in the literature. [1]

VOLTAGE-CONTROLLED CRYSTAL OSCILLATOR FOR APC SYSTEM

Fig. 1 shows the μA703 integrated circuit and associated circuitry for a voltage-controlled crystal oscillator. The positive feedback voltage to start and sustain oscillations is taken from a capacitive tap in the tuned circuit at the collector of transistor Q_B. This voltage is fed back through a narrow bandpass filter to the base of transistor Q_A. The common-collector transistor, Q_A, drives the common-base transistor, Q_B, to complete the regenerative feedback path required for oscillation.

1. Barrett, Blaser, and Suzuki; "An FM Tuner Using MOS-FET'S and Integrated Circuits", IEEE Transactions on Broadcast and Television Receivers, pp 24-32; July 1965. Also avaliable as Fairchild Semiconductor Technical Paper, TP-21.

FAIRCHILD
SEMICONDUCTOR

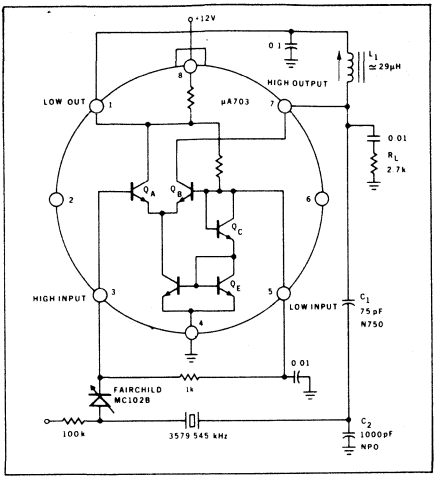


Fig. 1. Integrated circuit, voltage-controlled crystal oscillator.

The inductor, L_1, in combination with the series capacitors, C_1 and C_2, make up the reactive components of the temperature-compensated, 3.58-MHz output tank circuit. The output signal amplitude (V peak - 5 volts) is determined by load resistance, R_L. The loaded Q of the output tank is approximately 5. The inductor, L_1, provides a ±400 cps oscillator frequency adjustment range with less than a 1-db change in output level. The range of +400 cps is more than sufficient to accommodate the tolerances of all frequency-determining components, the more predominant ones being ±0.005 percent crystal and the ±10 percent varactor diode in the feedback circuit. A relatively large feedback signal (0.5 volt peak-to-peak) is fed into the high input of the integrated amplifier to take advantage of its self-limiting properties. The crystal in the feedback circuit is the primary frequency stabilizing element. It operates in the inductive mode and resonates with the capacitance of the varactor diode. The voltage-dependent capacitance of the diode provides a fine frequency control.

The low input of the µA703 sets positive above ground by the forward voltage drops of the two diode-connected transistors, Q_C and Q_E. The 1-kilohm resistor from the "high" to "low" inputs of the µA703 provides base current for transistor Q_A, and is the predominant load on the series resonant feedback circuit.

The "high" input which also sets 1.5 volts above ground provides an excellent voltage reference point for the varactor diode because of the small change in voltage at this point with variations in temperature and V_{CC}. The variactor diode has a nominal capacity of 30 picofarads at 1.5 volts reverse bias and $\frac{C_{2V}}{C_{40V}} \leq 3.1$. With a 1.5-volt reverse bias on the diode, a plus or minus 1-volt control voltage, which changes the capacitance appreciably, can be applied without forward biasing the diode. Because the diode always operates reversed-biased, it can be driven from a high-impedance phase detector.

INJECTION-LOCKED CRYSTAL OSCILLATOR

Fig. 2 shows the µA703 integrated circuit and associated circuitry for a injection-locked crystal oscillator, which is basically similar to the voltage-controlled oscillator. The output tuned circuit is the same, except that the ratio of C_1 and C_2 is smaller to allow for the additional voltage drop of the burst transformer impedance in the feedback loop. L_1 provides the initial frequency setup without affecting the output voltage significantly. The crystal in the feedback loop is the primary frequency-determining element. It operates in an inductive mode and resonates with capacitor C_3. The burst transformer induces the chroma reference synchronizing voltage into the feedback loop of the oscillator. It is parallel resonant and is tuned for maximum burst amplitude. The total reactance of the feedback loop will be changed during the injection period depending on the frequency difference between the oscillator and the induced voltage. The oscillator will tend to look to the induced synchronizing voltage if the ratio of induced voltage to the feedback voltage is large and the frequency difference between the oscillator and induced voltage is small. These two factors will further in-

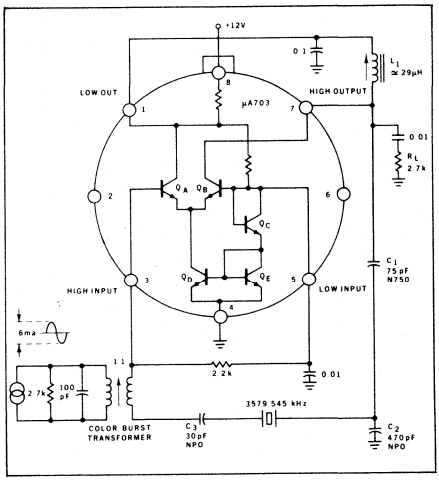


Fig. 2. The µA703 injection-locked crystal oscillator.

fluence the phase relation between the oscillator and the reference burst in the locked position.

It has been determined by controlled viewing tests of color scenes that the maximum tolerable phase error in the chrominance signal (or in the regenerate color reference signal) is approximately ±15 degrees.[2] For the burst injection system shown in Fig. 2, it was determined experimentally that a burst voltage injected across the crystal and C_3, which is six times the amplitude of the feedback signal at C_2, would hold the phase error of the locked oscillator to within ±15 degrees for a 100-cps change in oscillator free-running frequency. Since measured oscillator drift due to all causes is considerably less than 100 cps (Figs. 7 and 8), the expected tint shift in normal set operation would be quite acceptable.

The 6-mA peak-to-peak drive current required at the primary of the burst transformer can easily be developed by using another μA703 as a burst amplifier.

VOLTAGE-CONTROLLED CRYSTAL OSCILLATOR PERFORMANCE

The voltage-controlled oscillator frequency and output amplitude versus V_{CC} is shown in Fig. 3. The frequency drift of the oscillator for changes in ambient temperature is

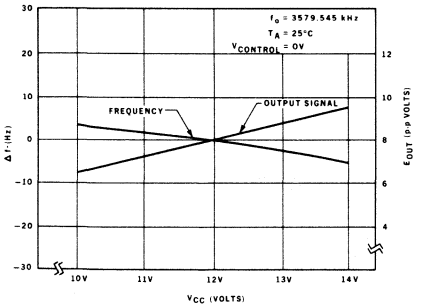


Fig. 3. Frequency and E_{out} versus V_{cc}, voltage-controlled oscillator.

dependent upon the type of crystal used and the overall layout of the circuit. Fig. 4 shows frequency drift versus temperature, with the oscillator being temperature-compensated for only one particular type of crystal in a breadboard layout.

2. Donald G. Fink, "Television Engineering Handbook"; McGraw-Hill Book Company, pp 9-30 to 9-32; 1957.

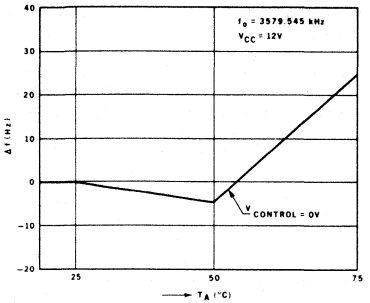


Fig. 4. Frequency versus temperature, voltage-controlled oscillator.

Oscillator sensitivity versus control voltage is shown in Fig. 5. The small control voltage needed to compensate for the oscillator drift due to all causes is easily achieved in a phase detector circuit. Table I shows oscillator frequency for several μA703's with no circuit readjustments.

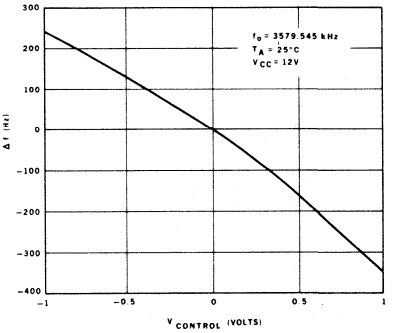


Fig. 5. Oscillator sensitivity for APC, voltage-controlled oscillator.

TABLE I.

Voltage-Controlled Oscillator--Frequency Variations with Several μA703's.

μA703 NO.	FREQUENCY OSCILLATOR(kHz)
1	3579.545
2	3579.520
3	3579.543
4	3579.500
5	3579.540

Conditions: V_{CC} = 12 V
T_A = 25°C
$V_{control}$ = 0V

NOTE: No circuit readjustments.

INJECTION-LOCKED CRYSTAL OSCILLATOR PERFORMANCE

In the absence of a synchronizing burst, the injection-locked oscillator frequency and output amplitude versus V_{CC} is shown in Fig. 6. Oscillator frequency versus ambient

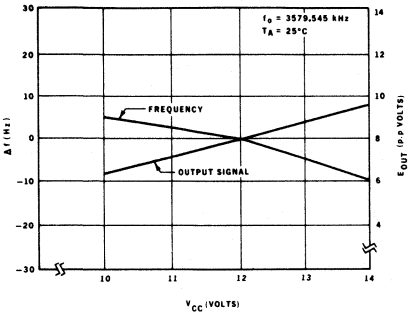


Fig. 6. Frequency and E_{out} versus V_{cc}, injection-locked oscillator.

temperature is shown in Fig. 7. With a burst voltage injected across the crystal, and C_3 six times the amplitude of the feedback signal at capacitor C_2, the measured phase

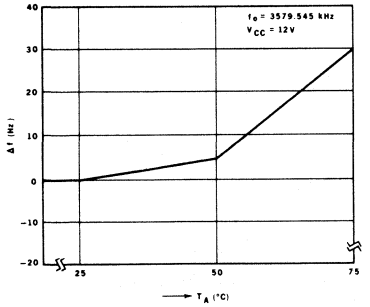


Fig. 7. Frequency versus temperature, injection-locked oscillator.

shift between burst and oscillator signal versus free-running oscillator frequency is shown in Fig. 8. Pull-in capability of the circuit with a 6:1 injection ratio is ±400 cps which is

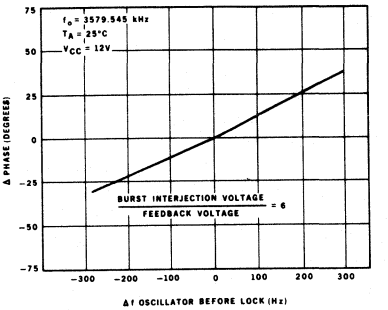


Fig. 8. Phase shift versus oscillator free-running frequency, injection-locked oscillator.

much greater than measured oscillator drift due to all causes. Table II shows the free-running oscillator frequency for different μA703's with no current readjustments.

TABLE II.

Injection-Locked Oscillator--Frequency Variations with Several μA703's.

μA703 NO.	FREQUENCY OSCILLATOR(kHz)
6	3579.545
7	3579.455
8	3579.548
9	3579.508
10	3579.516
Conditions:	V_{CC} = 12 V, T_A = 25 C

NOTE: No circuit readjustments.

CONCLUSION

Two crystal oscillators, one voltage-controlled and the other injection-locked, have been designed, taking advantage of the self-limiting properties of the μA703 integrated circuit. Both oscillators are capable of excellent temperature stability and both have almost complete immunity to supply voltage variations. These two oscillators meet the requirements imposed by the chroma reference system for which they have been designed.

VOLTAGE REGULATOR APPLICATIONS USING μA723 – NUMBER 2

The circuits presented here are designed to fill applications in which range or accuracy extensions are required beyond the basic voltage regulator's capability.

Figures 1 and 2 allow input voltages in excess of the forty volt maximum specified for the basic device. In both cases the output voltage must be less than forty volts to protect the μA723. R1 in Figure 1 may be replaced with an FET current source in instances where the min-max limits on the input voltage requires the internal series pass device to handle excessive power dissipations.

Some applications call for regulation figures equal to the temperature coefficient of the regulating device. The circuit in figure 3 accomplishes 0.005% voltage regulation by adding one resistor (R_1) to the basic floating regulator schematic while figure 4 accomplishes 0.05% current regulation by the same addition. In both cases the output range and power capability is determined by the selection of the output devices

The μA723 uses a single transistor's base-emitter junction as the current limit sensor. Figure 5 is one method of removing the 2 mV/°C temperature coefficient which changes the current limit point over any ambient temperature excursion.

Figure 6 is the circuit answer to the "if all else fails" situation. It provides overvoltage protection for the load by performing a temperature compensated overvoltage detection, latch and SCR firing function. This function responds in approximately one microsecond or may be slowed by capacitor C_1.

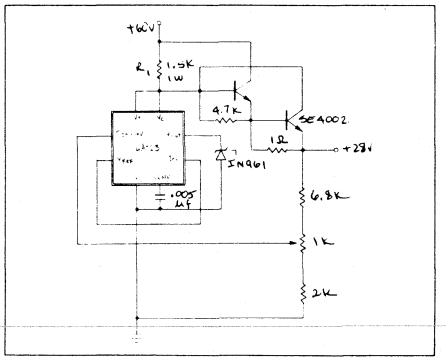


Fig. 1 High input voltage regulator.

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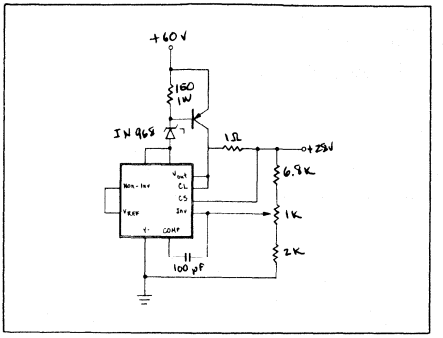


Fig. 2 High input voltage regulator.

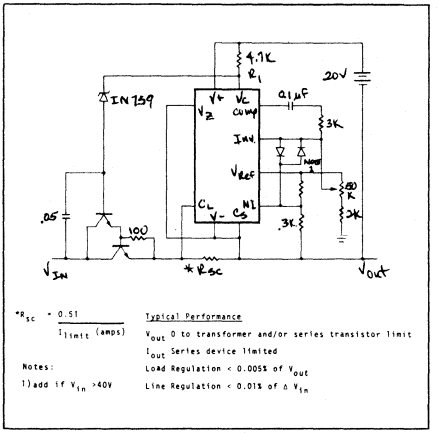


Fig. 3 Precision floating voltage regulator.

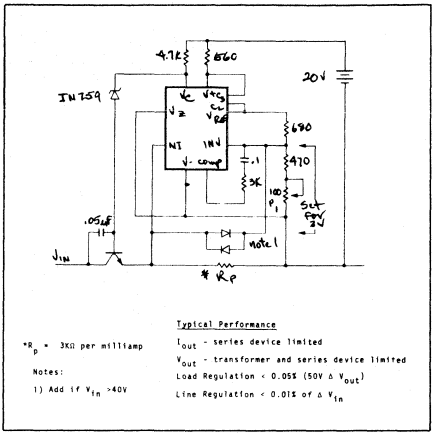


Fig. 4 Precision floating current source.

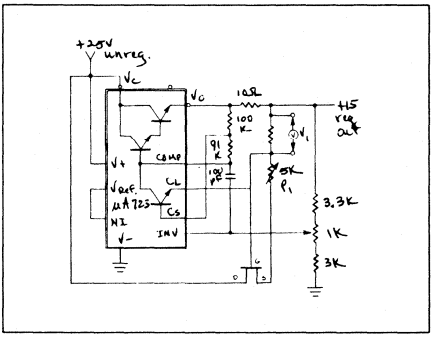


Fig. 5 Temperature stabilized short circuit.

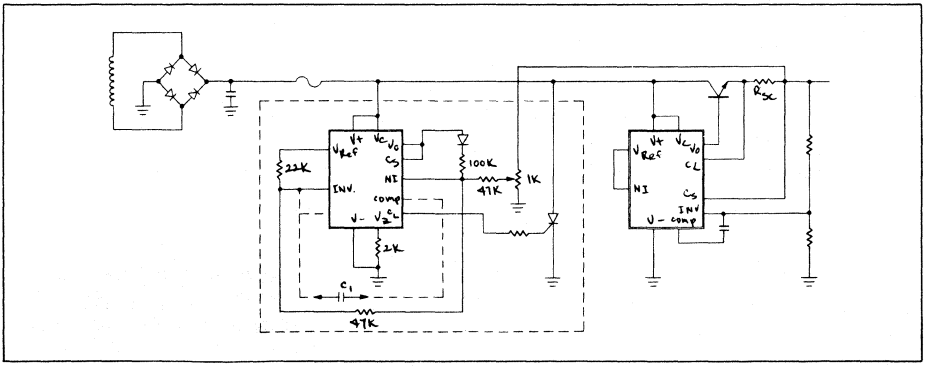


Fig. 6 Overvoltage crowbar.

CHARACTERIZATION AND APPLICATION OF THE μA703 IN A FOUR-STAGE FM-IF AMPLIFIER

INTRODUCTION

The μA703 is a linear integrated circuit designed to give very high available unneutralized power gain at 10.7 MHz and to have the capability of current mode limiting with a suitable choice of output load conductance. The advantages of current mode limiting are:

a. The loads presented to the transformers by either the input or the output of the μA703 do not change appreciably under any normal input signal (i.e., up to approximately 3 volts rms).

b. Since there is no breakup or phase distortion of the signal, no AGC is required for an FM IF amplifier.

c. The passband characteristics of the transformer are unaltered during any stage of limiting.

The performance of an IF amplifier employing current mode limiting is therefore characterized by a very low capture ratio, excellent AM rejection, and the ability to accommodate rapidly fluctuating signal strengths (as with a car radio).

In this report, the μA703 will be discussed with special reference to current mode limiting amplifiers for use at 10.7 MHz. Then a design for a four-stage high-quality FM IF amplifier will be described in detail.

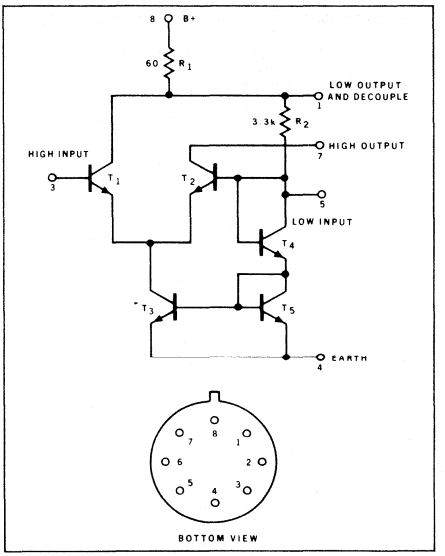


Fig. 1. Linear integrated circuit μA703.

μA703

The μA703 is shown schematically in Fig. 1. T_1 and T_2 act as an emitter-coupled pair of transistors and constitute the active RF amplifier. T_3, T_4, and T_5, together with R_1 and R_2, are used to provide the biasing for T_1 and T_2. In the following description of the biasing of T_1 and T_2, T_1 and T_2 together with T_3 and T_5, will be considered as perfectly matched pairs of transistors. This matching is achieved because all the transistors are manufactured on a monolithic chip, which results in identical diffusion schedules for all the transistors. Also, because of the close proximity of the transistors contained on a chip, the tolerances in manufacturing can be minimized.

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The current through the biasing chain (R_2, T_4, and T_5) is approximately equal to the B+ supply minus the two emitter voltage drops of T_4 and T_5 (i. e., 1.5 volts) divided by 3.3 Kilohms. For a 12-volt supply, this current will be a little over 3 milliamps. Since T_3 and T_5 are identical transistors, the V_{BE} - I_C characteristics will be identical. Therefore, neglecting the base currents in T_3 and T_5, the collector current of T_3 is approximately equal to the current in the biasing chain. Due to its very high output impedance, the T_3 acts as a current source to the identical pair of transistors T_1 and T_2. In a practical amplifier, the bases of T_1 and T_2 will be tied together through a transformer or choke so that the current defined by T_3 will be equally divided between T_1 and T_2.

The total current consumed by μA703 is approximately equal to twice the current through the biasing chain or four times the current through either T_1 and T_2. The function of T_4 is to provide a sufficiently high bias voltage for T_1 and T_2, so that there is no possibility of T_3 being driven into saturation. If T_3 were driven into saturation, it would no longer act as a current source to T_1 and T_2.

Considering the μA703 as an amplifier, the output impedance of T_3 appears almost infinite in value at medium to low frequencies, and the base of T_2 almost a short circuit to ground (the series resistance of T_4 and T_5 is only a few ohms).

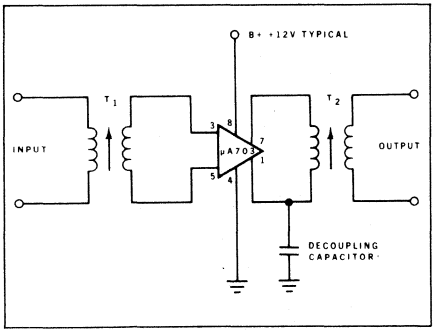


Fig. 2. Practical amplifier.

Fig. 2 shows the use of μA703 as a high-frequency amplifier. The only external components are the tuned transformers plus one decoupling capacitor. The supply voltage will normally be chosen between about 6 to 12 volts. The current through transistors T_1 and T_2 will be within these limits of supply voltage, approximately proportional to the supply voltage. If desired, the current in T_1 and T_2 may be increased by adding an external resistance in parallel to R_2 or may be decreased by adding an external resistance across T_4 and T_5. (See Fig. 3.)

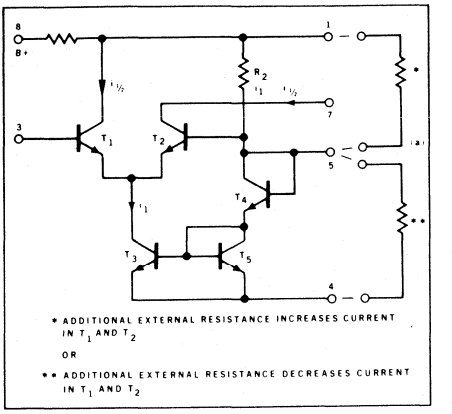


Fig. 3. Alternate No. 1 amplifier configuration.

Another possible circuit configuration is shown in Fig. 4. In this circuit the available power into a load is doubled, but the high frequency stability limited gain is decreased. Another disadvantage of this circuit is the non-usability of R_1.

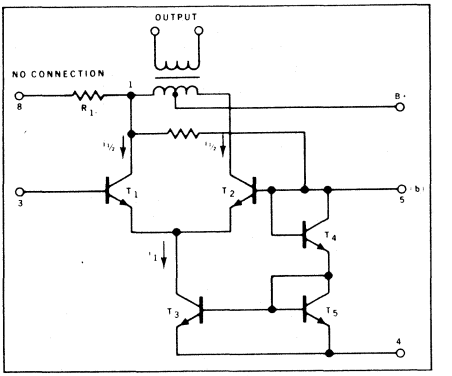


Fig. 4. Alternate No. 2 amplifier configuration.

THE μA703 AS A CURRENT MODE LIMITER

A current mode limiter is one that defines the maximum peak-to-peak output current independently of the load conductance. A single transistor, FET, or tube cannot satisfy the above condition since, as the input signal is increased, the maximum downward output current swing will be the product of:

(V supply - V saturation) x (load conductance), limited primarily by the load conductance.

The μA703, however, supplies a constant current, i_1, from T_3 and T_2. Therefore, the limiting current values of T_2, assuming a low-output load conductance, are either 0 or i_1, no matter how large the input signal is (as long as it does not break down the emitter diode of T_1 in the reverse direction). The load conductance value is chosen for nonsaturating or current-mode operation, so that the downward voltage swing across this load conductance never goes below the fixed base bias voltage on T_2.

DETERMINATION OF OUTPUT LOAD CONDUCTANCE FOR CURRENT MODE LIMITING CIRCUITS

If the input signal (sine wave) is very large in the circuit shown in Fig. 5, the output current will be a square wave of peak-to-peak amplitude of $-i_{1/2}$ to $+i_{1/2}$ to a transformer coupled load. By Fourier analysis, this current can be represented by an infinite series, as follows:

$$I = \frac{i}{2} \cdot \frac{4}{\pi} \left\{ \cos \omega t + \frac{\cos 3\omega t}{3} + \cdots\cdots \right\}$$

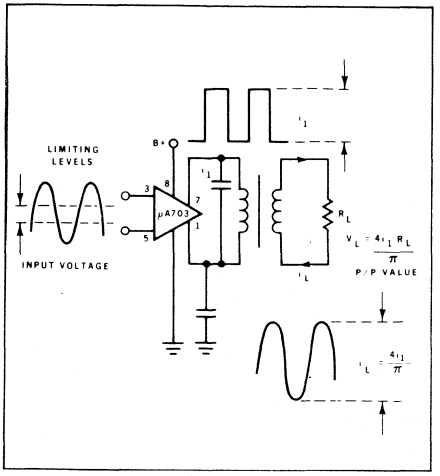


Fig. 5. Voltage and current waveforms for the μA703 in a non-saturating circuit.

The peak value of the fundamental frequency of the square wave has a peak value of $\frac{4}{\pi}$ times the peak value of the square wave.

In most RF applications the required amplifier bandwidth is narrow, and all terms other than the fundamental can be ignored. (FM IF transformers can be assumed to have negligible response at three times the IF frequency, or 32.1 MHz and higher frequencies). The voltage occurring across the load conductance is therefore sinusoidal, although the output current from the μA703 is a square wave.

The maximum load conductance can now be defined by:

$$\frac{\text{(peak downward current swing)}}{\text{(Supply voltage) - (Voltage across } T_4 \text{ and } T_5\text{)}}$$

$$= \frac{i_{1/2}}{\text{Supply Voltage - 1.5}} \times \frac{4}{\pi}.$$

In a practical design, the load conductance should be increased by 50 percent because of the normal tolerances of the load conductance and the variation of i_1 from one μA703 to another.

$$\therefore \text{ Load Conductance} = \frac{3 i_1}{\pi(\text{supply voltage - 1.5})}$$

$\therefore$ If i_1 = 3ma and V supply = 12 volts, the load conductance becomes

$$Q_L = \frac{3 \times 3}{\pi \times 10.5} = 0.273 \text{ mmho}.$$

NOTE:

1. The load conductance is independent of frequency.
2. If the current i_1 is varied by the addition of an external resistance between pins 1 and 5, as previously mentioned, the load conductance must be recalculated.

INPUT MATCHING CONSIDERATIONS

For optimum design in a current-mode limiting amplifier, the μA703 should be mismatched at the input.

a. The input conductance of the μA703 will be primarily determined by h_{FE} of T_1 at low RF frequencies. The

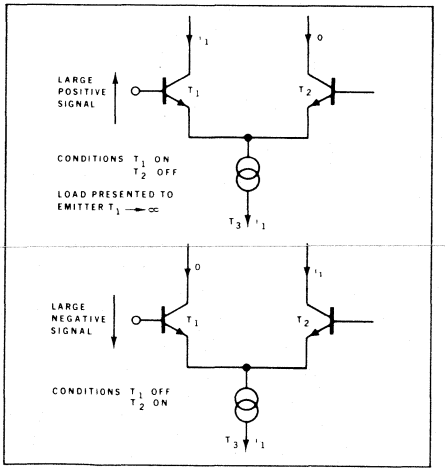


Fig. 6. Large signal operation.

h_{FE} for any transistor family will vary over a substantial range. For the μA703, this range is from 50 to 200.

b. The input conductance will decrease when the μA703 is driven into limiting. This can easily be seen by considering Fig. 6. If a large positive voltage is applied to T_1, then T_2 will be switched off and the total admittance presented to the emitter of T_1 will be very small, thereby decreasing the input conductance. If a large negative voltage is applied to T_1, T_1 will be switched off and the input conductance reduced.

DESIGN OF AN FM IF AMPLIFIER

The requirements for an FM IF amplifier design are as follows:

1. Power gain greater than 85 dB
2. Bandwidth of amplifier to be -6 dB at ± 120 kHz, center frequency; 10.7 MHz together with a linear phase characteristic across the passband.
3. Total harmonic distortion at 400 Hz to be less than 1 percent with ± 75 kHz deviation.
4. Capture ratio to be as low as possible, preferably less than 2 dB.

Typical "y" parameters of the μA703 at 10.7 MHz with a 12-volt supply are:

$$y_{11} = 0.5 + j\,0.8 \text{ mmho}$$

$$y_{22} = 0 + j\,0.23 \text{ mmho}$$

$$y_{21} = -25 + j\,0 \text{ mmho.}$$

Due to the very small value of y_{12}, its value can best be determined by the ratio of the forward power gain to the reverse power gain in a carefully shielded jig.

Ratio of forward-to-reverse power gain

$$\left|\frac{y_{21}}{y_{12}}\right|^2 = 93 \text{ dB}$$

or the maximum stable unneutralized power gain

$$\left|\frac{y_{21}}{y_{12}}\right| = 46.5 \text{ dB.}$$

In order to realize the phase and bandpass characteristics of the IF amplifier, three undercoupled transformers (kQ_{pri} = 0.8, where k = coupling factor, and Q_{pri} = primary Q factor) each of which having a -3 dB bandwidth of 310 kHz are a satisfactory compromise.

$$\text{If } y = \frac{\text{Bandwidth}}{\text{Center frequency}} = \frac{2\Delta f}{f_o} = \frac{0.31}{10.7} = 0.029.$$

Then yQ_{pri} can be obtained from the standard admittance curves, providing kQ_{pri} = 0.8 and yQ_{pri} = 1.2.

$$\therefore Q_{pri} = 41.5$$

(assuming equal primary and secondary "Q" factors).

To minimize the effect of the variability of the input conductance of the μA703 on the Q_{sec} of a transformer, the input conductance in the nominal case will be designed so that it will load the unloaded "Q" by 25 percent. The output conductance of the μA703 being extremely low will not affect the Q_{pri} of the transformer.

Assuming the primary and secondary unloaded "Q"s to be equal, the loaded "Q" ratio is

$$\frac{Q_{pri}}{Q_{sec}} = 1.33$$

$$\text{but} \quad \sqrt{Q_{pri}\,Q_{sec}} = 41.5$$

$$\therefore \quad Q_{pri} = 48 \text{ (loaded)}$$

$$\text{and} \quad Q_{sec} = 36 \text{ (loaded)}$$

The input conductance of the transformer with the secondary loaded is given by

$$G_{in} = G_{pri}\left(1 + \frac{K^2 t}{\left\{1 + (y\,Q_{pri})^2 t^2\right\}}\right)$$

where $$t = \frac{Q_{sec}\text{ loaded}}{Q_{pri}\text{ loaded}}$$

and G_{pri} = the parallel conductance of the primary of the transformer.

$$K = kQ_{pri}$$

$$\therefore \quad G_{in} = G_{pri}\left(\frac{1 + 0.8 \times 0.75}{\left\{1 + 1.2^2 \times 0.75\right\}}\right)$$

$$= 1.33\,G_{pri}$$

The load conductance to be presented by the primary of the transformer to the output of the μA703 has been previously determined to be 0.273 mmho for a nonsaturating amplifier.

$$\therefore \quad 1.33\,G_{pri} = 0.273 \text{ mmho}$$

$$\therefore \quad G_{pri} = 0.205 \text{ mmho.}$$

The tuning capacitance necessary to give a Q_{pri} of 48 with a primary conductance of 0.216 mmho:

$$= \frac{Q_{pri}\,G_p \times 10^{-3} \times 10^{12}}{\omega} \text{ pF}$$

$$= \frac{48 \times 0.205 \times 10^9}{2\pi 1.07 \times 10^7} \text{ pF}$$

$$= 146 \text{ pF.}$$

If both the primary and secondary windings of the transformer have the same number of turns and tuning capacitances, the secondary tap to the μA703 is given by:

$$n^2 = G_{pri}\left(\frac{Q_{sec}\text{ unloaded} - Q_{sec}\text{ loaded}}{Q_{sec}\text{ unloaded}}\right)\frac{0.1}{g_{11}}$$

$$= 0.205\left(\frac{48 - 36}{48}\right)\cdot\frac{1}{0.5} = 0.103$$

$$n = 0.322.$$

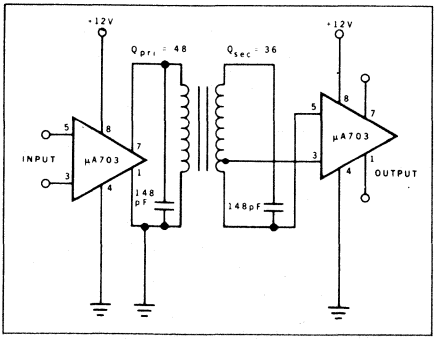


Fig. 7. The complete FM interstage transformer showing interfacing between two μA703's.

Due to cost considerations, a value of tuning capacitance lower than 148 pF is preferred by coil manufacturers. An alternative transformer with 82-pF tuning capacitance is given in Fig. 8,

where $n_p^2 = \frac{82}{148}$

$\therefore n_p = 0.745$

$n_s = n_p \times 0.33$

$= 0.246.$

POWER GAIN CALCULATION

Assuming that the power gain of a stage will be much less than the maximum stable unneutralized power gain, $\left|\frac{y_{21}}{y_{12}}\right|$ = 46.5 dB, then the effect of y_{12} can be ignored.

The total reflected conductance at the primary of the transformer of the loaded secondary of the transformer is equal to 0.33 x 0.273 mmho. One-fourth of this conductance

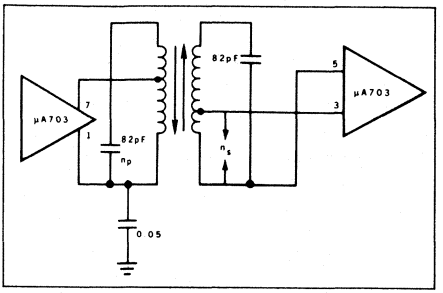


Fig. 8. Alternate interstage transformer.

is due to the loading of the input of the μA703. Therefore, the reflected admittance of the input of the μA703 at the output of the previous μA703 is:

$\frac{0.33 \times 0.273}{4}$ = 0.0274 mmho

$\therefore$ Power gain =

$$\frac{|y_f|^2 \text{ (reflected input conductance of following } \mu A703)}{g_{11} \text{ (total load conductance)}^2}$$

$$= \frac{25^2 \times 0.0274}{0.5 \times 0.273^2}$$

$$= 460$$

$$= 26.6 \text{ dB}.$$

To satisfy the power gain requirement of the amplifier, four stages are required; resultant power gain is therefore 106 db.

Fig. 8 shows the schematic of the four-stage FM IF amplifier. The detector is a modified ratio detector which, due to the excellent limiting properties of the amplifier, does not require the usual large electrolytic capacitor.

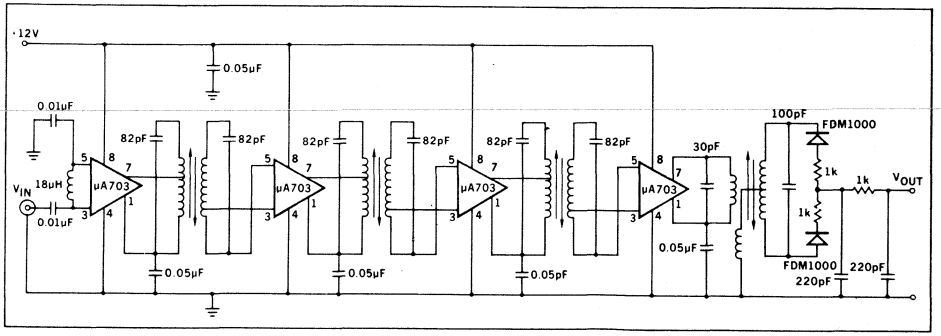


Fig. 9. Four-stage FM IF amplifier employing non-saturating limiters.

PERFORMANCE OF THE AMPLIFIER

The four-stage FM IF amplifier has the following performance parameters.

Sensitivity < 50μV for full limiting

Capture ratio < 1.5 dB

Bandwidth of detector ~800 kHz

AM rejection >40 dB.

SUMMARY

The μA703 has been described and an analysis of its operation as a current mode limiter given. Its application in an FM IF amplifier, together with a practical four-stage amplifier, has also been shown. Further applications include very high-gain, unneutralized, small-signal amplifiers up to 200 MHz.

The μA703 should prove to be a useful and economical device for the consumer market, based on its very high frequency power gain, the availability of current mode limiting, the possibility of changing its bias current by the simple addition of an external resistor, and its lack of complicated biasing and decoupling networks.

REFERENCES

1. John Barret, Larry Blaser, and Harry Suzuki, "An FM Tuner Using MOS-FET's and Integrated Circuits", Fairchild Technical Paper TP-31.
2. R. J. Widlar, "Some Circuit Design Techniques for Linear Integrated Circuits", Fairchild Technical Paper TP-33.

APPLICATIONS OF THE μA757 GAIN CONTROLLED AMPLIFIER

Introduction

The μA757 is a high performance gain controlled amplifier useful at frequencies from audio thru IF and video up to 25 MHz. The circuit has two stages which may be cascaded or operated independently; and the gain of each stage may also be varied independently.

Figure 1 shows the schematic diagram of the μA757. The input consists of a differential pair loaded with diode-connected transistors that provide a means of gain control which is accomplished by increasing the current in these diodes, thereby reducing their impedance. At large signal levels, the diodes will cause distortion of signals, however, this distortion is cancelled by the input characteristics of the second stage differential pair so that good overall linearity is obtained.

Both the first and second sections of the circuit employ the basic type of gain control blocks, however, the second section has an additional output amplifier for additional gain and greater output capability.

The first section of the microcircuit has approximately 25 dB of voltage gain into a 1 kΩ load while the second section of the circuit has approximately 50 dB of voltage gain into a similar load.

The design of the circuit is such that gain variations with temperature and supply voltage variations are minimized. The μA757 has excellent signal handling characteristics with AGC so unlike certain previous circuits, the full gain control range of 70 dB is usable. The circuit is designed to fulfill the needs of communications circuit design engineers in the audio, video, telemetry and radio fields for a high performance, gain controlled amplifier.

Figure 2 shows how the μA757 may be used as a high gain, wide AGC range IF amplifier. In this circuit the input signal is matched from the generator to the input of the microcircuit with transformer T_1. The output of the first section is taken from Pin 12 across a tank circuit which acts as a load impedance. The signal is coupled thru a capacitor to the input of the second section, Pin 10. The

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output of the second section is taken in a push-pull manner with transformer T_3. The secondary drives the diode detector from which audio is recovered. Q_1 acts as an AGC signal amplifier to provide gain for the AGC signal from the diode detector.

Voltage gain of the circuit from the input of T_1 to the input of T_3 is typically 80 dB, while the AGC range is 70 dB. Input signal handling capability of the microcircuit is typically 300 mV RMS at the input terminals of the microcircuit at full AGC. Constant, stable gain is obtained over a wide temperature range regardless of AGC setting.

Audio-Video Compressor Amplifier

The µA757 is well suited to audio/video compressor amplifier applications. Wide ranges of input signal levels can be accommodated without overload or distortion. Figure 3 shows how the microcircuit is connected in a typical compressor application. The input signal is fed into the first stage amplifier of the device; this stage is loaded with a 1 K load resistor. The signal is then coupled to the input of the second stage with a 1 µF coupling capacitor. The signal output is taken from the positive output of the second stage across a 1 K load resistor. The negative output of the circuit is also loaded with a 1 K resistor, and the output derived here is used to drive the AGC detector (D1 and Q1). In this manner, the loading of the AGC detector does not affect the signal output and distortion is minimized.

As shown, the circuit has a voltage gain of better than 70 dB and an AGC range of approximately 70 dB. AGC begins at an input signal level of 150 µV and is effective up to input levels of 300 mV. Over this range, the output is held between 0.7 and 1.2 volts. The bandwidth of the circuit is approximatley 50 Hz to 50 kHz.

Circuit performance may be tailored by minor modifications. For example, a bandwidth of greater than 5 MHz may be obtained by omitting roll off capacitors C6 and C8. The attack and release times may be varied by changing the size of C10 and R4. If tighter regulation of the output level is required, additional voltage gain may be added between the output of Q1 and the AGC input to the microcircuit (pins 3 and 4).

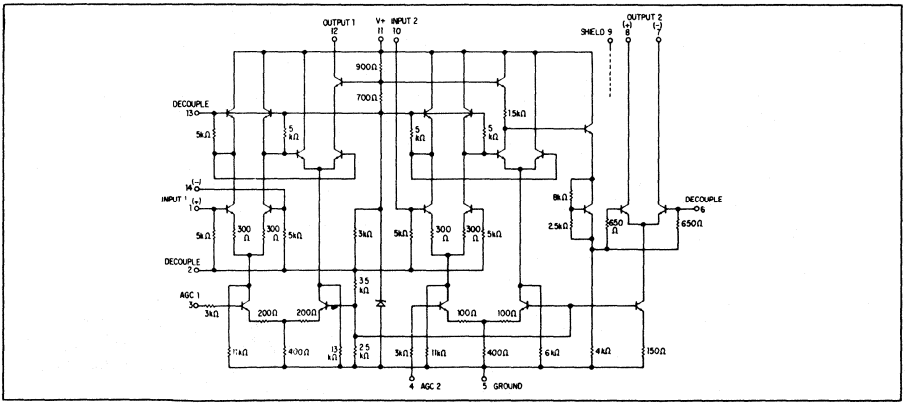


Fig. 1

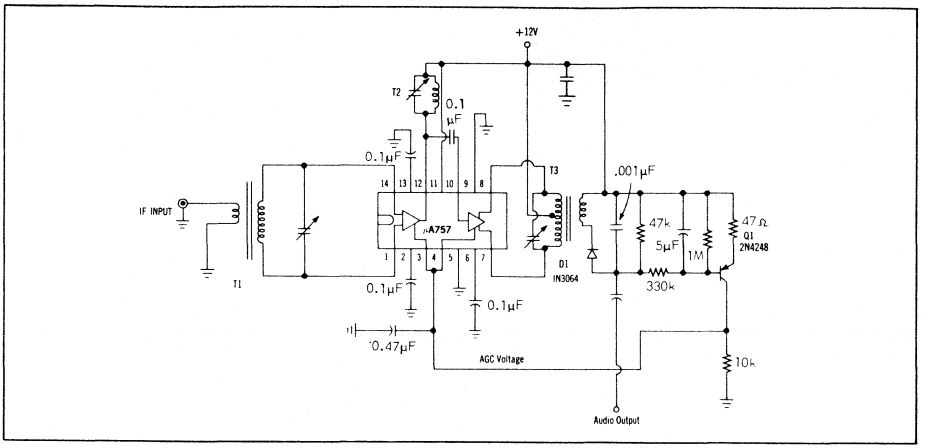


Fig. 2. AM/IF Amplifier.

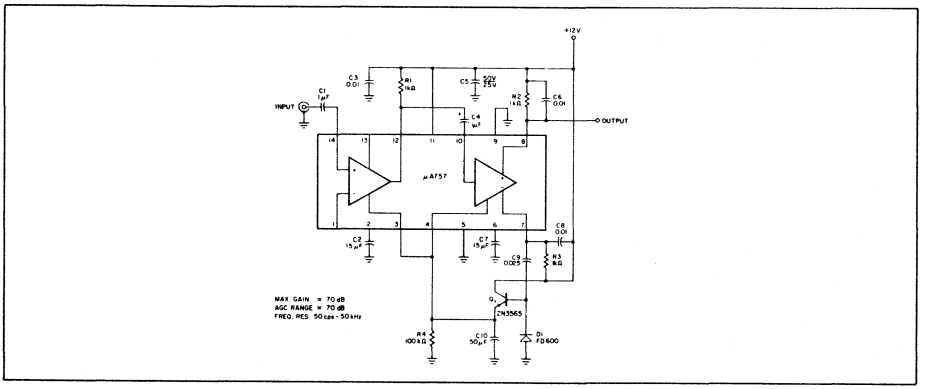


Fig. 3. Audio/Video Compressor Amplifier.

THE μA729, μA732 AND μA767 INTEGRATED CIRCUIT STEREO MULTIPLEX DECODERS

INTRODUCTION

High quality broadcast receivers have seen the introduction of linear integrated circuits during the past few years. These ICs often embodied novel design approaches to obtain the best performance/cost features simultaneously. This article describes recent complements to this family of integrated circuits, the μA729 and μA732 IC stereo multiplex decoders, which incorporate the components required for stereo demodulation plus the auxiliary functions normally associated with the stereo demodulator in stereo FM receivers.

The μA729 and μA732 are slightly different versions of the same basic multiplex decoder in that the μA729 has provision for an external separation adjustment. Both IC multiplex decoders are otherwise identical and each contains the functions of stereo demodulator, 19KHz amplifier and doubler, stereo-monaural switch, stereo indicator lamp driver and audio mute switch. The μA767, a less complex design offering the functions of stereo demodulator, 19kHz amplifier and doubler, and lamp driver, also is available.

Operation of the IC decoders is discussed first in the following pages. Application of the μA729 and μA732 in stereo FM receivers is then described and several possible user options are detailed. The μA767 is not specifically referenced since it is essentially similar to the μA732 except for the stereo-monaural and audio-mute switching functions. Schematic diagrams of the μA767 and its application appear at the end of this paper.

STEREO DEMODULATOR

Stereo demodulation in the μA729 and μA732 is achieved by a fully balanced differential synchronous demodulator (Figure 1). In this demodulator, the composite stereo signal is fed to the base of transistor Q_{16}. The resulting AC current which flows in the collector of Q_{16} is then switched at a 38KHz rate by the differential pair Q_{11} and Q_{12}. The amplitude of the 38KHz switching signal is large enough to instantaneously gate the AC current alternately to the left and right audio channels. If the 38KHz gating signal is properly phased with respect to the composite stereo signal, this process will

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separate the stereo signal into its left and right audio components (for a theoretical treatment of this demodulation process, see Ref. 1).

A second differential stage (Q_{13}, Q_{14} and Q_{17}) is added to the stereo demodulator for two reasons. First, the 38KHz also switches the DC current flowing in the collector of Q_{16} resulting in a large undesired 38KHz voltage in both output channels. By gating the DC current in Q_{17} and adding the resulting signals in phase opposition to those from Q_{16}, these 38HKz components are cancelled. More importantly however, the second differential stage provides improved stereo separation. With a single differential demodulator stage, the theoretical stereo separation is limited to 13 dB due to the crosstalk inherent in the half-wave demodulation process. If a portion of the desired output is inverted and added to the crosstalk signal, however, this crosstalk component can be effectively cancelled resulting in stereo separations that are typically 45dB. The crosstalk correction is provided in the μA732 by the second differential stage and internal resistors R_9, R_{10} and R_{11}. In the μA729 resistor R_{11} is an external potentiometer adjustment.

One very important consequence of the demodulation process described above is the elimination of SCA interfence without the necessity of SCA filters. This is possible because any beat frequencies which occur between the 67KHz SCA and the 38KHz switching signal or its harmonics, fall above the normal audio frequency range.

19KHZ AMPLIFIER/DOUBLER

To demodulate the stereo signal, the 38KHz switching voltage must be reconstructed from the 19KHz pilot subcarrier. In the μA729 and μA732 this is accomplished by frequency doubling the 19KHz pilot. First, the pilot subcarrier is filtered from the composite stereo signal by 19KHz tuned circuits L_1C_1 and L_2C_2 and then amplified by the Darlington pair Q_3Q_4 (see Figure 2). This amplified 19KHz pilot causes the composite PNP pair Q_5Q_6 to conduct during negative swings. The resultant 19KHz pulses are then used to drive the 38KHz amplifier Q_{10}. A 38KHz tuned circuit L_3C_3 at the collector of Q_{10} filters the 38KHz component from these pulses and also provides a DC path to insure balanced bias conditions at the demodulator transistor bases.

The 19KHz voltage pulses appearing at the base of Q_{10} are limited to four V_{BE} peak amplitudes by diodes Q_7 through Q_9. This clipper action prevents the 38KHz amplifier transistor from being driven into saturation and loading the 38KHz tuned circuit. An external RC network at the emitter of Q_{10} allows this transistor to simultaneously function as a peak detector. The resultant DC voltage which appears at the emitter of Q_{10} when a 19KHz subcarrier is present, is used to drive the stereo indicator lamp circuits.

STEREO/MONAURAL SWITCHING

Circuitry is incorporated in the μA729 and μA732 to automatically

switch between the "Stereo" and "Monaural" operating modes. This functional change is controlled by an external DC voltage applied to Pin 4 of the integrated circuits (Figures 3 and 4). The DC control voltage activates an internal Schmitt Trigger which accomplishes the switching while the hysteresis present prevents the stereo circuits from flickering on and off due to small changes in bias and input signal conditions. The Schmitt Trigger is biased from an internally regulated three-V_{BE} supply to reduce any shift in the DC firing points due to supply voltage variations.

Transistors Q_{26}, Q_{27} and Q_{28} make up the Schmitt circuit which is set in the monaural mode when the external control voltage approaches zero. Under this condition, Q_{26} is biased off and Q_{27} and Q_{28} are conducting. When turned on, transistor Q_{26} saturates and prevents any 19KHz signal from reaching the 19KHz amplifier, Q_3Q_4, by shunting the AC to ground. Now, when the DC control voltage rises to approximately two V_{BE}, there is sufficient bias to turn on Q_{26}. Transistor Q_{26} then fully saturates, removing bias from Q_{28} and allowing the 19KHz signal to be amplified. This sets the IC decoder in the stereo mode.

The circuit will remain in the stereo mode as the DC control voltage is decreased until there is insufficient bias to keep Q_{26} turned on; this occurs when the input control voltage has been reduced to slightly more than one V_{BE}. When bias is removed from Q_{26}, transistor Q_{28} will again saturate, once again setting the circuit in the monaural state. To summarize: the IC decoder remains in the monaural mode as the DC voltage at Pin 4 is increased from zero to approximately 1.3V. At this voltage the circuit will then switch to the stereo condition and remain in this state until the DC control voltage decreases below about 0.8V.

INTERSTATION AUDIO MUTE SWITCHING

Both IC multiplex decoders contain circuitry which will allow the audio signals to either pass normally or be attenuated by about 55dB in response to an external DC control voltage applied to Pin 5 of the IC. This feature allows both the µA729 and µA732 to be used in receiver designs which have Interstation Audio Muting. The audio mute switching is achieved with a Schmitt Trigger consisting of transistors Q_{18}, Q_{19} and Q_{20} whose operation and firing voltages are similar to those of the stereo monaural circuit previously described.

The muting Schmitt Trigger will be in the "Normal" or "Unmuted" mode when the DC voltage at Pin 5 is increased to approximately 1.3V. Under this condition the composite audio input signal passes normally to the stereo demodulator through input emitter followers Q_1 and Q_2. When the control DC voltage decreases to less than 0.8V, the mute Schmitt Trigger will switch into the "Muted" state with the audio input signal now being shunted to ground through transistor Q_{21}. To prevent a large DC transient when switching into the muted mode, DC bias to the demodulator is maintained by transistor Q_{15}.

OTHER CIRCUIT FUNCTIONS

Both the μA729 and μA732 contain circuitry consisting of a Schmitt Trigger switch and a power NPN stage for driving a high current stereo indicator lamp. The lamp driver switch (transistors Q_{22} and Q_{23}) is activated by the detected 19 KHz. When sufficient 19 KHz pilot is present (approximately 12mV RMS at the input) the Schmitt Trigger will be turned on by the resultant DC at Pin 14. When the Schmitt circuit is on, it allows the power NPN stage (Transistors Q_{24} and Q_{25}) to saturate, placing the full supply voltage across the stereo lamp. When the Schmitt Trigger switches to the off state, bias is removed from the lamp driver stage. This ensures that the stereo lamp will either be fully on or fully off, avoiding any ambiguity as to whether a stereo signal is present and also preventing the lamp driver from dissipating excessive power.

Both IC multiplex decoders contain a diode bias string (diodes Q_{29} through Q_{34}) to establish reference voltages for the stereo demodulator and switching circuits. Three regulator transistors (Q_{35} through Q_{37}) provide internal decoupling and improved regulation. These internal regulators essentially fix the operating currents of each stage and allow the IC to operate over a wide range of supply voltages.

TYPICAL PERFORMANCE CHARACTERISTICS

When operated with the recommended external components, typical performance of the μA729 and μA732 is detailed in Table I and in Figures 7 and 8. This performance was measured at $V^+ = 12V$, $T = 25^oC$ and with a standard 200mV RMS multiplex signal consisting of 10% pilot with L = R. (See Table I).

APPLICATION

External components required with the μA729 and μA732 are shown in Figures 5 and 6. The values indicated here should allow the IC decoder to be used directly in most FM stereo receivers. Since some component variations may be necessary to adopt this integrated circuit to existing receiver designs, the external component requirements are discussed briefly in the following sections.

Recommended characteristics for the 19KHz and 38KHz coils are detailed in Figures 5 and 6. These coil parameters will yield the separation and 19KHz sensitivity performance indicated in Table 1. The 38KHz coils should be tapped at a 10:1 turns ratio to provide a load impedance of approximately 1kΩ to 2KΩ at the collector of the 38KHz amplifier stage, Q_{10}. This will provide approximately 1.5V P-P of 38KHz switching signal at the stereo demodulator. Higher load impedances may result in 38KHz voltages large enough to saturate Q_{10}. Under this condition stereo separation will be degraded due to an unbalanced drive to the stereo demodulator. Similarly, if the load impedance is too low the 38KHz voltage will not fully switch the

current in the differential amplifier stages, resulting in reduced stereo separation.

To obtain the maximum stereo separation at all audio frequencies, the IC multiplex decoder and its associated circuitry should have no significant phase distortion. At low audio frequencies, phase shifts in the L+R component of the stereo signal can occur as a result of the high pass network formed by the input coupling capacitor C_5, and the input resistance of the IC decoder (typically 20KΩ). This can reduce low frequency separation and so establishes a minimum value for the input coupling capacitor (see Figure 9).

When the IC multiplex decoder performance is measured in an actual stereo FM receiver, the IF filter phase characteristic may cause some reduction in stereo separation, especially at higher audio frequencies. This effect may be compensated by an RC lead network in series with the audio input (Figure 10). The exact component values of the RC network will vary with each particular receiver design depending on the IF response

Because of the high inherent storecast (SCA) rejection of the IC decoder, SCA traps are not normally required. These SCA traps generally result in a phase shift of the high frequency L-R stereo signal components when used at the decoder input; consequently, the μA729 and μA732 possess better high frequency separation than most discrete multiplex decoders.

Depending on the receiver V^+ voltage and design characteristics, the recovered audio voltage available at the IC decoder input may vary considerably. It may therefore be necessary with some receivers to increase the 19KHz gain to provide optimum stereo performance. The 19KHz pilot level requirements may be adjusted by means of an external resistor in series with the second 19KHz tuned circuit (Figure 11).

The IC decoder is capable of supplying 100mA current to a stereo indicator lamp. This permits the μA729 and μA732 to drive high intensity stereo indicator lights directly, which makes these ICs particularly suitable for such applications as automotive radios which require a bright lamp. For maximum IC operating life, the lamp surge current during turn on should be limited to 500mA max. The stereo lamp should be returned to a low source impedance power supply; otherwise the large transient current which occurs when the stereo lamp is initially turned on may appear as a voltage spike at the multiplex decoder or audio preamplifier V^+. This voltage spike could then cause a "pop" to be heard at the audio output.

OPERATION AT DIFFERENT SUPPLY VOLTAGES

Both the μA729 and μA732 can function with DC supply voltages ranging from 8.0V to 14.0V. Operation over this wide supply voltage range is possible because most circuitry in the IC decoder including the output stages is biased from internal voltage regulators. Since the output currents are essentially independent of supply voltage, the external load resistor values may be increased at higher V^+ voltages

to increase the AC voltage gain. If the load resistor values are changed from those described in Figures 5 and 6, the de-emphasis capacitors should be altered accordingly to maintain a 75μsec de-emphasis characteristic. Recommended values for the load R and C are listed in Table 2.

TABLE 2

RECOMMENDED LOAD COMPONENT VALUES VS. MINIMUM SUPPLY VOLTAGE

Minimum Operating Supply Voltage	Load Resistors (R_2 and R_3)	De-emphasis Capacitor (C_6 and C_7)	Typical 1KHz Voltage Gain
8.0V	3.9KΩ	0.02μF	1X
10.0V	5.6KΩ	0.015μF	1.4X
12.0V	8.2KΩ	0.01μF	2.1X

ALIGNMENT OF THE IC MULTIPLEX DECODER

To obtain the full performance capabilities of the μA729 and μA732, alignment should be performed with a test signal obtained from a commercial FM stereo multiplex signal generator rather than from a broadcast stereo signal.

For the μA732, alignment with a multiplex generator should proceed as follows:

1. With a 19KHz pilot signal fed to the multiplex decoder (30 mV RMS nominally), peak L_1 and L_2 for a maximum reading at the second 19KHz filter (Pin 1).

2. With the same input as above peak L_3 the 38KHz coil, for maximum voltage at Pin 13.

3. With a Left only stereo signal (150 mV RMS) containing 10% 19KHz pilot, retune L_3 for a minimum reading on the Right Output (Pin 12).

4. With a Right only stereo signal, retune L_3 if necessary to obtain the same separation on both channels.

For the μA729 the following procedure is recommended:

1. Adjust the stereo separation potentiometer, R_5, to mid-range.

2. Repeat steps 1, 2 and 3 of the μA732 tuning procedure.

3. With a Right only stereo signal, adjust L_3 and the R_5 separation control to obtain the best separation. Retune L_3 and R_5 with a Left only input if this is necessary to obtain the same separation on each channel.

S

Since both IC multiplex decoders are capable of typical stereo separations that are typically 45dB, the crosstalk voltages may be less than the residual 19KHz and 38KHz signals. To adjust the decoders for separations greater than 35dB, it may therefore be necessary to add a high frequency RC filter to the audio output terminals to suppress these ultrasonic components.

MULTIPLEX DECODER WITH ONE 19KHz TUNED CIRCUIT

An alternate external component connection requiring one 19KHz tuned circuit is shown in Figure 12. The µA732 is illustrated here, although this technique could equally be applied to the µA729. The first 19KHz tuned circuit is replaced with an 820pF capacitor, which together with an internal 10KΩ resistor forms a low pass filter with a pole at 19KHz. In addition to eliminating one 19KHz coil, this approach results in simpler alignment of the two remaining tuned circuits. When now phased at their respective frequencies, the 19KHz and 38KHz tank circuits will require only a slight readjustment for maximum separation.

The above design approach does have two disadvantages. First, the 19KHz sensitivity will be reduced by 3dB. This may be partially compensated by increasing the Q of the remaining 19KHz tuned circuit and/or increasing the value of external resistor R_1. Secondly, false indications of the stereo lamp may now possibly occur when the FM receiver is tuned off center carrier frequency. Such mistuning may cause the recovered audio to be distorted and the high frequency distortion components near 19KHz may then activate the stereo indicator circuitry. Should any false operation of the stereo indicator lamp be encountered, it may be minimized by increasing the Q of the remaining 19KHz tuned circuit.

STEREO AND AUDIO MUTE SWITCHING

The following user options are available with the µA729 and µA732 either separately or in any combination:

Stereo/Monaural Automatic Switching
Interstation Audio Mute Automatic Switching
Stereo Only Signal Seeking

These functions are activated by external DC control voltages. As previously described, the Stereo/Monaural switching is controlled by a DC voltage applied to Pin 4 of the decoder IC; being set in the stereo mode when the DC control voltage is 1.3 V and returning to the monaural state when the DC voltage decreases to 0.8V. The interstation audio mute function is activated by similar DC voltages applied to Pin 5.

Some receiver designs may not require the interstation audio muting function. In this case the muting circuit may be permanently placed in the unmuted or normal mode by connecting a 22KΩ resistor between V^+ and Pin 5.

Most stereo FM receivers have a "Monaural Only" operating mode.

Under this condition, the stereo function is switched off by the listener to improve the audio quality when a weak signal or multi-path reception is encountered. With the µA729 and µA732 the 19KHz amplifier may be disabled by connecting the stereo/monaural control point, Pin 4, to ground. This sets the IC decoder in the monaural only condition. If desired, the IC may also be biased so the 19KHz amplifier is permanently on by connecting a 22KΩ resistor between V^+ and Pin 4.

To provide automatic switching of the above functions, the DC control voltages must be derived from a change in the FM signal conditions. Two general methods are employed: detecting the increase in IF voltage when a carrier is present; or detecting the reduction in the audio noise components as the RF input signal is increased. The first alternative is more commonly used and its implementation with an IF employing four µA703D IC IF amplifiers is shown in Figure 13. An audio bypass capacitor should be connected to the Pin 5 mute control to prevent any audio feedthrough at this point. The designer may choose to switch to the stereo mode at a somewhat higher RF signal than is required to open the audio channel. This is easily achieved by connecting Pin 4 to a DC divider as shown in Figure 13. If the IC decoder is used with receiver designs utilizing direct coupled IF amplifiers such as the µA754C FM IF integrated circuit (Reference 3), the IF voltage amplitudes available to drive a diode detector may not be adequate. Consequently, an active detector circuit may be required to obtain sufficient DC voltage to switch the IC decoder (Figure 14).

Deriving the DC control voltages by detecting the reduction in high frequency audio noise provides a sensitive indication of relative signal strength. Care must be taken with this method, however, to prevent the decoder from being falsely switched by SCA or audio distortion signals.

The µA729 and µA732 also have provision for operating in the "Stereo Only" mode, in which the multiplex decoder allows only stations broadcasting in stereo to be heard. One possible interconnection diagram for the "Stereo Only" function is shown in Figure 15. When the function selector switch is set to "Stereo Only," the 19KHz amplifier in the decoder will operate only when a strong carrier is received. If the station is also transmitting a stereo signal with a 19KHz pilot subcarrier a DC voltage will be developed at Pin 14 due to the detected 19KHz. When this DC voltage is connected to the muting control terminal (Pin 4), the audio channels will be unmuted. The net effect of this interconnection is to prevent any audio signals from being heard until the receiver is tuned to a strong station which has stereo modulation.

CONCLUSION

Operation and application of the µA729 and µA732 integrated circuit stereo demodulators has been described in this application brief. The excellent electrical performance which is maintained over a wide range of operating conditions makes these ICs suitable for most FM stereo receiver designs. By incorporating auxiliary circuit functions in the same chip, these devices may also provide a number of flexible user options.

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2. T. Hanna, "High Performance FM IF Amplifiers Using the µA703," Application Note 151, Fairchild Semiconductor

3. D. K. Long, "The µA754 TV/FM Sound System," Application Note 190, Fairchild Semiconductor

TABLE I

Supply Current	10	mA
Input Resistance	20	KΩ
Stereo Separation		
f = 100Hz	40	dB
f = 1KHz	45	dB
f = 10KHz	40	dB
Channel Balance (Monaural Input)	0.2	dB
Total Harmonic Distrotion	0.5	%
Voltage Gain	1	V/V
67KHz Storecast Rejection	55	dB
19KHz Pilot Level Required at Input for:		
Stereo Indicator Lamp on	12	mV RMS
Stereo Indicator Lamp off	8	mV RMS
DC Voltage Required at Pin 4 for Stereo Monaural Switching		
Stereo on	1.25	V DC
Stereo off	0.85	V DC
DC Voltage REquired at Pin 5 for Audio Mute Switching		
Audio on (unmuted)	1.2	V DC
Audio off (muted)	0.85	V DC
Mute Attenuation of Audio	55	dB
High Frequency Audio Components in Left and Right Outputs (dB below 1KHz output)		
19KHz	30	dB
38KHz	25	dB

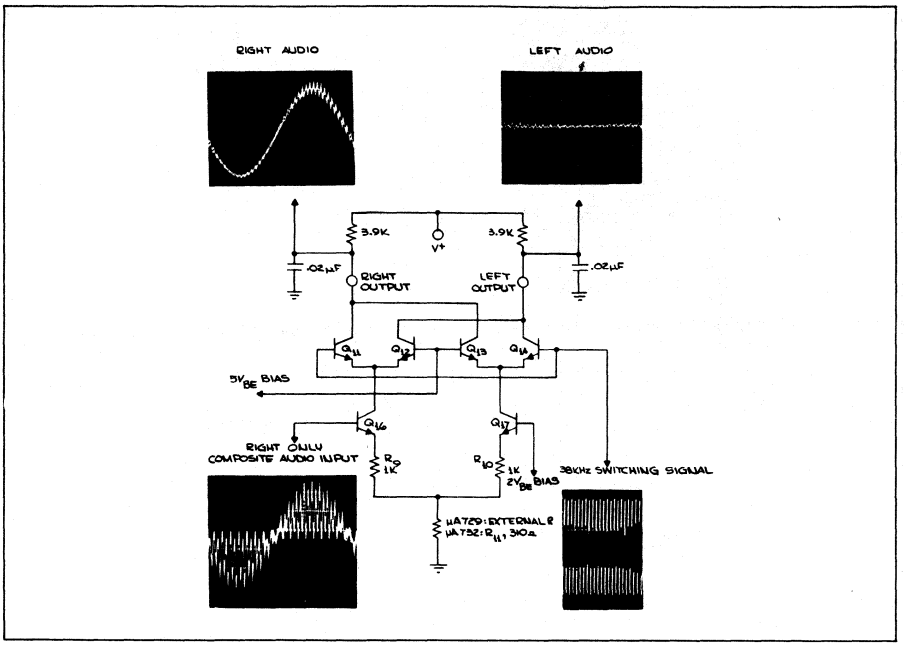


Fig. 1.

Basic Stereo Demodulator Circuit

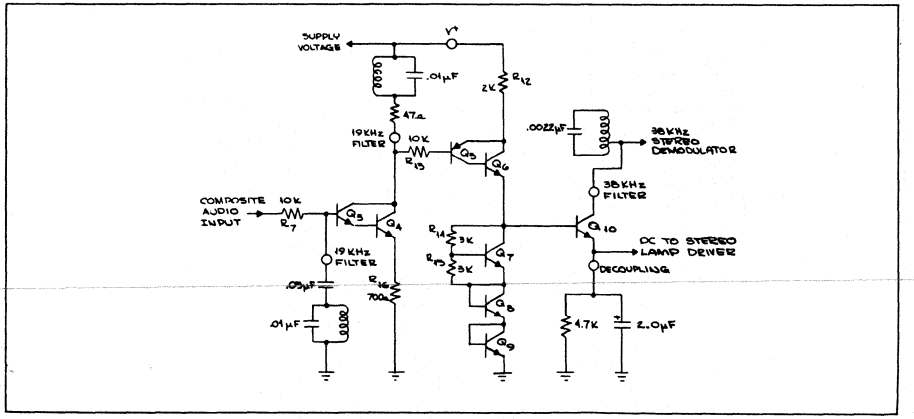


Fig. 2.

19kHz Amplifier/Doubler Circuit

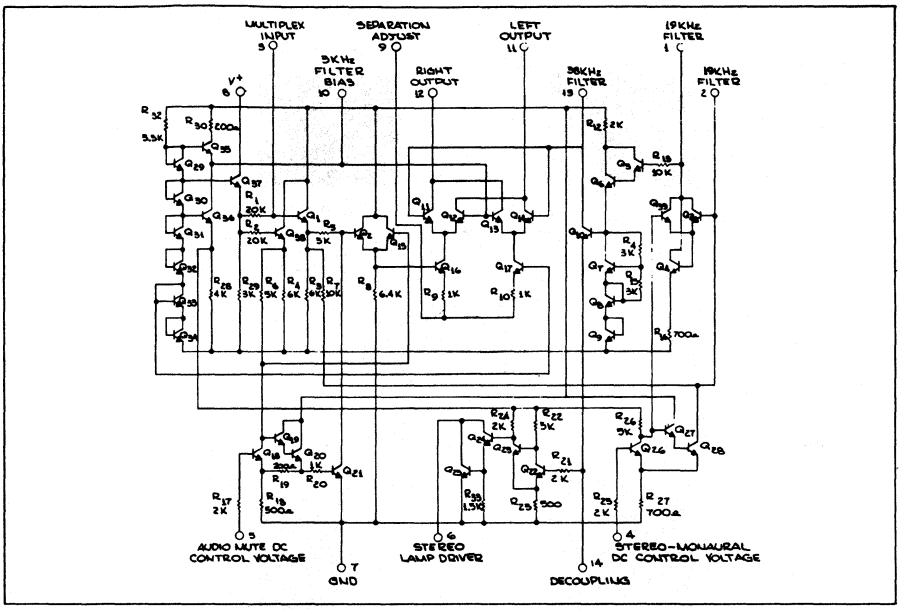


Fig. 3. µA729 FM Stereo Multiplex Decoder

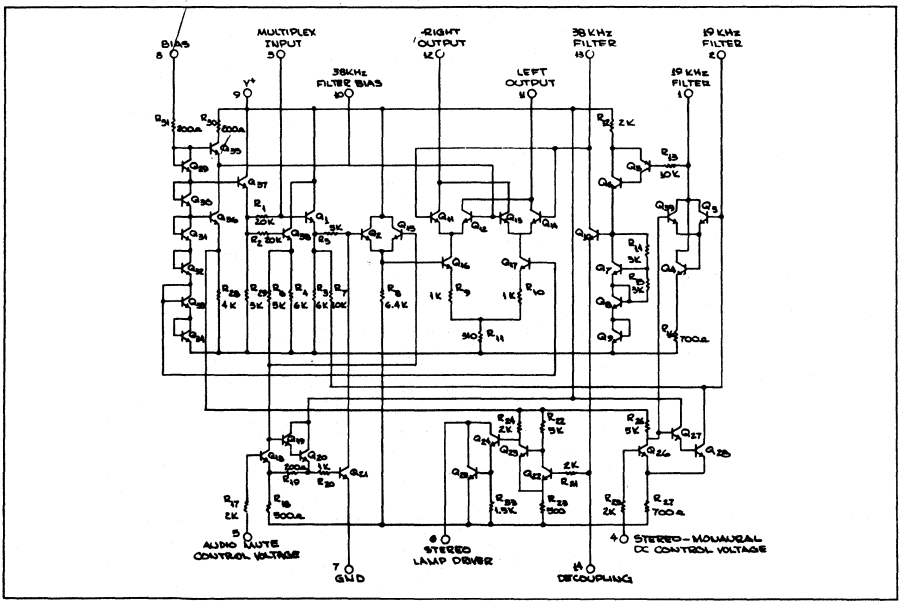


Fig. 4. µA732 FM Stereo Multiplex Decoder

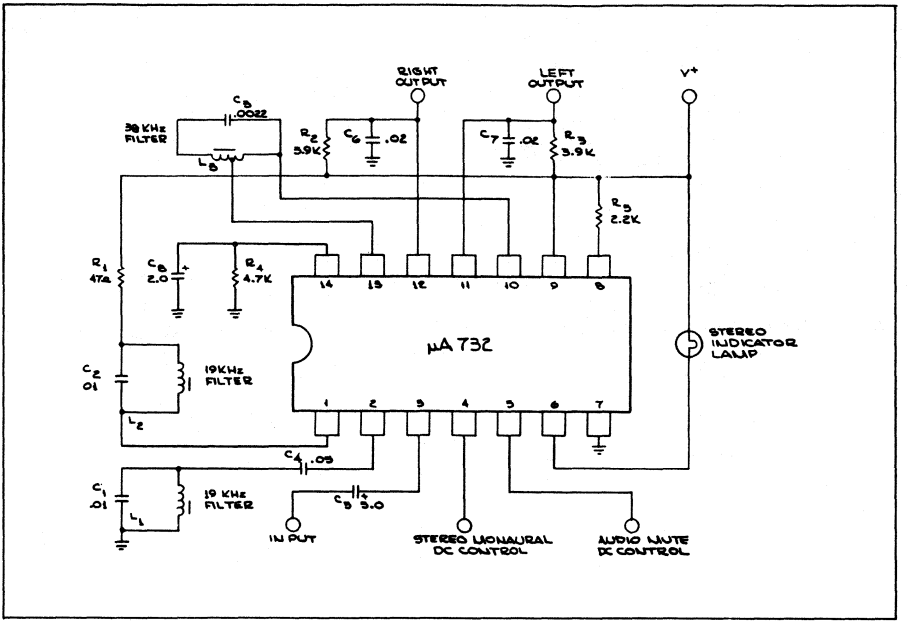


Fig. 5.

External Components Required with μA732 FM Stereo Multiplex Decoder

Notes:

L_1 and L_2 = 7.0 mH Nominal
Q_{UL} = 60
(Miller #1361 or equivalent)

L_3 = 8.0mH Nominal
Q_{UL} = 80
(Miller #1362 or equivalent)

C_1, C_2 and C_3 should be mylar or polystyrene.

All resistors in Ω.

All capacitors in μF.

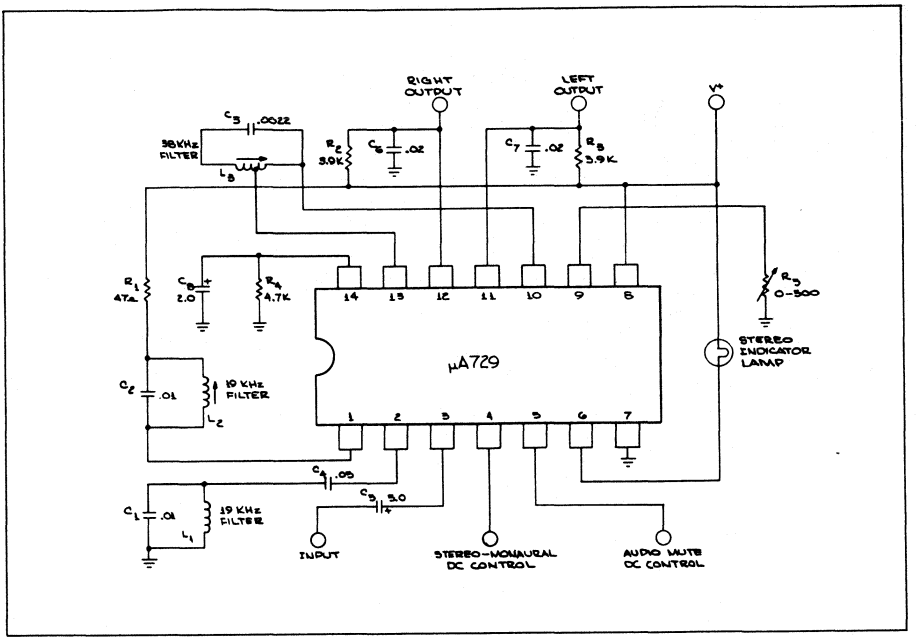


Fig. 6.

External Components Required with μA729 FM Stereo Multiplex Decoder

Notes:

L_1 and L_2 = 7.0 mH Nominal
Q_{UL} = 60
(Miller #1361 or equivalent)

L_3 = 8.0mH Nominal
Q_{UL} = 80
(Miller #1362 or equivalent)

C_1, C_2, and C_3 should be mylar or polystyrene.

All resistors in Ω.

All capacitors in μF.

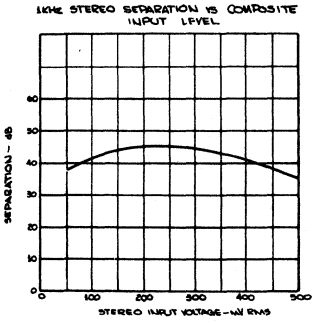


Fig. 7.

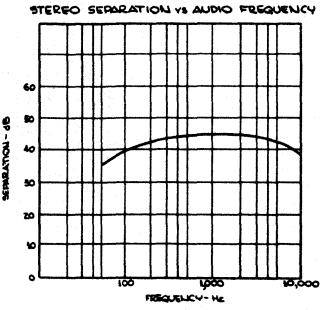


Fig. 8.

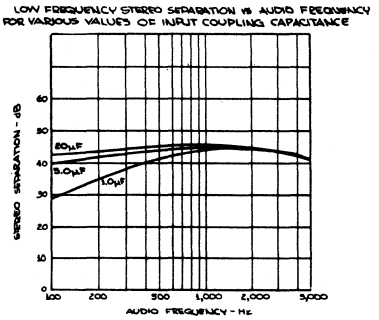


Fig. 9.

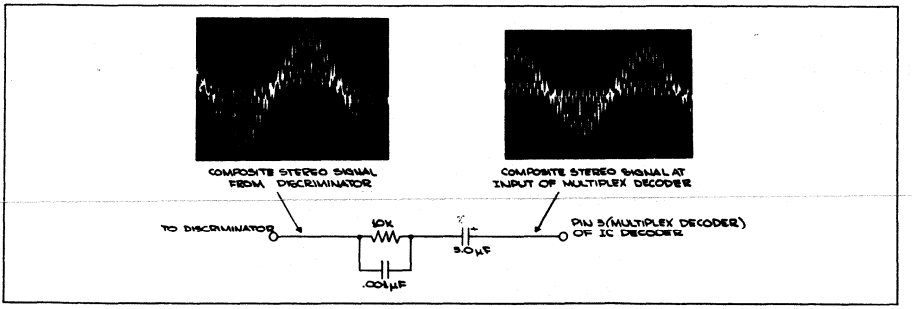


Fig. 10.

Effect of Input Phase Correction Network on 1kHz Right Only Composite Stereo Signal

Fig. 11.

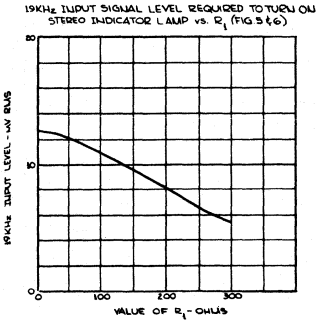
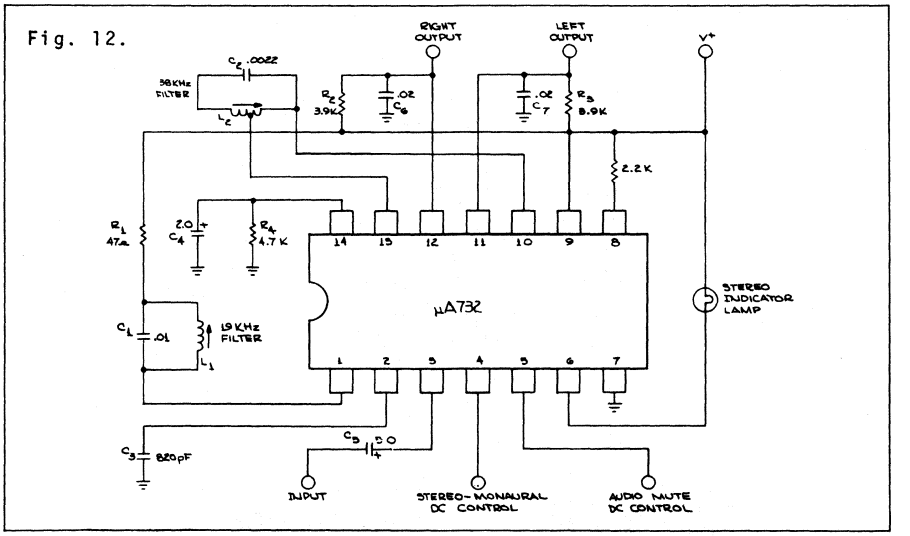


Fig. 12.



μA732 Alternate External Component Connection Using One 19kHz Coil

Notes:

L_1 = 7.0 mH Nominal
Q_{UL} = 60
(Miller #1361 or equivalent)

L_2 = 8.0 mH Nominal
Q_{UL} = 80
(Miller #1362 or equivalent)

C_1 and C_2 should be mylar or polystyrene capacitors.

All capacitors in μF unless specified.

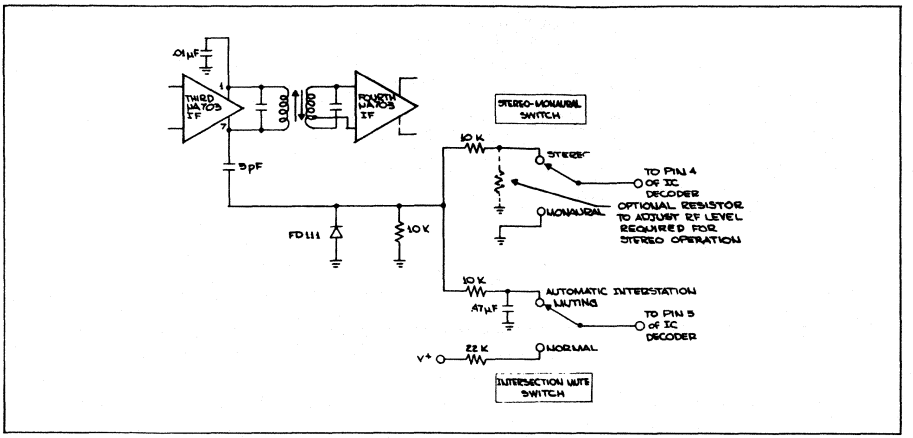


Fig. 13.

Detector and Switching Circuitry Required to Use Multiplex Decoder with Four Stage μA703 IF

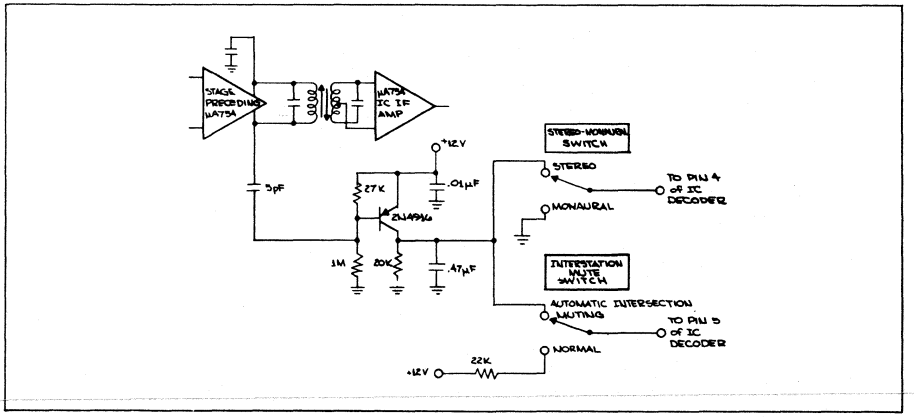
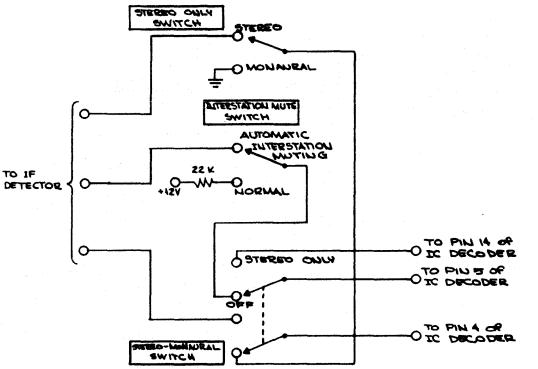


Fig. 14.

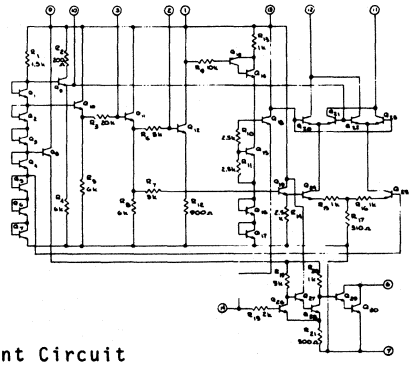
Active Detector and Switching Circuitry Required to Use IC Multiplex Decoder with μA754 IC FM Amplifier

Fig. 15.



One Possible Arrangement for Full Auxiliary Function Switching

FIG. 16



μA767 Equivalent Circuit

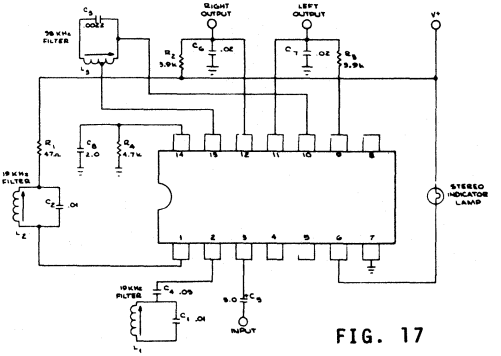


FIG. 17

NOTES:
L_1 AND L_2 = 7.0MH NOMINAL
Q_{UL} = 60
(MILLER #1361 OR EQUIVALENT)
L_3 = 8MH NOMINAL
Q_{UL} = 80
(MILLER #1362 OR EQUIVALENT)
C_1, C_2, AND C_3 SHOULD BE MYLAR OR POLYSTYRENE.
ALL RESISTORS IN Ω.
ALL CAPACITORS IN μF.

External Components Required with μA767 FM Stereo Multiplex Decoder

HIGH-PERFORMANCE FM-IF AMPLIFIERS USING μA703

ABSTRACT

Four-stage, integrated FM-IF amplifiers are discussed and compared in relation to component count and performance characteristics. Design notes for four-stage, integrated FM-IF amplifiers and a three-stage, integrated FM-IF amplifier are given. FM-IF transformer characteristics and an FM-AM integrated IF amplifier are discussed in the Appendices.

DISCUSSION

This note describes integrated FM-IF amplifiers or strips (using μA703's) whose performance compares favorably with the higher quality discrete component IF strips (e.g., using SE1001's) currently available. A capture ratio of less than 1 db is obtained with an integrated four-stage amplifier. The performance of this strip, as compared to high-quality discrete ones, is tabulated in Table I. All measurements were made with a signal generator connected into the strip rather than into a tuner, since the input impedance of the μA703 is typically 0.35 + j 0.6 mmho, compared to 0.8 + j 1.4 mmho for an SE1001. Also, audio output was taken directly off one side of a balanced 10-KΩ load through a 75-μsec de-emphasis filter. Except where otherwise specified, measurements are as per Institute of High Fidelity Standards Manufacturers, IHFM-T-100, Addendum I.

TABLE I.
PERFORMANCE OF FOUR-STAGE FM-IF USING (1) IC's and (2) DISCRETE DEVICES.

MEASUREMENT	PERFORMANCE	
	Integrated Circuits	Discrete Devices
Sensitivity	11 μV	16 μV
Capture Ratio at 100μV	0.85 db	2.92 db
Selectivity (-30 db, 100% modulated)		
Alternate channel	-46 db	-45 db
AM Rejection	-44 db	-37 db
Bandwidth (-3 db)	180 KHz	180 KHz
Output Voltage into 10 KΩ	0.30 V rms, balanced	0.35 V rms, balanced
Distortion at 1000 Hz	0.3%	0.3%
Supply requirements	38 mA at 12 VDC	22 mA at 12 VDC

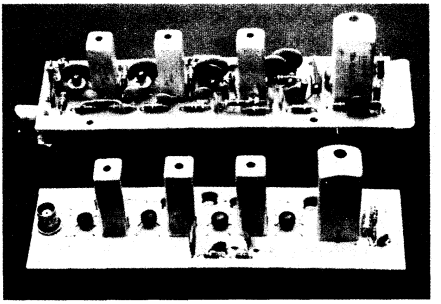


Fig. 1. FM-IF strips showing assembly with discrete components (top view) and clean, simplified construction with integrated circuits (bottom view).

The component count of this strip compared to a high-quality discrete component strip is given in Table II and shown photographically in Fig. 1. Four μA703 integrated

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RF-IF amplifiers are used, resulting in a clean, easily assembled strip.

TABLE II.

FOUR-STAGE FM-IF STRIP COMPONENT COUNT--COMPARISON.

COMPONENT	DEVICE COUNT	
	IC Board	Discrete Board
Semiconductors		
Active	4	5
Diodes	4	4
Transformers	4	4
Resistors	4	30
Capacitors	14*	27
Coils/chokes	4*	1
	34 (27*)	71

*Two capacitors and two chokes could be eliminated by reducing the by-passing of the supply line. Two capacitors and one coil would normally be eliminated by link-coupling the IF input to tuner output transformer.

DESIGN NOTES

Four-stage Integrated FM-IF Amplifier

A coupling factor of kQ = 0.8 was chosen for the IF transformers in a four-stage FM-IF strip (Fig 2) for good phase linearity. The taps on these transformers are adjusted to present approximately 0.455 mmho to the output of the μA703 to ensure its operation in its current-limiting mode. The input of the μA703 sees approximately 5 mmho to make the secondary Q almost independent of normal device input parameter variations. (Winding data are given in Appendix 1.)

The ratio detector coil has a coupling factor of kQ = 1.4 for a wideband flat response. It is similar to TRW coil No. 21791, except that the bifilar primary is not required.

Single-Ended Four-stage FM-IF Amplifier

Periodic requests for single-ended output ratio detector circuits for use with the integrated FM-IF strip resulted in the development of the circuit in Figs. 3 and 4. The transformer used is a TRW 21732-R1. The board layout is as in Fig. 3. Performance of this modified strip is roughly equivalent to that of the original.

Three-stage Integrated FM-IF Amplifier

The characteristics in Table III may be obtained with three μA703 IF stages. The circuitry used is the same as for the four-stage, except for different IF transformers and, of course, one less stage (See Fig. 5.) The measurements were made according to IEEE Standard No. 185 but with the signal fed directly into the IF.

TABLE III.

THREE-STAGE INTEGRATED FM-IF CHARACTERISTICS.

MEASUREMENT	PERFORMANCE
Quieting-Signal Sensitivity	18 μV
Co-Channel Interference (1000 μV)	-3 db
Selectivity (100 μV)	
Adjacent Channel	0.2 db
Alternate Channel	-19 db
AM Suppression (2000 μV)	-38 db
Bandwidth (-3 db)	190 KHz
Output Voltage (10-KΩ load, 30% mod.)	100 mV rms
Power Supply Requirements	15 V, 35 mA

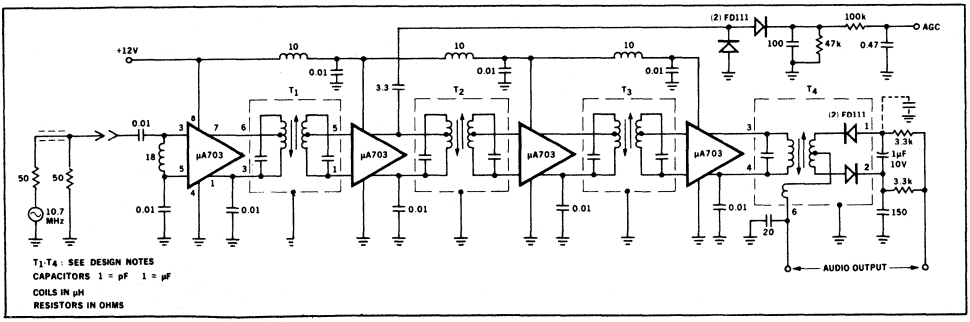


Fig. 2. Four-stage FM-IF amplifier.

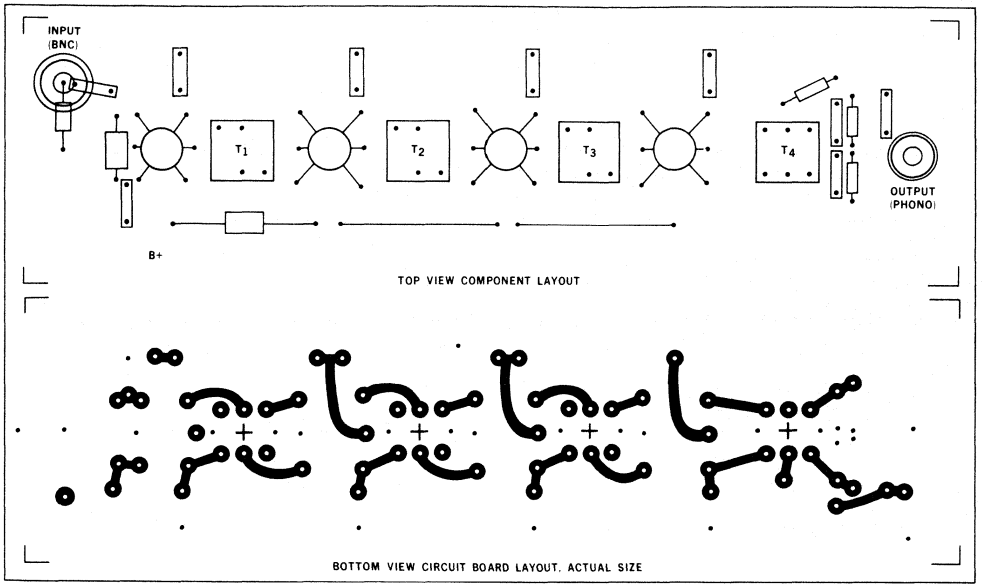


Fig. 3 FM-IF PC board layout using μA703's.

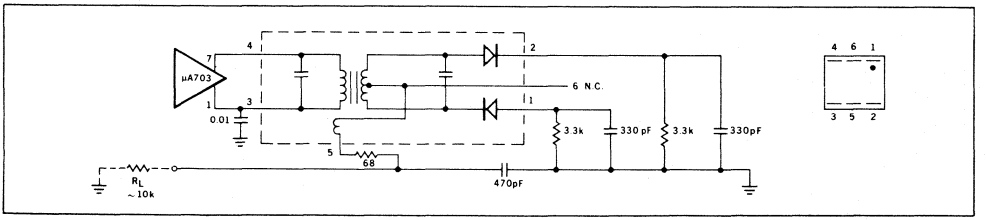


Fig. 4. Modified ratio detector with μA703.

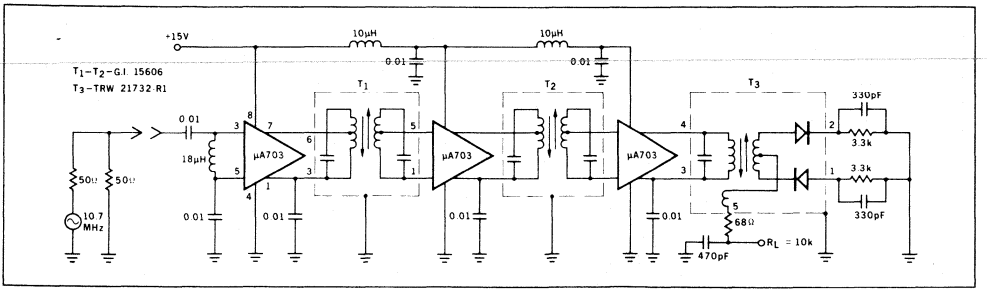


Fig. 5. Three-stage integrated FM-IF amplifier.

APPENDIX I.

FM-IF Transformer Specifications

Specifications for the transformers for both four-stage and three-state integrated FM-IF amplifiers are presented.

Transformer Specifications For Four-Stage μA703.

The transformer for the four-stage FM-IF μA703 has the characteristics given in Table IV. Figure 6 is a bottom view of the transformer.

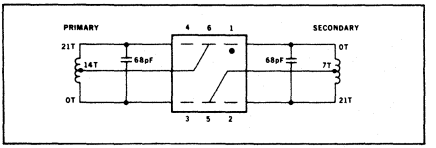


Fig. 6. Four-stage FM-IF transformer, bottom view.

Transformer Specifications For Three-Stage μA703.

The transformer specifications for the three-stage FM-IF μA703 are presented in Table V. The transformer circuit (bottom view) is shown in Fig. 7.

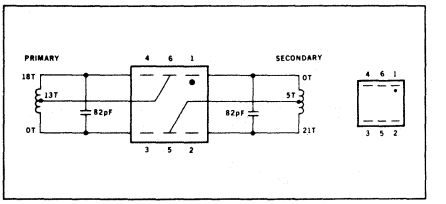


Fig. 7. Transformer for three-stage FM-IF.

TABLE IV.

TRANSFORMER SPECIFICATIONS FOR FOUR-STAGE μA703.

ITEM	SPECIFICATION
Wire	No. 36 SNB
Form	7/32" OD x 1-1/2" L (TRW 7M56BB1)
Cores (2)	TRW E0640
Capacitors (2)	68 pf, silver mica
Primary	21 turns (pins 3 to 4) Tap 14 Turns from cold end (pins 3 to 6), R_P = 19.3 KΩ $R_{P,tap}$ = 3.28 KΩ
Secondary	21 turns (pins 2 to 1) Tap 7 turns from cold end (pins 5 to 1), R_S = 19.3 KΩ $R_{S,tap}$ = 350Ω
Coupling	With 4.7-KΩ load, terminals 1 to 5, kQ = 0.8. In circuit bandwidth: -1 db at 2Δf = 180 KHz -3 db at 2Δf = 270 KHz -10 db at 2Δf = 490 KHz

TABLE V.

TRANSFORMER SPECIFICATIONS FOR THREE-STAGE μA703.

ITEM	SPECIFICATION
Wire	No. 36 Sodereze
Form	7/32" OD x 1-1/2" (TRW7M56BB1)
Cores (2)	TRW E0609E
Capacitors (2)	82 pf, silver mica
Primary	18 turns (pins 4 to 3), Q = 55. Tap 13 turns from cold end (6 to 3)
Secondary	21 turns (2 to 1), Q = 62. Tap 5 turns from cold end (5 to 1). With R_L = 3.9 KΩ, pin 5 to pin 1; Q measured across pin 2 to pin 1, Q = 55.
Coupling	With secondary loaded as above and resonated with 82 pf silver mica, primary Q = 30.5. In circuit: 3-db bandwidth = ±115 KHz.
Part No.	G.I. 15606

APPENDIX II.

FM-AM Integrated IF Amplifier

The high, stable gain of the μA703 can be used to advantage as an FM-AM IF amplifier. The block diagram in Fig. 8 shows a configuration in which the μA703 has been used successfully for FM-AM application.

If additional AGC is required, approximately 20-db AGC action can be obtained from Circuit No. 1 in Fig. 9, and 55 db from Circuit No. 2 in Fig. 10.

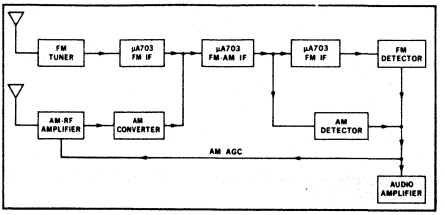


Fig. 8. Use of μA703 in FM/AM Amplifier.

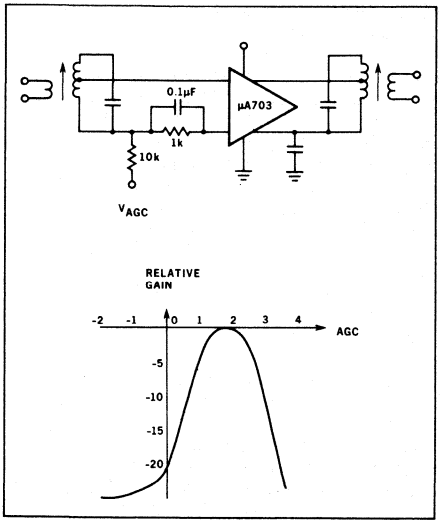


Fig. 9. AGC circuit No. 1.

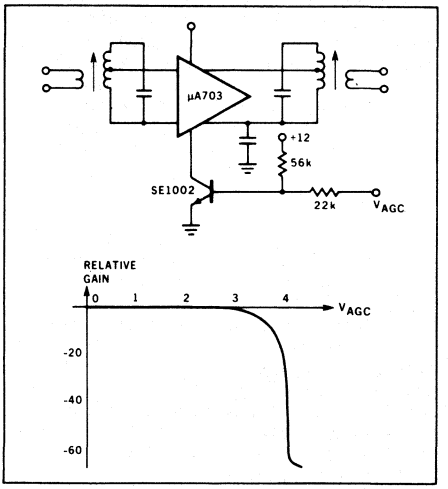


Fig. 10. AGC circuit No. 2.

A NEW APPROACH TO LOW DRIFT AMPLIFIERS

INTRODUCTION

Very low drift amplifiers are required in low level transducers and in precision analog computation. Existing circuits use closely matched bipolar transistor pairs or rely upon the inherent matching and close thermal coupling of monolithic integrated circuits to obtain drifts on the order of 5 to 10μV/°C. Individual trimming of these circuits is tedious, but permits voltage tracking of about 1 to 3μV/°C to be achieved.

Trimming, however, does not stabilize input bias and offset currents which may increase more than threefold as the ambient temperature decreases. FET input stages have been employed when input currents in the hundred pico-amp range were needed, but at the sacrifice of offset voltage drift. In addition, the input currents of the FET's double every 10°C, and therefore, quickly approach bipolar levels at higher temperatures.

Perhaps the most common method now used to obtain low drift is chopper stabilization, which can give excellent stability if properly designed. Their use is restricted in many applications, however, because of size, expense and performance drawbacks such as poor overload recovery, large shot noise and poor reliability. A fourth method is to use ovens on the critical components, but this usually ends in a compromise on which components can be stabilized because of the large amounts of power required.

A new technique using the unique advantages of monolithic circuitry is the temperature-stabilized substrate, where all components of the circuit are kept at constant temperature by an active regulator included on the chip. This approach can give drift performance approaching that of the best chopper-stabilized amplifiers, with small size, low cost, moderate power consumption and excellent reliability. The first circuit of this type was a simple transistor pair, put into volume production over 3 years ago. The design and production experience gained with this circuit as well as the improvements developed since that time, have made it possible to include a complete preamplifier on the temperature-stabilized substrate. Designated as the μA727, this circuit contains 24 active devices and 600kΩ of resistance, and illustrates the degree of complexity obtainable with second generation linear circuits. The device is a fixed gain, differential-input, differential-output preamplifier, designed to drive integrated circuit operational amplifiers and comparators such as the μA709 and μA710 as well

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as discrete and module amplifiers. It was not possible to integrate an entire operational amplifier on a stabilized substrate because changes in internal power dissipation resulting from driving moderate external loads would require too much power in the temperature regulator. The device's versatility would also be limited because it could not be used in front of comparators or other circuits. The combination of a μA727 and a μA709 provides a composite operational amplifier with a gain of 5 million, input resistance of 300MΩ, an offset voltage drift of 0.6μV/°C and an offset current drift of 2pA/°C.

CIRCUIT DESCRIPTION

Amplifier

The μA727 consists of a two-stage differential-input, differential-output amplifier and a temperature regulator. Its voltage gain of 100 is high enough to reduce the effects of drift in the following amplifier to a negligible value and yet not so high as to make frequency compensation difficult in operational amplifier applications. The device is mounted in a high thermal resistance package making tight chip temperature control with moderate power consumption possible.

Figure 1 is a simplified schematic of the amplifier section. The differential-input pair, Q_{12} and Q_{22}, is buffered with emitter followers Q_9 and Q_{24} to obtain an input resistance of 300MΩ and low offset and bias currents. Current source biasing of the emitter followers results in an input-offset voltage relatively independent of the base and leakage currents of the differential pair. It also doubles the differential input voltage range achieved with resistor biasing.

It is extremely important in low-drift amplifiers to maintain the input transistors at exactly the same temperature. The regulator circuit of the μA727 greatly reduces temperature changes seen by the chip, but slight thermal gradients across the chip may be present due to uneven heating, uneven die attach and edge effects. Even a 0.01°C temperature difference between the transistors in a pair will produce 20μV of offset drift. Two pairs of input transistors, however, allows them to be located on the chip which will cancel the effects of thermal gradients. The photomicrograph in Figure 2 shows that the emitter followers have been placed on opposite sides of the chip centerline from their corresponding amplifier transistors. If gradients are present across the chip, equal offsets will be produced in each half of the input stage thus producing a net drift of zero.

The second stage employs compound pairs of PNP and NPN transistors to provide level shifting and additional gain. The circuit uses lateral PNP's with current gains of about 1 to 3 connected in a feedback arrangement with NPN's to form high beta compound transistors. This minimizes loading of the first stage. Current source biased emitter followers are used at the output to provide low output resistance, reducing loading effects on the μA727 by subsequent circuitry. Zener diode D_2 and the voltage drop across the 10kΩ second stage collector resistors determine output common-mode voltage.

Temperature Regulator

Figure 3 shows the basic temperature regulator circuit which consists of a pair of temperature sensors, Q_6 and Q_7, a large power transistor, Q_4, and associated circuitry. Changes in chip temperature are sensed by Q_6 and Q_7 which develop a temperature dependent voltage across the external temperature adjust resistor, R_{adj}. This control voltage is applied to the base of the power transistor via Q_3 and D_1 and acts to change Q_4's collector current (and hence power dissipation), in a manner that retains a constant chip temperature.

The photomicrograph in Figure 2 illustrates the central location of the temperature sensors and the opposing

location of amplifier input stages and the heater transistor. The use of multiple emitters and multiple emitter resistors on the power transistor prevents current hogging, spreads power dissipation evenly across the chip, and reduces thermal gradients. Transistor Q_5 limits the initial turn-on current of the device, preventing possible damage to the power transistor. Stabilization after turn-on is rapid, with the chip temperature reaching 1°C of final value in one second. The R_{adj} resistor was made external to the chip to allow the user a wide selection of supply voltages, ambient temperature ranges and power consumption. A complete description of the regulator circuit is given in Reference 1.

Biasing

A complete schematic of the μA727 is shown in Figure 4. The amplifier and heater share common biasing at the anode of D_2 and the collector of Q_8. This arrangement with the selection of R_{adj} establishes amplifier current levels and chip temperature. High value pinch resistors have been used in many parts of the circuit to reduce operating currents without sacrifice of gain or chip area . Requiring a tenth of the area of equivalent base-diffusion resistors, these resistors can be well-matched, although control of absolute value is poor. As is the case with many monolithic circuits, the overall amplifier gain is determined by resistor ratios rather than absolute values, and no loss of performance results.

PERFORMANCE

Performance improvements achieved using the temperature-stabilized-substrate technique are illustrated in Table I. The μA727's superiority over non-stabilized bipolar input stages is obvious. Comparison with FET input stages (Figure 5) shows that the μA727 exhibits better offset drift for source resistances below 5MΩ, and due to the exponential behavior of the FET's leakage current, it has better drift for any source resistance for ambient temperatures above 45°C.

There is almost no change in any characteristic of the circuit over the full temperature range, due to the temperature stabilization. The only exception, of course, is power dissipation which varies inversely with temperature (Figure 6). In those applications where the maximum ambient temperature is less than 125°C, it may be desirable to lower the chip temperature and hence reduce the power required by the heater. This is accomplished by increasing temperature-control resistor R_{adj} to the value given by Figure 7. Variation in chip temperature as a function of ambient temperature is shown in Figure 8 for different values of R_{adj}.

Versatility of the μA727 is enhanced by the capability of operating over a supply voltage range of ±9 to ±18 volts with little degradation in performance. All that is required is a change in R_{adj} (Figure 9) to maintain constant chip temperature. Symmetry of supplies need not be maintained as long as the total voltage across the device is held between 18 and 36 volts. Since the output common mode voltage tracks the negative supply voltage, this feature enables the amplifier to be used with devices that have a limited input common mode range such as the μA702A and the μA730.

APPLICATION

In using the μA727 as a low-drift preamplifier, careful consideration must be given to drift in the other components used as well as the physical layout, in order to achieve optimum overall performance. Drift due to the post amplifier is usually insignificant due to the high gain and low differential load rejection of the μA727. A μA709 with drifts of 10μV/°C and 2nA/°C for example, contributes only 0.11μV/°C to the μA727's overall drift. Drift of the external passive components must be low, however, particularly in the offset nulling circuit. Here a drift of 50ppm/°C can, for instance,

cause up to 0.25μV/°C effective input drift.

Physical layout is another factor that can effect the drift performance. Since the μA727 must regulate its power dissipation to maintain constant chip temperature, best control is obtained if the case-to-ambient thermal resistance is kept as high as possible. Heat sinking of the can should therefore be avoided and moving air over the circuitry should be minimized. Precautions should also eliminate thermal-electric voltages produced by two dissimilar metals in contact. This can occur when component leads are soldered to a copper circuit board. Normally the thermo-electric voltage at one junction is cancelled by another (such as at the two input connections to the μA727); however, if the junctions are at different temperatures due to unequal air movement or heat sinking, an appreciable offset drift can result. The number of such junctions should therefore be minimized and should be placed as close together as possible to minimize temperature differences.

In operational amplifier applications, the frequency response characteristics of the μA727 and post amplifier must be shaped together to avoid oscillation when feedback is applied. As an assistance, the collectors of the input stage have been brought out for frequency compensation purposes. Each side has a 300Ω resistor in series with the compensation terminal. This eliminates the need for an external resistor in many cases. Response of the circuit of Figure 10 for various values of compensation components is given in Figure 11. Together with the corresponding characteristics of the operational amplifier, these curves, can be used to obtain stable performance in any specific application.

Since the μA727 can be used as a preamplifier for almost any circuit, the application possibilities are unlimited. A few of the more basic circuits are illustrated in Figures 12 through 15. The operational amplifier used may be either integrated circuit or module type. Frequency compensation has not been shown in detail because it is dependent upon the particular amplifier and circuit configuration employed.

CONCLUSION

Using the temperature stabilized substrate technique together with advances in process technology has resulted in a linear integrated circuit with very stable characteristics. The unique advantages of monolithic circuits are used in this design to provide a versatile preamplifier that may be used with most existing monolithic and module circuits over a wide range of power supplies. The performance attained equals or surpasses existing approaches, such as FET inputs or chopper stabilization, with the added advantages of small size, simple construction, good reliability and low cost.

TABLE I

TYPICAL ELECTRICAL CHARACTERISTICS

Input Offset Voltage	2mV
Input Offset Current	2nA
Input Bias Current	5nA
Input Offset Voltage Drift	0.6μV/°C
Input Offset Current Drift	2pA/°C
Input Bias Current Drift	15pA/°C
Differential Input Resistance	300MΩ
Input Voltage Range	±12V
Differential Input Voltage Range	±10V
Supply Voltage Rejection Ratio	50μV/V
Common Mode Rejection Ratio	90 dB
Output Common Mode Voltage	-5.0 V
Output Differential Voltage Swing	±6.0 V
Output Differential Load Rejection	5μV/μA
Differential Voltage Gain	100

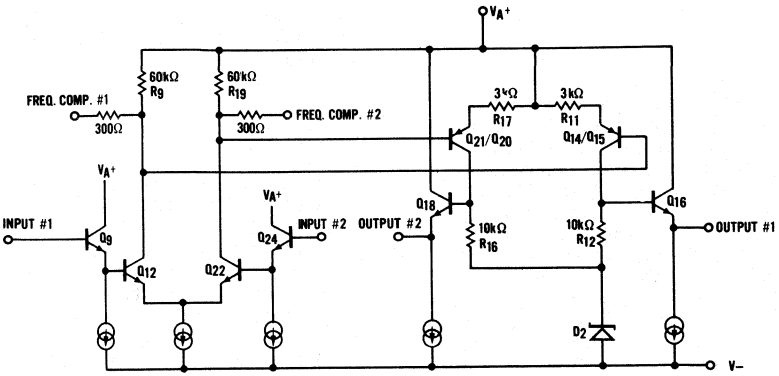


FIG. 1. SIMPLIFIED SCHEMATIC OF AMPLIFIER.

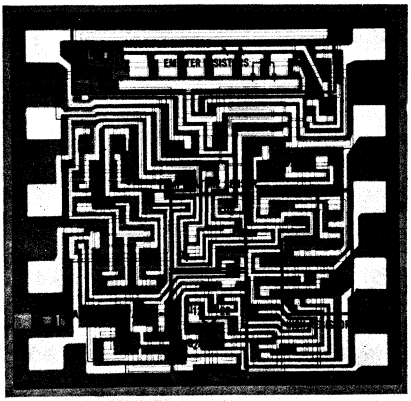


FIG. 2. PHOTOMICROGRAPH OF THE μA727.

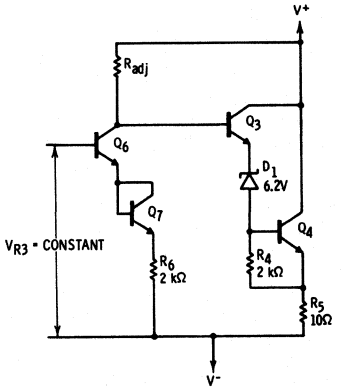


FIG. 3. SIMPLIFIED SCHEMATIC OF TEMPERATURE CONTROL CIRCUIT.

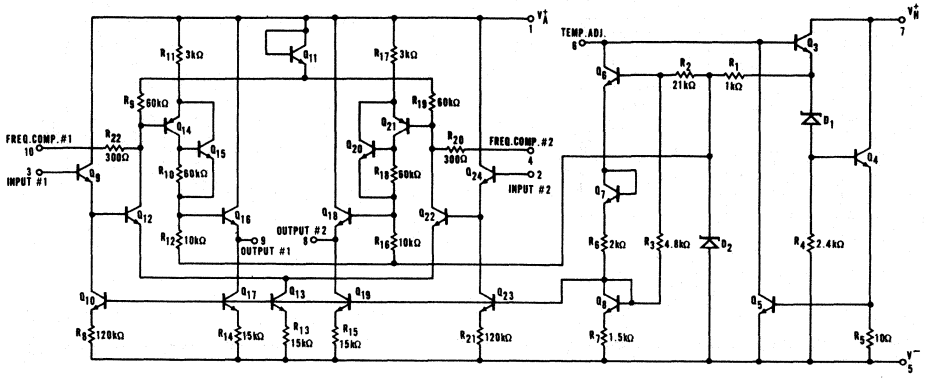


FIG. 4. COMPLETE μA727 SCHEMATIC.

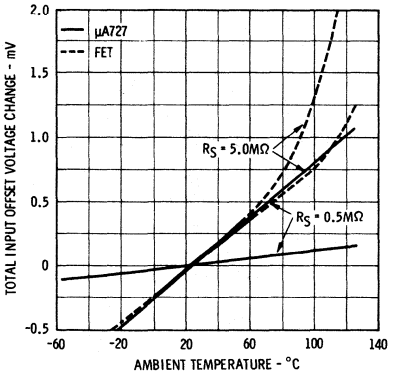


FIG. 5. COMPARISON OF TYPICAL FET INPUT STAGE WITH μA727.

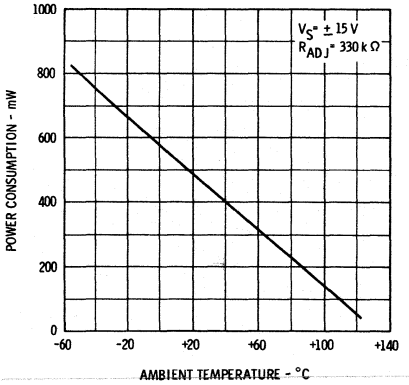


FIG. 6. POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE.

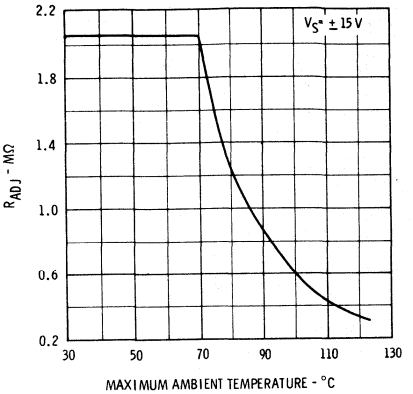


FIG. 7. RECOMMENDED R_{ADJ} AS A FUNCTION OF MAXIMUM AMBIENT TEMPERATURE.

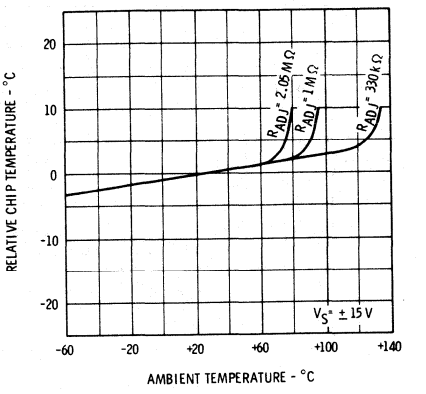


FIG. 8. RELATIVE CHIP TEMPERATURE AS A FUNCTION OF AMBIENT TEMPERATURE.

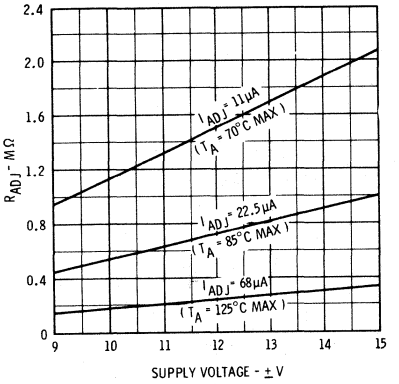


FIG. 9. REQUIRED R_{ADJ} FOR CONSTANT I_{ADJ} AS A FUNCTION OF SUPPLY VOLTAGE.

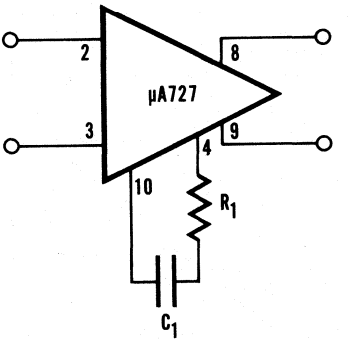


FIG. 10. FREQUENCY COMPENSATION CIRCUIT.

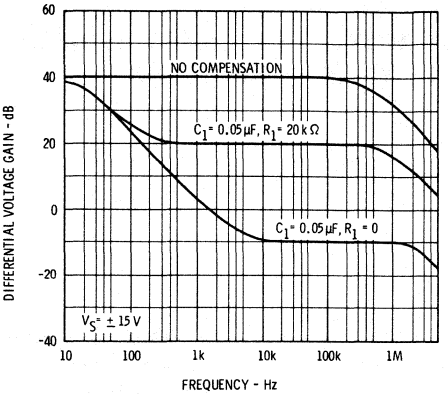


FIG. 11. OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF COMPENSATION.

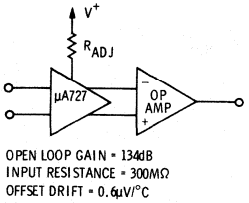


FIG. 12. PRECISION OPERATIONAL AMPLIFIER.

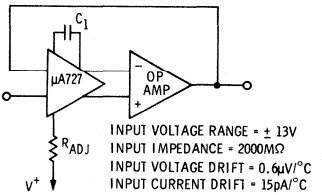


FIG. 13. HIGH PERFORMANCE VOLTAGE FOLLOWER.

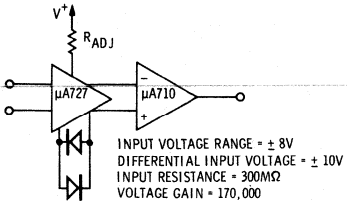


FIG. 14. PRECISION INTEGRATOR.

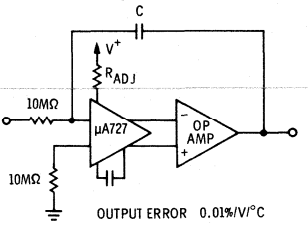


FIG. 15. HIGH INPUT IMPEDANCE COMPARATOR.

DESIGNING WITH THE μA703 MONOLITHIC RF-IF AMPLIFIER

INTRODUCTION

The IF-RF amplifiers and mixers in most receiving systems generally employ few components in addition to the tuned circuits. Since tuned circuits cannot be economically integrated using existing technology, use of the remaining components in integrated form will be worthwhile only if a substantial improvement in performance or stability can be obtained, or if simplified design procedures can be used.

These improvements are provided by the emitter-coupled amplifier, the μA703, shown in Fig. 1. Designed for use with transformers and/or tuned circuits, the μA703 eliminates the biasing resistors, bypass capacitors, and coupling capacitors required in conventional amplifiers. Operation is essentially unilateral, and the circuit has a symmetrical output current-limiting characteristic. This provides increased available power gain, simplified tuning, and superior limiting performance which greatly reduces the de-tuning, phase shift, and blocking that occur when conventional amplifiers saturate. The device may also be used as a harmonic mixer and is especially attractive when used as an FM limiter.

The biasing arrangement takes advantage of the closely-matched characteristics of integrated circuit transistors, while the dc return path for biasing the input and output is provided by interstage transformer coupling. A single voltage supply is all that is required for operation.

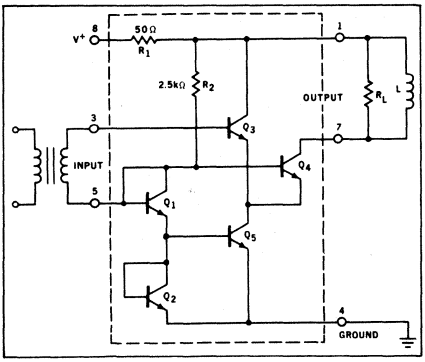


Fig. 1. Schematic diagram of the μA703.

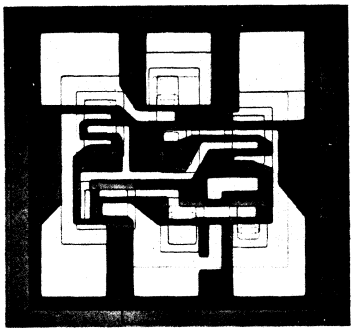


Fig. 2. Photomicrograph of the μA703.

The simplicity of the amplifier is demonstrated by the fact that it is constructed on a 20-mil-square silicon die (Fig. 2) -- a size which is small by comparison to many discrete transistors.

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Circuit Description

The dc biasing of the amplifier is easily understood, if it is assumed that all parts within the circuit are well matched and the transistor current gains are high enough that the base currents can be neglected. It is also assumed that the transformer windings, particularly in the input circuit, have negligible dc resistance.

The collector current of the biasing transistor, Q_2, is

$$I_{C2} = \frac{V^+ - 2V_{BE}}{R_2 + 2R_1} \tag{1}$$

Since $V^+ \gg 2V_{BE}$ and $R_2 \gg 2R_1$, this current is substantially independent of the transistor characteristics and is simply a function of the supply voltage and a single resistor.

The transistors are assumed to be identical, hence the collector current of the current source, Q_5, is equal to that of Q_{2_1} because their bases are fed from a common voltage point. The collector current of Q_5 splits evenly between Q_3 and Q_4 with zero input signal. When the amplifier is driven into limiting, this current is alternately switched between Q_3 and Q_4. To prevent saturation of Q_4 when the amplifier is driven with a large signal, the load resistance must be low enough that current limiting occurs before the output voltage drops to $2V_{BE}$. Thus, for a transformer-coupled output,

$$R_L \leq \frac{2(V^+ - 2V_{BE})}{I_{C2}} \leq 2R_2 \tag{2}$$

A more detailed analysis of the μA703 transfer function is given in Appendix I, along with some qualitative discussion of temperature and frequency effects. Curves of the two-port parameters are included to illustrate typical device characteristics.

RF Amplifier

Unneutralized small-signal amplifiers have a feedback path which can cause the real part of the input admittance of the device to become negative for certain combinations of frequency and load impedance. If this situation occurs and the source admittance is equal to or less than the negative real part of the input admittance, self-sustaining oscillations are possible. For the typical amplifier, the designer has one of two choices: feedback that is equal in magnitude and opposite in phase to that inherent in his device can be applied around the circuit, or the interstage coupling networks can be loaded sufficiently to make the input admittance always greater than zero. These solutions have major drawbacks -- neutralization is at best a marginal solution since it is very frequency-sensitive and must be different for each situation. Loading the interstages is less frequency-sensitive, but the resultant mismatch loss is not always tolerable. The most satisfactory solution would be to use a device which possesses negligible intrinsic feedback -- if something of that description does indeed exist. For the μA703, the internal feedback is an order of magnitude less than most high-frequency transistors. For example, a reverse transadmittance of less than 0.001 mmho at 10MHz is not unusual.

The effect of input and output loading on the stability of the amplifier can be best seen from the expression for power gain of the device. Characterizing the device as an active

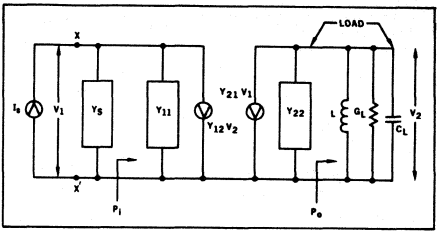


Fig. 3. Tuned amplifier equivalent circuit.

two-port and using short-circuit admittance parameters to describe its behavior gives the equivalent circuit shown in Fig. 3, where the following y-parameters have been used:

y_{11} - input admittance, $g_{11} + jb_{11}$

y_{12} - reverse transadmittance, $g_{12} + jb_{12}$

y_{22} - output admittance, $g_{22} + jb_{22}$

y_{21} - forward transadmittance, $g_{21} + jb_{21}$

Y_L - load admittance, $g_L + jb_L$

Y_S - source admittance, $g_s + jb_s$.

The expression for the input power for the circuit of Fig. 3 is:

$$P_i = |V_1|^2 R_e \left[Y_{in}\right] = |V_1|^2 R_e \left[y_{11} - \frac{y_{12}y_{21}}{y_{22} + Y_L}\right] \tag{3}$$

and the output power is:

$$P_o = |V_2|^2 R_e \left[Y_L\right] \tag{4}$$

From Fig. 3,

$$|V_2| = \frac{|y_{21}|\,|V_1|}{|y_{22} + Y_L|} \tag{5}$$

So

$$P_o = \frac{|y_{21}|^2 R_e \left[Y_L\right]}{|y_{22} + Y_L|^2} |V_1|^2, \tag{6}$$

and the power gain becomes

$$\frac{P_o}{P_i} = \frac{\left|y_{21}\right|^2 R_e\left[Y_L\right]}{\left|y_{22}+Y_L\right|^2 R_e\left[y_{11}-\frac{y_{12}y_{21}}{y_{22}+Y_L}\right]} \qquad (7)$$

It can be seen from Equation 7 that the amplifier will be stable if

$$R_e\left[y_{11}-\frac{y_{12}y_{21}}{y_{22}+Y_L}\right] > 0. \qquad (8)$$

Equation 8 can be manipulated to yield[2, 3]

$$2g_{11}(g_{22}+g_L) - R_e\left[y_{12}y_{21}\right] - \left|y_{12}y_{21}\right| > 0. \qquad (9)$$

If the power gain is reckoned from the terminals XX' (Fig 3), Equation 9 becomes

$$2(g_{11}+g_s)(g_{22}+g_L) - R_e\left[y_{12}y_{21}\right] - \left|y_{12}y_{21}\right| > 0. \qquad (10)$$

Inspection of the above equation reveals that, for unconditional stability at all frequencies for any combination of source and load conductance, y_{12}, the reverse transadmittance, must equal zero. Since in practice y_{12} is finite, the source and load conductances must be manipulated to satisfy the stability criterion.

If it is assumed in Equation 9 that the real part of y_{12} is nearly zero, an expression can be obtained which will lead to a useful figure of merit for a two-port.

If $R_e\left[y_{12}y_{21}\right]$ approaches zero, Equation 9 becomes

$$2g_{11}(g_{22}+g_L) - \left|y_{12}y_{21}\right| \geq 0. \qquad (11)$$

which for conjugate matching becomes

$$4g_{11}g_{22} \geq \left|y_{12}y_{21}\right|. \qquad (12)$$

For conditional stability,

$$4g_{11}g_{22} = \left|y_{12}y_{21}\right|. \qquad (13)$$

The maximum gain which can be obtained from the two-port when the device is neutralized and conjugately matched is, from Equation 7

$$\frac{P_o}{P_i} = \frac{\left|y_{21}\right|^2}{4g_{11}g_{22}} \qquad (14)$$

Using Equation 13, the maximum stable gain will be

$$GMS = \left|\frac{y_{21}}{y_{12}}\right|. \qquad (15)$$

Obviously, the smaller y_{12} is, the greater will be the potentially available stable gain. For very small values of y_{12}, the gain will be determined essentially by the input and output parameters of the device.[4] For typical high frequency transistors at 10 MHz, the GMS is 20 decibels, while a GMS of 40 decibels can be obtained for the integrated emitter-coupled amplifier. Thus, fewer stages are required to achieve a given total gain.

A simplified design procedure for a 30-MHz amplifier can now be presented which will serve to illustrate the practical aspects of the preceding discussion.

The first problem that must be considered is: "How much gain can be realized at a given frequency?" To evaluate this problem, consider Equation 15 and the device parameters listed in Table I (taken from the curves of Appendix I). At 30 MHz, the forward transadmittance, y_{21}, is equal to 32 mmho and the reverse transadmittance, y_{12}, is 0.004 mmho. The maximum stable gain, GMS, is therefore 39 decibels.

TABLE I.

DEVICE PARAMETERS.

PARAMETER	CONDITION	VALUE	UNITS
Input Resistance	V^+ = 12V, f = 30 MHz	1.7	kΩ
Input Capacitance	V^+ = 12V, f = 30 MHz	9.0	pF
Output Conductance	V^+ = 12V, f = 30 MHz	0.08	mmho
Output Capacitance	V^+ = 12V, f = 30 MHz	2.5	pF
Forward Transadmittance	V^+ = 12V, f = 30 MHz	32/140°	mmho
Reverse Transadmittance	V^+ = 12V, f = 30 MHz	0.004	mmho

To obtain this gain, two conditions must be satisfied by the circuit. First, the source and load admittances have to be conjugately matched to the device: otherwise maximum transfer of power from source to load cannot be obtained. Second, the layout of the components must be such that feedback from output to input is minimized.

The turns ratio of the input and output transformers are selected to provide a conjugate match to the device

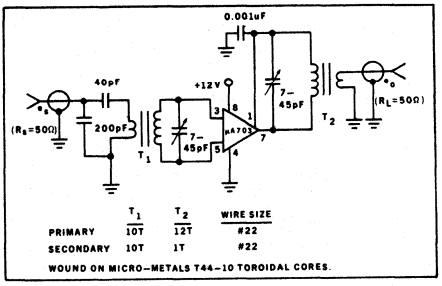


Fig. 4. The μA703 RF amplifier.

TABLE II.

AMPLIFIER PERFORMANCE.

PARAMETER	CONDITION	VALUE	UNITS
Power Gain	$V^+ = 12V$, $f = 30$ MHz	35	dB
Bandwidth	$V^+ = 12V$, $f = 30$ MHz	1	MHz
Noise Figure	$V^+ = 12V$, $f = 30$ MHz	6	dB
Power Gain (calculated)	Eq. 14	37.4	dB
Maximum Stable Gain	Eq. 7	39	dB

parameters listed in Table I. The actual circuit details are shown in Fig. 4, and the performance is listed in Table II. Excellent agreement is seen to exist between measured and calculated power gain. Interaction between interstage coupling networks is minimal.

Note that the amplifier does not utilize the limiting characteristic of the emitter-coupled pair and will saturate for large output swings. The input impedance does not drop, however, as the amplifier is driven into saturation.

Limiting RF Amplifier

The preceding discussion of the small-signal amplifier can be extended to limiting amplifiers without exception. The only additional requirement that must be fulfilled is that given by Equation 2, which ensures that the output transistor will not be saturated.

An amplifier which has a symmetrical output-voltage limiting characteristic can be obtained from the circuit of Fig. 4 by a minor modification in the output transformer. The effective turns ratio is adjusted so that the 50-ohm load, in parallel with the output resistance of the amplifier, causes the inequality of Equation 2 to be satisfied.

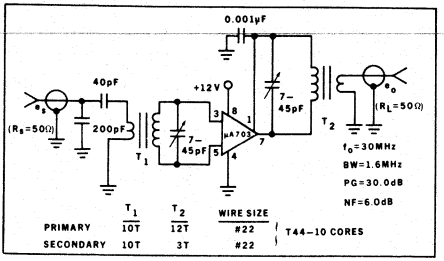


Fig. 5. Limiting RF amplifier.

For a 12-volt power supply and a 5-mA maximum collector current, the effective load should be less than 4.5 kilohms. Figure 5 shows the modified amplifier, designed for a 4500-ohm load and an output swing of 22 V_{pp}, with the measured performance characteristics.

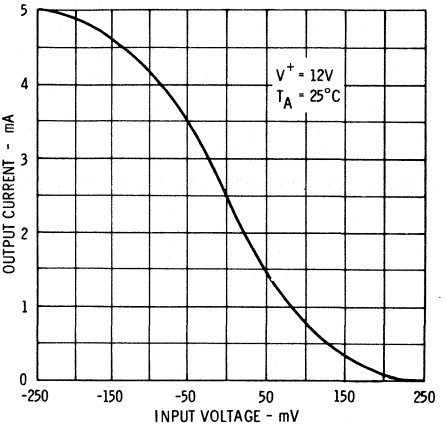


Fig. 6. Transfer function.

The current-limiting characteristic of the device is shown in Fig. 6. Fig. 7 shows the effect of large input signals on the input parameters.

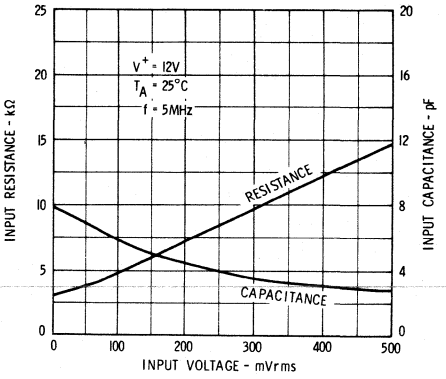


Fig. 7. Input parameters.

Oscillator

The design of transistor oscillators is complicated by the loading of the tank circuit caused by the decrease in input impedance of the device under large-signal conditions. The

usual solution is to provide some sort of impedance isolation between input and output, such as high turns ratio transformers or emitter followers in the feedback loop.

The input impedance of the μA703, however, tends to increase with large-signal inputs, as can be seen from Fig. 7. This simplifies the oscillator design, because the effect of input parameter variations can be neglected (depending upon the input voltage swing and becoming more valid for larger signals, but usually permissible for effective loads of 2 kilohms of less).

Predictable oscillator performance can be obtained by utilizing the Barkhausen criterion for oscillations, which states that the necessary and sufficient condition for oscillations to occur is:

$$1 - GH = 0, \tag{16}$$

where GH is the loop gain of the system; G is the forward transfer function, and H is the reverse (feedback) transfer function.

For the simplified equivalent circuit of Fig. 3 (assuming that the input admittance is small compared to the load admittance and the oscillator frequency is less than the corner frequency of the forward transadmittance), the forward transfer function is given by

$$G = \frac{V_2}{V_1} = \frac{y_{21}}{g'} \cdot \frac{1}{1 - j\omega L g' \left[1 - \frac{\omega^2}{\omega_o^2}\right]}, \tag{17}$$

where

$$\omega_o^2 = \frac{1}{LC'}$$

and C' = load capacitance, C_L, plus amplifier output capacitance, C_o

$$g' = g_L + g_{22}$$

Using a feedback transformer with a 1:1 turn ratio and assuming that the coefficient of coupling is unity (which is usually justified if a toroidal core is used), the reverse transfer function, H, will be equal to 1. Therefore, for oscillations to occur at $\omega = \omega_o$, the load conductance must be small enough that

$$\frac{y_{21}}{g'} \geq 1. \tag{18}$$

The effect of the phase shift contributed by the high frequency pole of y_{21} is to reduce the actual frequency of oscillation but, since in most tuned oscillators, a trimmer is used to set the final frequency, a more exact analysis is not justified. The effect of variations in input parameters was assumed negligible in the preceding discussion and any exact analysis must account for them, as well as the transformer coupling coefficient and losses.

The magnitude or the output voltage can be predicted quite well if the total voltage swing at the output collector of the device is allowed to be no more than 5 V_{pp} (since for a 1:1 transformer, the maximum input voltage rating of the device will be exceeded and the emitter-base junctions may be damaged), and the effective collector load resistor is

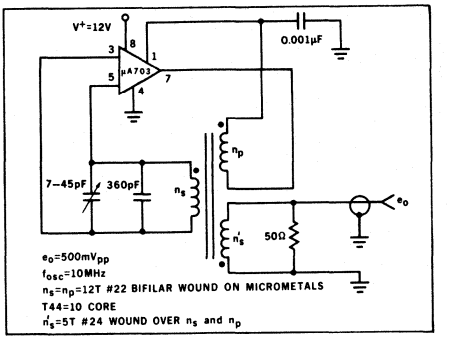


Fig. 8. 10-MHz oscillator.

small enough to ensure that current limiting occurs, but large enough that oscillations are maintained. The value of the load resistor can be determined from the expression

$$R_L = \frac{V_{pp}\ (\text{allowed})}{\text{max p-p output current}} \tag{19}$$

An oscillator was designed using the preceding criteria with the results shown in Fig. 8. The circuit was designed for a collector voltage swing of 2 V_{pp}, hence, from Equation 19, an effective load resistance of 400 ohms is required, using the typical maximum output current of 5 mA. Figure 9 shows an oscilloscope photo of the output waveform, and the frequency stability as a function of power supply appears in Fig. 10.

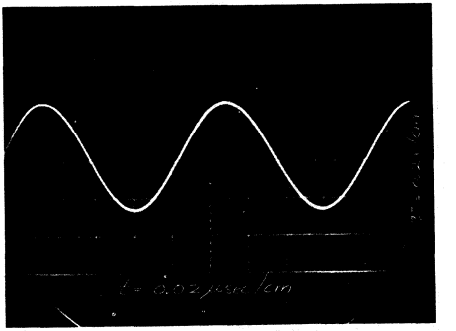


Fig. 9. Oscillator output waveform.

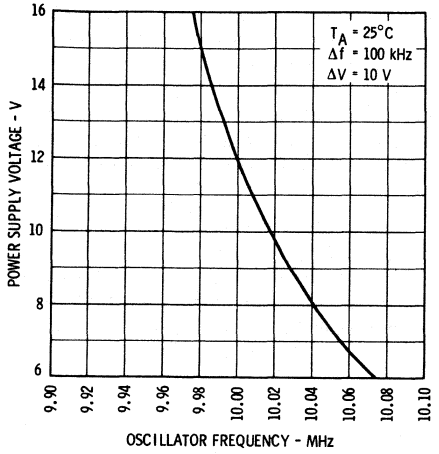


Fig. 10. Frequency stability of 10-MHz oscillator.

Harmonic Mixer

The transfer function of the μA703 is given by the function (discussed in Appendix I).

$$y_{21}(0) = -\frac{qI_{C4}}{kT}\left[1 - \frac{I_{C4}}{I_T}\right] \qquad (20)$$

This function describes the values of the small-signal transconductance for a specified source-to-output current ratio. What we would like to determine now is, which function will best describe the time varying transconductance, and how does the output compare to a conventional mixer? The answer to these questions may be found by substituting the expression for I_{C4} as a function of time into Equation 20. From Equation A-8 in Appendix I, the small-signal output current may be written,

$$i_{C4}(t) = io(t)$$

$$= I_T \,/\, (\exp qv_{in}(t)/kT + 1) \qquad (21)$$

since the source current, I_T, is constant and independent of input signal.

$$y_{21}(t) = -AI_T \frac{1}{\exp Av_{in}(t) + 1}\left(1 - \frac{1}{\exp Av_{in}(t) + 1}\right)$$

$$= -AI_T \frac{\exp Av_{in}(t)}{(\exp Av_{in}(t) + 1)^2}$$

$$= -\frac{A}{2} I_T \frac{1}{1 + \cosh Av_{in}(t)} \qquad (22)$$

where

$$A = \frac{q}{kT}$$

$$v_{in}(t) = V_{1o} \operatorname{Cos} \omega_{1o} t + V_s \operatorname{Cos} \omega_s t$$

V_{1o} = local oscillator voltage

V_s = signal voltage .

For the case we are considering, the amplitude of the signal must be much less than the local oscillator so that transconductance modulation of the μA703 is accomplished essentially by V_{1o}.

Since the displaced cosh function of Equation 22 is an even function, only components which are even multiples of the local oscillator frequency will be present in the output of the μA703. The graphical solution of Equation 22 is shown in Fig. 11 for the first three harmonics. A general algebraic solution is not attempted here, since it would provide little more than exercise. It can be seen from the figure that the large local oscillator drive generates components of the forward transadmittance which are even functions only.

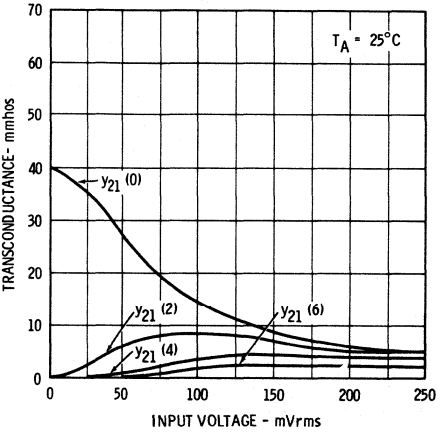


Fig. 11. Forward transconductance of emitter-coupled pair for even-order harmonics.

This "harmonic mixing" is more useful than a conventional mixer because of the lower frequencies and reduced filtering required. For example, it would be much easier to design a 50-MHz oscillator rather than a 100-MHz oscillator to use as a local oscillator. A possible configuration for the mixer is shown in Fig. 12. Reference 5 gives a more detailed description of the μA703 used as a harmonic mixer.

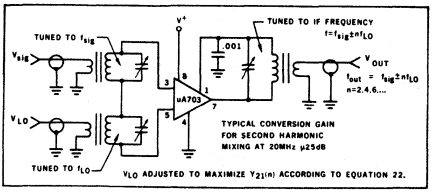


Fig. 12. The μA703 mixer connection.

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6. L. Blaser and N. Sturn, "Color Television Chroma Reference Systems Using Integrated Circuits, "APP 145, Fairchild Semiconductor Application Bulletin; 1967.
7. L. Blaser, "A Color TV Sound System Using the Fairchild μA703," APP 146, Fairchild Semiconductor Application Bulletin; 1967.
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APPENDIX

The analysis of the μA703 is simplified if the circuit is initially divided into a differential pair (Q_3 and Q_4 of Fig. 1) and their associated bias circuitry. Relationships may be derived between the transfer function of the pair and its terminal currents and voltages. Following this analysis will be a qualitative discussion of the bias circuitry. Since the signal processing takes place in the emitter-coupled pair, a detailed analysis of the bias network is not necessary. For convenience, Fig. 1 appears again as Fig. A-1; the configuration to be analyzed is shown in Fig. A-2, parts (a) and (b).

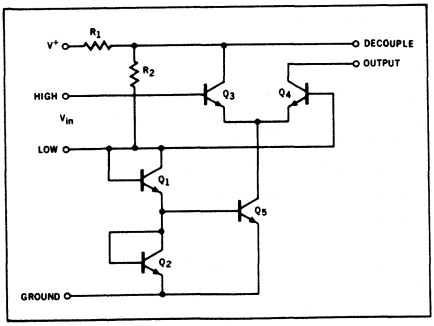


Fig. A-1. Schematic diagram of the μA703.

From elementary device considerations we recall that:

$$I_C = \alpha I_E \cong \alpha I_S \exp qV_{BE}\ kT. \qquad (A\text{-}1)$$

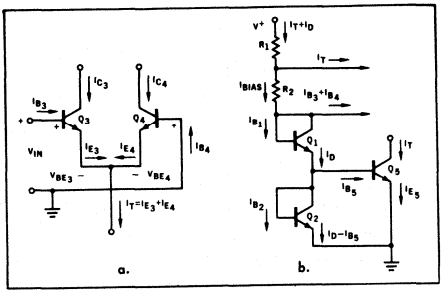


Fig. A-2. μA703 circuit for analysis.

This relates the collector current of a transistor to the base-emitter voltage via an exponential function and a constant I_S, which depends upon the particular geometry and processing used. The alpha term is the familiar common-base current gain of the device.

Manipulation of Equation (A-1) yields

$$V_{BE} = \frac{kT}{q} \ln \frac{I_c}{\alpha I_S}, \qquad (A\text{-}2)$$

and upon substitution of the appropriate quantities, this equation becomes:

$$V_{BE3} = \frac{kT}{q} \ln \frac{I_{C3}}{\alpha_3 I_{S3}}, \qquad (A\text{-}3)$$

$$V_{BE4} = \frac{kT}{q} \ln \frac{I_{C4}}{\alpha_4 I_{S4}}. \qquad (A\text{-}4)$$

From Fig. A-2(a),

$$V_{BE3} - V_{BE4} = Vin . \quad (A-5)$$

Substitution of Equations A-3 and A-4 in Equation A-5 yields

$$V_{in} = \frac{kT}{q} \ln \frac{I_{C3}}{\alpha_3 I_{S3}} - \ln \frac{I_{C4}}{\alpha_4 I_{S4}}$$

$$= \frac{kT}{q} \ln \frac{I_{C3}}{I_{C4}} + \ln \frac{\alpha_4 I_{S4}}{\alpha_3 I_{S3}} . \quad (A-6)$$

The second term of Equation A-6 depends upon the degree of matching that exists between the devices Q_3 and Q_4. Assuming reasonably close tolerances, this term is negligible and the input voltage is equivalent to

$$V_{in} = \frac{kT}{q} \ln \frac{I_{C3}}{I_{C4}} . \quad (A-7)$$

Since the sum of the collector currents of Q_3 and Q_4 is equal to the source current I_T, V_{in} may be expressed in terms of the ratio of total current to output current,

$$V_{in} = \frac{kT}{q} \ln \frac{I_T - I_{C4}}{I_{C4}}$$

$$= \frac{kT}{q} \ln \left[\frac{I_T}{I_{C4}} - 1 \right] . \quad (A-8)$$

The forward transadmittance of the μA703 may be obtained from Equation A-8 according to the two-port parameter definition

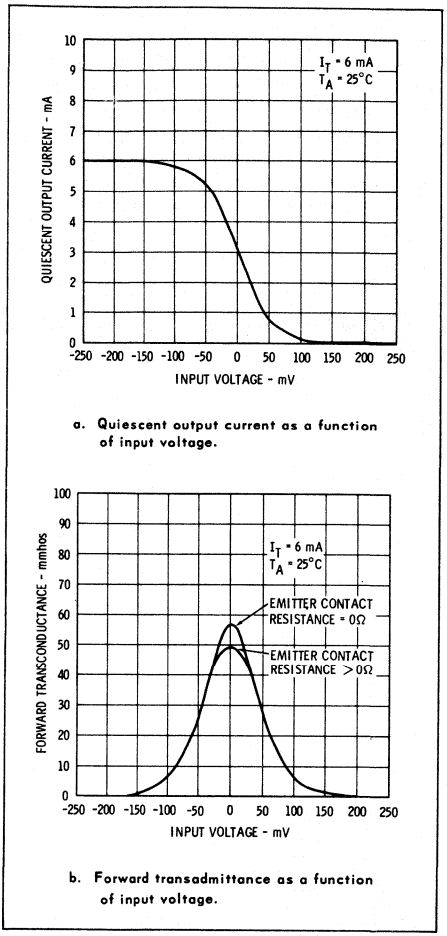
$$y_{21} = \frac{\delta I_o}{\delta V_{in}} \quad (A-9)$$

and is

$$y_{21} = 1/\frac{\delta V_{in}}{\delta I_{C4}}$$

$$= - \frac{qI_{C4}}{kT} \left(1 - \frac{I_{C4}}{I_T} \right) . \quad (A-10)$$

Since y_{21} is a function of the ratio of I_{C4} to I_T, Equation A-8 must be solved in order to evaluate y_{21} as a function of V_{in}. The graphical representation of Equation A-8 and A-10 are given in Fig. A-3 (a) and (b). Note that the forward transadmittance, y_{21}, is maximum when the collector currents of the device are equal and that, for matched devices, V_{in} equal to zero corresponds to an output current equal to one-half the source current. A large resistance between the input terminals causes V_{in} to become greater than zero because of the dc offset voltage produced by the finite base currents, I_{B3} and I_{B4}, and results in a shift of the operating point on the y_{21} curve to somewhat below maximum. Therefore, low dc source impedance or transformer coupling should be used with the μA703.



a. Quiescent output current as a function of input voltage.

b. Forward transadmittance as a function of input voltage.

Fig. A-3. Frequency variations in equivalence circuits.

The effect of the emitter contact resistance of Q_3 and Q_4 has not been included in the analysis. By simple superposition it can be shown that contact resistance merely decreases the maximum y_{21} available. The relative position of the maximum with respect to V_{in} is not altered. In addition, some desensitivity to input voltage will be realized because of emitter degeneration.

The total source current, I_T, is approximately equal to the bias current as given by the circuit description following the introduction. Limiting operation of the device is assured if the proper load resistance is used (Eq. 2).

T

The preceding analysis was based on an ambient temperature of 25 degrees centigrade and a frequency low enough to neglect the effect of the reverse transadmittance of the μA703. If the effect of temperature is included, one will find that output current will vary according to the saturation characteristics of the active devices and the variation of the integrated resistors. Frequency variation of the forward transadmittance will be quite evident above a few megahertz. Curves showing the variation of the two-port parameters of the μA703 are given in Figs. A-4 through A-7, while temperature stability of the quiescent operating point is indicated by Figs. A-8 through A-11. Additionally, quiescent operating conditions as a function of supply voltage are given in Figs. A-12 through A-13.

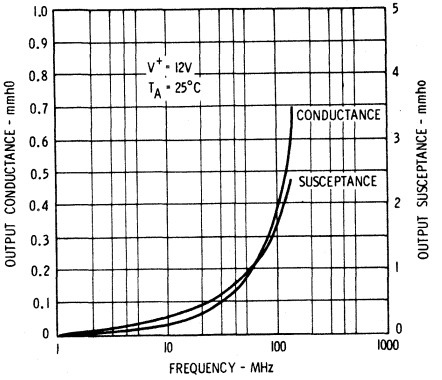


Fig. A-4. Output parameters as a function of frequency.

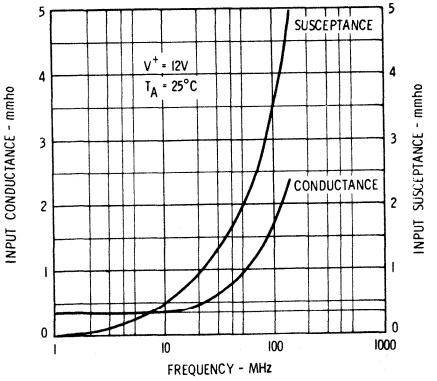


Fig. A-5. Input parameters as a function of frequency.

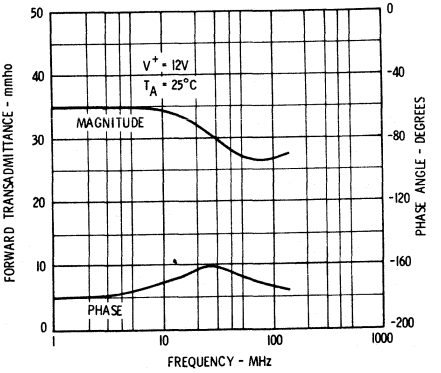


Fig. A-6. Forward transadmittance as a function of frequency.

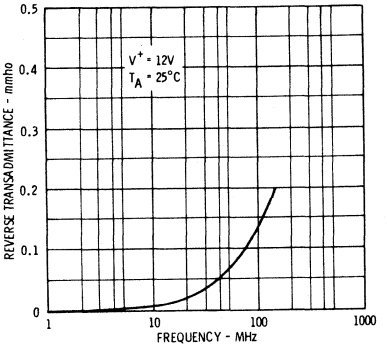


Fig. A-7. Magnitude of reverse transadmittance as a function of frequency.

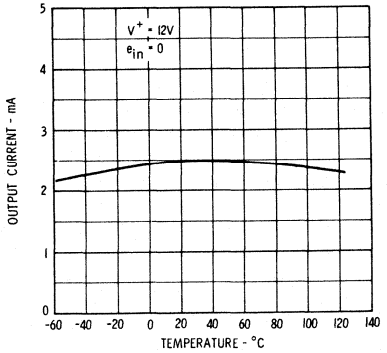


Fig. A-8. Output current as a function of ambient temperature.

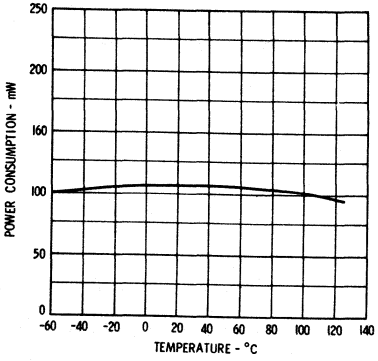


Fig. A-9. Power consumption as a function of ambient temperature.

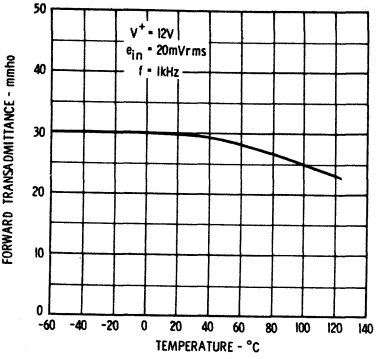


Fig. A-10. Transadmittance as a function of ambient temperature.

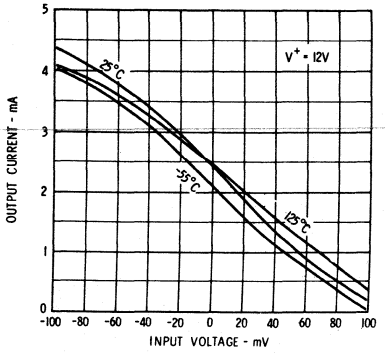


Fig. A-11. Output current as a function of input voltage.

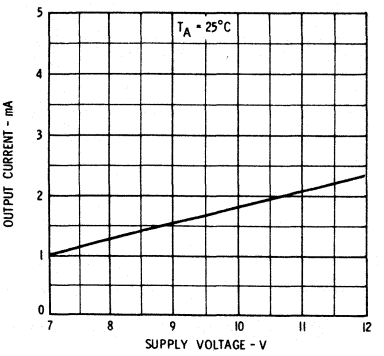


Fig. A-12. Output current as a function of supply voltage.

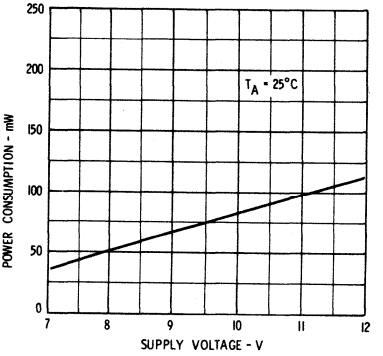


Fig. A-13. Power consumption as a function of supply voltage.

In general, the temperature and supply voltage sensitivities of the μA703 are present because of the voltage variation of biasing diodes, Q_1 and Q_2, and current source, Q_5. A change in the bias current source will cause a proportional change in I_T which will result in a modification of Equations A-1 through A-10. To evaluate, algebraically, the effect of these variations, one need only substitute the appropriate quantities in the above equations.

The frequency variation of the input, output and transfer admittances justify the equivalent circuit of Fig. 3 and are typical of any two-port.

APPLICATION OF THE μA722 10-BIT CURRENT SOURCE

INTRODUCTION

The purpose of this application note is threefold:

(1) to describe the characteristics of the μA722 in sufficient detail to enable advance designers to plan new subsystems around it;

(2) to present standard trouble-free designs for D/A and A/D converters using the μA722;

(3) to suggest system applications of D/A and A/D converters, especially those made feasible for the first time by the combination of performance, economy, and miniaturization which the μA722 and compatible IC's will offer.

Therefore, it is organized in three major sections, as follows:

I. Operating Principles, Performance, and Interface Requirements of the μA722.

II. D/A-A/D Conversion and Other Subsystem Applications of the μA722.

III. System Applications of μA722 Subsystems.

The treatment and style are intended to be comprehensive yet not exhaustive. Therefore, lengthy analyses and derivations have been omitted or relegated to the Appendix, in favor of directly useful information in the form of figures, tables, curves, and brief paragraphs outlining application principles and procedures.

I. OPERATING PRINCIPLES, PERFORMANCE AND INTERFACE REQUIREMENTS

General Description

The μA722 is a high-speed, 10-bit precision current source intended for use in current-summing digital-to-analog converters or as the feedback element in successive approximation analog-to-digital converters. It is constructed on a single silicon chip, using the Fairchild Planar* exitaxial process, and consists of a reference supply, 10 current sources connected to a single output summing line, and associated logic switches. The full-scale current and coding format are set by an external resistor array, which may be preselected and fixed for general usage or trimmed for greater accuracy. The μA722 is compatible with all Fairchild digital circuits, and with most linear circuits such as the μA702, μA709, μA710, μA741, and μA727.

SUMMARY OF TYPICAL OPERATING SPECIFICATIONS

Supply Voltages:	V^+	+6 Volts to +12 Volts
	V^-	-6 Volts to -12 Volts
Logic Levels:	Source "ON"	≤+0.5 Volts
	Source "OFF"	≥+2 Volts
Summing Line (Output) Potential		Virtual Ground ±.5 Volts
Emitter Resistors		See Table I
Resolution		1024 Parts
Range (Full-Scale)		0 to 2560 μA
Speed		0.6μsec/bit
Accuracy: Full-Scale (-20°C to +85°C)		±0.2% (including resistor tolerances)
Nonlinearity (+25°C)		±0.07% (fixed resistors); zero (trimmed resistors)
Total Error (-20°C to +85°C)		±0.2%* (including resistor tolerances)
Package		24-Lead Flatpack (1/4" x 3/8")

Circuit Description

A converter requires either accurate voltage or current switching. Current switching was chosen because it is generally more compatible with both the advantages and limitations of integrated circuits. Major advantages are:

(1) The excellent matching of collector current and base-emitter voltage permits accurately weighted currents to be generated that are stable over a wide range of temperatures.

* Planar is a patented Fairchild process.

* Full scale and nonlinearity errors are not additive (see Fig. 6).

FAIRCHILD SEMICONDUCTOR

(2) The current switching may be easily accomplished with excellent isolation between control and signal circuits without the use of capacitors or transformers.

(3) The accuracy of current switching is relatively independent of the device characteristics.

(4) The switching may be accomplished with acceptable speed using device structures compatible with linear integrated circuit requirements.

A simplified equivalent circuit for the μA722 is shown in Figure 1. The external resistor array sets the individual current source values. The bit control gates are controlled from the logic inputs with levels that are compatible with the various Fairchild Micrologic® integrated circuit families. The internal voltage reference establishes the proper bias for the current sources.

The basic circuit for each current source (Figure 2) consists of a level shifter (Q_{11}, D_{11}, and Q_{31}), a current steering network (Q_{21}, D_1), the current source transistor (Q_1), and an h_{FE} compensating circuit (Q_{41}, R_1). For maximum output impedance, the current source transistor is operated in a common base configuration. The value of the internal diffused emitter resistor (R_1) of Q_{41} was chosen to make the collector currents of Q_1 and Q_{41} approximately equal. If the two transistors are well-matched, their base currents will be equal and the collector current of Q_1 will be given by:

$$I_{C_1} = \frac{V_B - V_{BE_1}}{R_{E_1}} \qquad (1)$$

The bias voltage, V_B, is designed to have a temperature coefficient equal and opposite to that of V_{BE_1}, so that the voltage across R_{E_1} is held constant with temperature. Thus, I_{C_1} may be accurately controlled by the external precision resistor independent of transistor h_{FE} and V_{BE}, provided Q_1 and Q_{41} are well-matched.

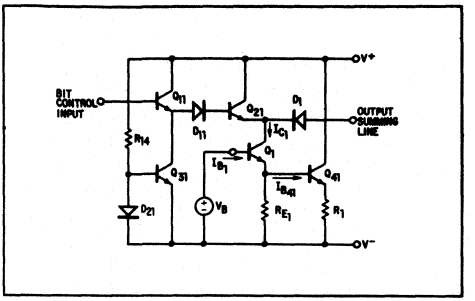


Fig. 2. Basic current source with switching network.

Switching is obtained by current steering. In order to be compatible with DTL, RTL, and CTL logic levels, a buffered level shifter is employed with the steering circuitry. When the logic level is high, the source current is provided from the logic side through Q_{21}, raising the collector voltage of Q_1 sufficiently to back-bias diode D_1 and thus keep the current out of the summing line. When the logic is low, the base of transistor Q_{21} is sufficiently negative with respect to the collector of Q_1 to turn off Q_{21}, allowing D_1 to be forward-biased, and drawing the current through the summing line. The converter consists of ten such current sources and switch networks, operating in parallel from a common reference supply. The complete circuit is shown in Figure 3.

The reference supply includes a stable voltage source and a voltage regulator. The regulator output provides the proper temperature compensating voltage reference level with a low source impedance. An external 200pF* capacitor is required at the frequency compensation terminal to protect against oscillation in the regulator.

* 200 pF is adequate; 1000 pF is best. See Fig. 13.

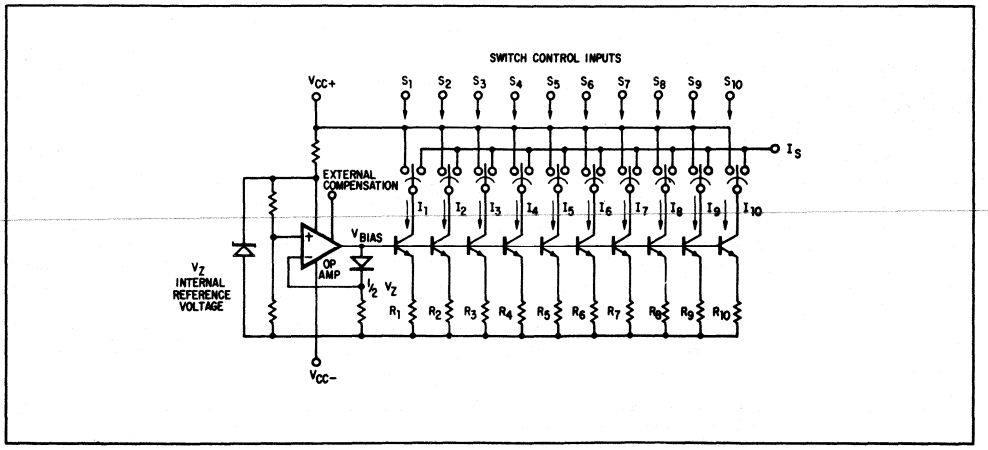


Fig. 1. Functional schematic: μA722 digital-to-analog converter current source.

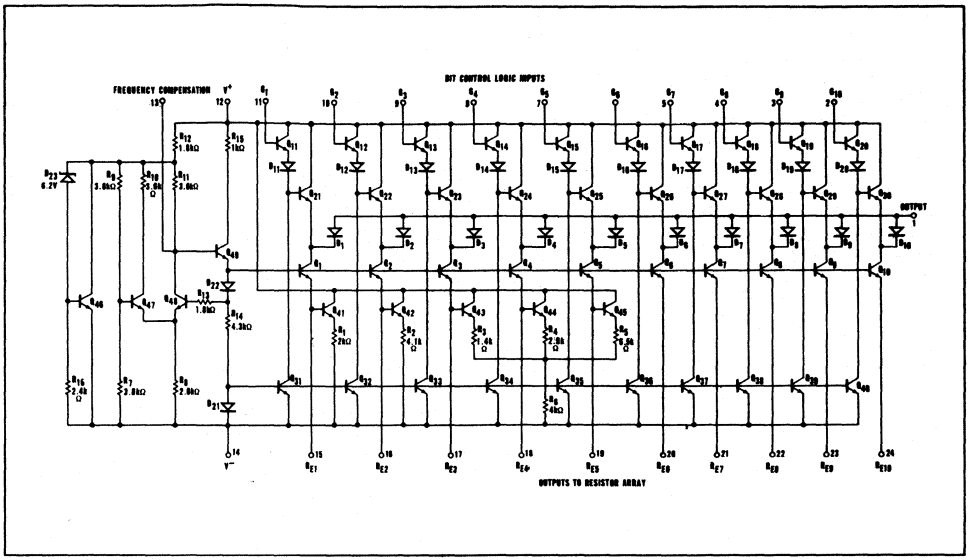


Fig. 3. Schematic diagram.

The converter maintains accuracy with ambient temperature variations as follows:

The regulator output versus temperature is tailored to maintain $V_B - V_{BE}$ constant. Diode D_{22} in the regulator feedback loop carries the same current density as the first two current source transistors, Q_1 and Q_2. Diode D_{22} and transistor Q_2 have identical geometries and carry a nominal 640μA. Transistor Q_1 has twice the emitter area of D_{22} and Q_2, and hence carries 1280μA. Therefore, D_{22}, Q_1, and Q_2 have the same V_{BE} and the same V_{BE} temperature coefficient, thus maintaining the emitter voltages of Q_1 and Q_2 constant over temperature. Other subsequent current sources have geometries identical to Q_2 but carry binarily decreasing currents and therefore have slightly differing temperature coefficients. However, the error resulting from this mismatch is small.

The emitter-follower circuits, Q_{41} through Q_{45}, compensate for temperature-dependent changes in the base currents of the current source transistors by removing a similar current prior to the external emitter resistor. If the external emitter resistors are near their nominal value (±10%), errors due to beta mismatch between the source transistor and the compensating transistor are small, as are errors due to the tolerance on the diffused emitter resistors for Q_{41} through Q_{45}. Since the ratio of bit current to full-scale current decreases towards the least significant bit, this compensation is required only on the first 5 current sources.

The current source transistors have high betas at the current levels of the most significant bits. This results in a bias current drawn by the 10 sources that is small compared to the 640μA flowing in the regulator diode. This, coupled with a low output impedance for the regulator, results in negligible reference voltage variations due to the temperature-dependent base currents of the current sources.

Diode D_{21} compensates temperature-dependent variations in R_{14} sufficiently to limit the current variations in diode D_{22} to less than ±5%. The resulting variations in the reference voltage are small enough to permit operation over a wide temperature range.

Selection of Emitter Resistors

An examination of the binary code resistor array values (Table I) indicates that resistors R_{E_3} to $R_{E_{10}}$ do not increase in an exact binary fashion. There are two reasons for this: first, the V_{BE}'s of current sources 3 to 10 do not match exactly the biasing diode voltage $V_{D_{22}}$; and second, the base currents of sources 6 to 10 are not compensated. The resistor array values given in Table I account for these factors and, if kept within the indicated tolerances, will give the overall accuracy specified for the converter. Recommended TCR values are given for accuracies ranging from 6 bits ±1/2 LSB to 9 bits* ±1/2 LSB over the restricted military temperature range, -20°C to +85°C. Obviously, they are conservative for reduced temperature ranges commonly specified for industrial and commercial equipment. The resistors R_{s1}, R_{s2}, and R_s' in Table I are discussed in the following subsections (see Eq. 1).

---

* Table I anticipates more accurate versions of the μA722 in the future.

TABLE IA.
BINARY CODE RESISTOR ARRAY

			6 Bit ±1/2 Bit Array Error = ±.8% Error Allocated to Resistors = ±.16%		7 Bit ±1/2 Bit Array Error = ±.4% Error Allocated to Resistors = ±.08%		8 Bit ±1/2 Bit Array Error = ±.2% Error Allocated to Resistors = 400 ppm		9 Bit ±1/2 Bit Array Error = ±.1% Error Allocated to Resistors = 200 ppm	
Resistor No.	Nominal Resistance Value kΩ	Nominal R/R_{E1} Ratio	Ratio Tolerance at 25°C %	T.C. max (-20°C -85°C) of Resistor Ratios ppm/°C	Ratio Tolerance at 25°C %	T.C. max (-20°C -85°C) of Resistor Ratios ppm/°C	Ratio Tolerance at 25°C %	T.C. max (-20°C to 85°C) of Resistor Ratios ppm/°C	Ratio Tolerance at 25°C %	T.C. max (-20°C to 85°C) of Resistor Ratios ppm/°C
R_{E1}	2.547	1.000	±10.0*	±50	±10.0*	±50	±10.0*	±20	±10.0*	±20
R_{E2}	5.094	2.000	± .10	±20	±.05	±10	±.02	± 5	±.01	± 2
R_{E3}	10.24	4.022	±.20	±50	±.05	±20	±.05	±10	±.02	± 5
R_{E4}	20.60	8.088	±.20	±50	± .10	±20	± .10	±20	±.05	±10
R_{E5}	41.43	16.26	±.50	± 100	±.20	±50	±.20	±20	± .10	±20
R_{E6}	81.93	32.17	± .50	± 100	± .50	±50	±.20	±50	± .10	±20
R_{E7}	163.4	64.16	±1.0	± 500	± 1.0	±200	± .50	±100	± .50	±100
R_{E8}	325.7	127.9	±1.0	± 500	± 1.0	±200	±1.0	±200	± .50	±100
R_{E9}	644.9	253.2	±5.0	± 1000	±2.0	±500	±2.0	±500	±1.0	±200
R_{E10}	1275	500.8	±5.0	± 1000	±2.0	±500	±2.0	±500	±1.0	±200

*Absolute tolerance on R_{E1}.

TABLE IB.
SUMMING RESISTOR TABLE CORRESPONDING TO IA. VALUES.

		6 Bit ±1/2 Bit Array Error = ±.8% Error Allocated to Resistors = .16%				7 Bit ±1/2 Bit Array Error = ±.4% Error Allocated to Resistors = .08%				8 Bit ±1/2 Bit Array Error = ±.2% Error Allocated to Resistors = 400 ppm				9 Bit ±1/2 Bit Array Error = ±.1% Error Allocated to Resistors = 200 ppm			
V Full-Scale	Resistor No.	Nominal Resistance kΩ	Nominal R/R_{E1} Ratio	Ratio Tolerance at 25°C	T.C. max (-20°C -85°C) of Resistor Ratios ppm/°C	Nominal Resistance kΩ	Nominal R/R_{E1} Ratio	Ratio Tolerance at 25°C	T.C. max (-20°C -85°C) of Resistor Ratios ppm/°C	Nominal Resistance kΩ	Nominal R/R_{E1} Ratio	Ratio Tolerance at 25°C	T.C. max (-20°C -85°C) of Resistor Ratios ppm/°C	Nominal Resistance kΩ	Nominal R/R_{E1} Ratio	Ratio Tolerance at 25°C	T.C. max (-20°C -85°C) of Resistor Ratios ppm/°C
5 V	R_{S1}	1.650	.648	±.50	± 20	1.780	.698	±.50	±5	1.840	.723	±.50	± 2	1.885	.740	±.10	± 2
	R_{S2}	0	----	----	----	0	----	----	----	.068	.0267	±1.0	±20	.068	.0267	±1.0	±20
10 V	R_{S1}	3.300	1.295	±.50	± 20	3.560	1.395	±.50	±5	3.680	1.445	±.50	± 2	3.770	1.480	±.10	± 2
	R_{S2}	0	----	----	----	0	----	----	----	.130	.0510	±1.0	±20	.130	.0510	±1.0	±20

TABLE IC.
R'_S (POT.) RESISTANCE VALUES CORRESPONDING TO IA. AND IB. VALUES

	6 Bit ±1/2 Bit Array Error = ±.8% Error Allocated to Resistors = .16%				7 Bit ±1/2 Bit Array Error = ±.4% Error Allocated to Resistors = .08%				8 Bit ±1/2 Bit Array Error = ±.2% Error Allocated to Resistors = 400 ppm				9 Bit ±1/2 Bit Array Error = ±.1% Error Allocated to Resistors = 200 ppm			
V Full-Scale	Nominal Resistance kΩ	Resistance Tolerance	Resolution Ω	T.C. max ppm/°C	Nominal Resistance kΩ	Resistance Tolerance	Resolution Ω	T.C. max ppm/°C	Nominal Resistance kΩ	Resistance Tolerance	Resolution Ω	T.C. max ppm/°C	Nominal Resistance kΩ	Resistance Tolerance	Resolution Ω	T.C. max ppm/°C
5V	1.000	±5%	1.3	±50	.500	±5%	1.3	±20	200	±5%	.636	±20	100	±5%	.431	±20
10V	1.500	±5%	2.6	±50	1.000	±5%	2.6	±20	500	±5%	1.731	±20	200	±5%	.636	±20

If greater accuracy over a restricted temperature range is required, then each emitter resistor may be individually trimmed. Using the nominal resistor ratios of Table I and allowing for ±0.1% adjustment, the nonlinearity errors due to manufacturing mismatches in the μA722 may be trimmed out at a given temperature. The accuracy of the converter will then be due primarily to the temperature coefficient of the full-scale current, which has the typical characteristics shown in Figure 4.

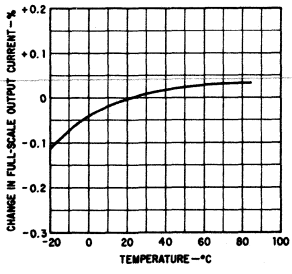


Fig. 4. Typical full-scale output current as a function of ambient temperature.

Basic Digital-to-Voltage Conversion

Normally, a voltage proportional to the input code is required, and an operational amplifier operating in the inverting mode provides the conversion from current to voltage. Figure 5 shows the connection. From basic operational amplifier theory, the output voltage is simply:

$$E_{OUT} = I_S R_S \text{ where } R_S = R_{S1} + R_{S2} + R'_S \qquad (2)$$

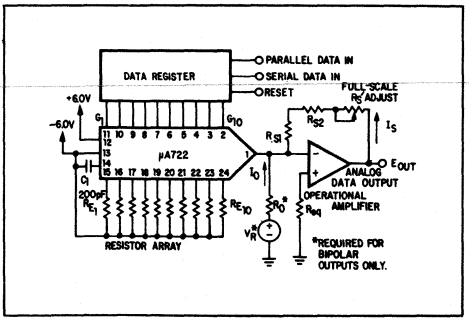


Fig. 5. Typical digital-to-analog converter.

Selection of Summing Resistors

Summing resistor R_S is selected to give the required output voltage swing (normally 5 or 10 volts). Since the full-scale output current of the device may range from 2160 to 3000 μA, provision must be made to trim R_S to obtain the exact output voltage swing. For good ratio tracking with temperature, R_S must track R_{E1} more closely than the capability of most potentiometers. Hence, two fixed series resistors, R_{S1} and R_{S2}, are given in Table I to permit adjustment over the full current range of the μA722 (by choice of shorting R_{S2}), and yet permit use of an available potentiometer with TCR considerably worse than that required of R_S.

From Equations (1) and (2), it can be seen that E_{OUT} depends on the ratio of $\frac{R_S}{R_E}$, and therefore batch fabricated resistors with poor absolute value control may be used for the R_{EJ} and R_S.

PERFORMANCE

Accuracy

The factors defining the accuracy of the μA722 are:

(1) Full-scale current (I_{FS}) drift with temperature

(2) Nonlinearity: worst-case deviation at a given temperature from a straight line drawn through zero and I_{FS} (Code 1,1,1...1) at that temperature,

(3) Error: worst-case deviation from the calibrated straight line (normally at 25°C) value over a specified temperature range.

These concepts are illustrated in Figure 6. The nominal current lines are obtained by joining the zero current and the I_{FS} points. (The nonlinear curve is chosen for illustrative purposes and is not typical for the μA722). Since, by definition, I_{FS} has zero nonlinearity, a given code and its complement have nonlinearities of equal magnitude but opposite sign.

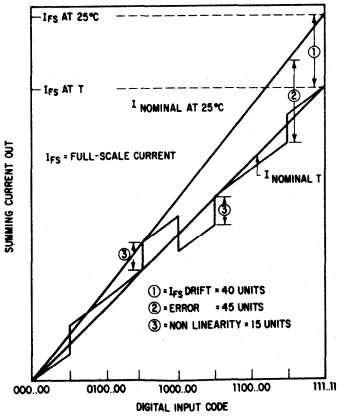


Fig. 6. Hypothetical summing current vs. digital code curve at T to illustrate the concepts of I_{FS} drift, nonlinearity, and error.

The Error is the most significant parameter. For constant temperature operation,

$$\text{ERROR} = \text{NONLINEARITY};$$

for a unit with zero nonlinearity,

$$\text{ERROR} = I_{\text{FS DRIFT}}.$$

For all other cases,

$$I_{\text{FS DRIFT}} \leq \text{ERROR} < I_{\text{FS DRIFT}} + \text{NONLINEARITY}$$

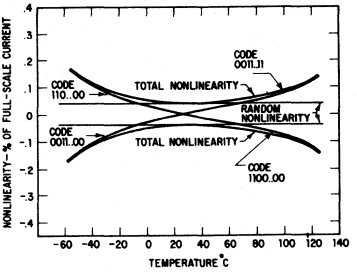
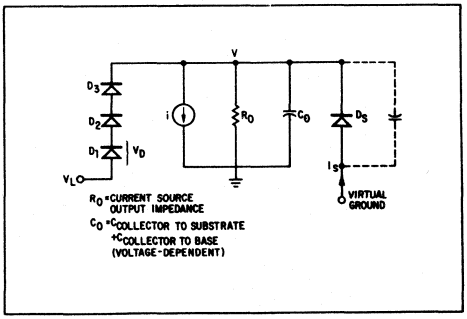


Fig. 7. Nonlinearity vs. temperature: typical graphs.

The nonlinearity of the μA722 is composed of two components, as shown in Figure 7. One is random, and the other is temperature- and code-correlated. At room temperature, the μA722 can have zero nonlinearity through trimming of the individual R_{E_j}. If nominal values of the R_{E_j}'s are used, nonlinearity appearing at 25°C will be random in nature.

Speed

The speed of the μA722 is defined as the settling time after switching to within one-half of the least significant bit value. A simplified diagram of any one of the bit current sources is:



Potential V when V_L is high = $V_{LH} - 3V_D$

when V_L is low = $-V_D$

Therefore, there is a change in V of $V_{LH} - 2V_D$

While this change in V is occurring, both current steering paths are non-conducting. R_o is large, and capacitor C_o provides all the current required by the current source. The time required for this change in voltage is

$$\Delta t \approx \frac{V(\Delta C_o) + C_o(\Delta V)}{i} \approx \frac{C_o(V_{LH} - 2V_D)}{i} - \frac{V(\Delta C_o)}{i} \quad (3)$$

For a constant V_{LH}, switching time is inversely proportional to current; i.e., it will be limited by the least significant bit.

To turn on I_S, V has to change $V_{LH} - 2V_D$; to turn it off, V has to increase approximately 100 mV from $-V_D$. Since normally $V_{LH} - 2V_D > 100$ mV, the turn-on time determines the maximum speed.

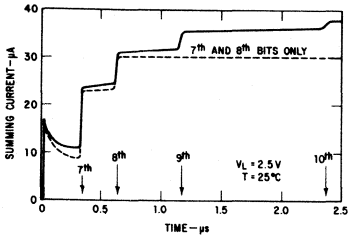


Fig. 8. Turn-on time of 7th, 8th, 9th, and 10th bits.

Figure 8 shows the current waveform obtained after switching bits 7, 8, 9, and 10. The current spike at 30 nsec is due to the capacitive feedthrough from the logic inputs to the summing current terminal. Only a very small fraction of this is feedthrough along D_1, D_2, D_3, and D_S; most of it is due to capacitance associated with the package and external connections. There is a current flow of 11 μA before the 7th bit turns on (<350 nsec). This is due to the voltage changing across the capacitance of D_S as V varies.

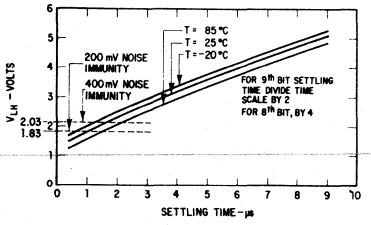


Fig. 9. Settling time - 10th bit.

From equation (3), settling time is proportional to $V_{LH} - 2V_D$; consequently, it will be a strong function of the high logic level and temperature (through V_D). Figure 9 illustrates that with $V_{LH} = 1.90$ V, the μA722 has at least 300 mV noise immunity and at most 1.60 μsec speed for 10 bits, 800 nsec for 9 bits, and 400 nsec for 8 bits.

Switching Thresholds

The high logic threshold is the minimum V_{LH} ($V_{LH\ min}$) necessary to make $I_S = (1/2)\ I_{LSB}$; the low logic threshold is the maximum V_{LL} ($V_{LL\ max}$) necessary to make $I_S = I_{FS} - (1/2)\ I_{LSB}$.

These voltages are limited by the first bit according to the equation:

$$V(T) \simeq 2\,V(T)_{BE} \Big|_{I = 300\ \mu A \pm \frac{kT}{q} \ln X} \quad (4)$$

where $X = 2^N$

N = number of bits used

"+" for $V_{LH\ min}$

"-" for $V_{LL\ max}$

Table II summarizes the results. The low temperature extreme limits $V_{LH\ min}$, while $V_{LL\ max}$ is restricted by the highest temperature.

TABLE II.

	LEAST SIGNIFICANT BIT	SWITCHING THRESHOLD AT -20°C	+25°C	+85°C	ABSOLUTE LIMIT OVER -20°C to +85°C RANGE - VOLTS
$V_{LH min}$	8	1.66	1.45	1.23	1.66
	9	1.64	1.47	1.25	1.64
	10	1.63	1.49	1.27	1.63
$V_{LL max}$	8	1.36	1.17	.89	.89
	9	1.34	1.15	.87	.87
	10	1.33	1.13	.85	.85

GENERAL INTERFACE REQUIREMENTS

Logic Interface

The μA722 is compatible with most types of bipolar digital integrated circuits. The guaranteed μA722 input thresholds of 0.7 V for V_{IL} and 2.1 V for V_{IH}, in conjunction with an extremely high input impedance, allow operation with TTμL, DTμL, LPDTμL, RTμL, LPRTμL, CμL and CTμL families of logic.

Compatible Current Sinking Logic (CCSL) consisting of TTμL, DTμL, LPDTμL, and CCSL Medium Scale Integration Logic have guaranteed worst-case output voltages of $V_{OL} = 0.4$ V, $V_{OH} = 2.5$ V at full fan-out. This allows a μA722 to be driven with no loss of logic fan-out.

Complementary Transistor Logic (CTμL) inverters, buffers, and flip-flops provide typical output voltages of $V_{OL} = -0.5$ V and $V_{OH} = 2.4$ at low fan-outs, adequate for μA722 operation.

Current Sourcing Logic such as RTμL, LPRTμL and CμL have output swings on the order of $V_{OL} = 0.4$ V and $V_{OH} = 1.2$ V when operating at full fan-out. This V_{OH} is unacceptable for driving the μA722; thus, no current sourcing loads may be driven from an output which is driving a μA722 input unless worst-case analysis determines that the μA722 V_{IH} threshold will be met.

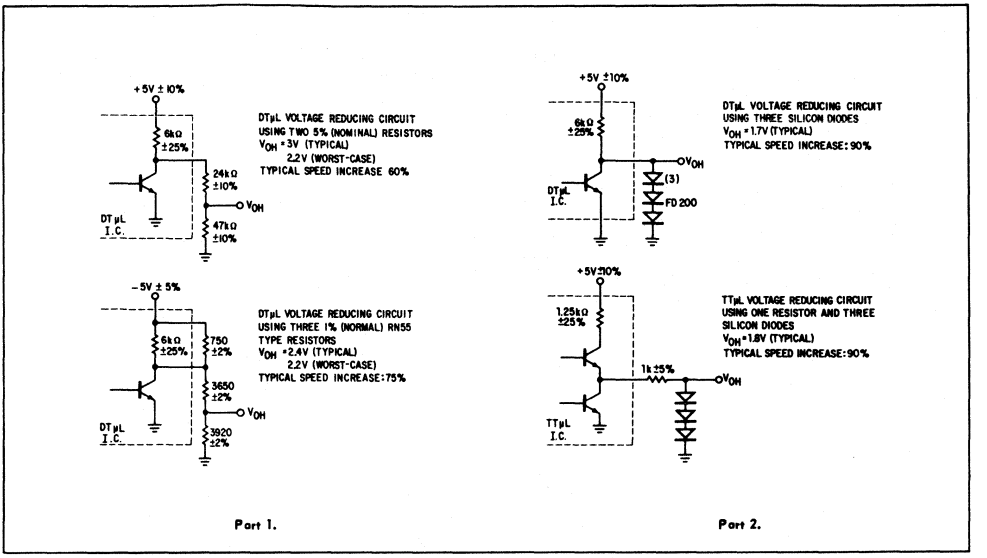


Fig. 10. Representative voltage reducing networks for minimizing μA722 switching time (for least significant bits).

For maximum speed applications, it is desirable to lower the logic level on the least significant bits. In general, the closer the V_{IH} is to the threshold, the faster the μA722 will operate. The V_{IH} must, at the same time, maintain an adequate noise margin with worst-case tolerance of power supplies, temperature, and components. Since the μA722 input threshold is essentially two diode-drops above ground (see Table II for exact value), a technique which will "track" this threshold with temperature will give the fastest operation over a temperature range.

Some representative voltage reducing networks are shown in Figure 10. The diode networks will provide approximately one diode-drop noise immunity. The resistive dividers were calculated for 2.2 V minimum worst-case output.

Current Determining Resistors

Individual current setting resistors are required for each bit used in the μA722, and a matched feedback resistor for current/voltage conversion. Table I listed the recommended resistor values and temperature coefficients. Tolerances were determined by allocating about 20% of the total 1/2 bit error to resistor imperfection. If trimming is to be done, parallel or series potentiometers may be used, but TC mismatch between the primary resistors and the trimpots must be considered. The greater the TC difference, the less the tolerable trim range for a given required accuracy and temperature range.

Since the current through the resistors is constant, wirewound resistors having significant inductance may be used for the current setting resistors with no sacrifice in speed. However, the current/voltage converting feedback resistor, which receives the μA722's switched current steps, must be non-inductive for high speed D/A operation. Thus, for high speed operation, two constraints are placed on the combination of current setting resistors and feedback resistor. First, their TC's must track; second, the feedback resistor must have low inductance. If TC tracking rather than very low TC is relied on to meet accuracy requirements, a third constraint must be considered: the need for a low R_{TH}, or thermal resistance, between the feedback resistor and the others. The reason is that the temperature of the feedback resistor will vary from ambient as the square of I_S, the μA722 summing current, averaged over the feedback resistor's thermal time constant. For a 0 to 5 V encoder, the maximum power dissipated is $(2.5\ mA)^2 \times 2\ k\Omega$, or 12.5 mW. This causes less than 1°C rise in many discrete component resistors, but can be significant for miniature film resistors unless they have low TC.

Power Supplies, Noise, and μA722 Stability

The μA722 has at least 20:1 built-in V^+/V^- power supply rejection* at DC, and even greater rejection can be established at higher frequencies by use of a large stabilization capacitor (say .01 μF). However, high frequency variation of the V^- supply relative to ground will produce AC error current on the summing line via the capacitance between the μA722's substrate and output line. It should be emphasized that such error currents may be innocuous in low speed applications where some form of integration follows D/A conversion. However, for high speed, high accuracy applications, high frequency noise, up to several MHz,

* For the μA722, PSR is defined as % V^+/V^- variation divided by % I_{FS} variation, or vice versa.

must be controlled. High frequency variation of V^+/V^-, and V^- /ground and/ or I_S can result from several causes:

(1) Spurious pickup on supply and ground leads.
(2) Ringing of V^+ and ground leads due to the switching of I_S from V^+ to summing line (or vice-versa).
(3) Ringing due to inadequate stabilization of the μA722's internal regulator.

By applying techniques appropriate to the application, as described in the next several paragraphs, the sources of high frequency error can readily be eliminated or reduced to a level permitting high speed operation of the μA722 within 10 bit ± 1/2 bit accuracy (temperature variation not considered).

Principal Load and Power Supply Configuration

The principal load and power supply configurations for application of the μA722 are expected to be combinations of the following three categories:

(1) μA722 drives either:
  (a) High or low speed inverting op amp (see Fig. 5).
  (b) Resistive load to ground (see Fig. 11).
(2) Available power supplies are either:
  (a) Logic Supply (0 to +6 V) and two analog supplies (0 to +12 V, and 0 to -12 V) or
  (b) Logic supply (0 to +6 V) and a single, floating analog supply (12 V to 18 V)--i.e., the "minimal supply" case.
(3) Length of supply and load leads:
  (a) Short (<3")
  (b) Long (>3").

The transimpedance op amp case is expected to be the principal load case, but the supply configuration depends strongly on the user's system. Generalized AC equivalent circuits for the two load cases are given in Figures 1 and 3 of the Appendix.

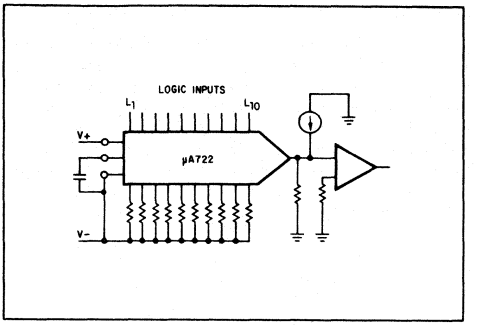
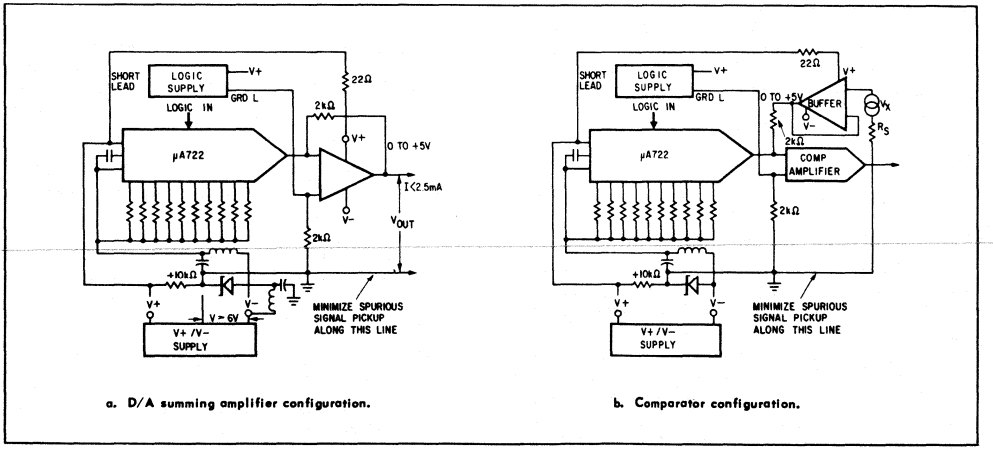


Fig. 11. Connection showing resistive load to ground.

Control of Spurious Pickup

The μA722 must normally function in proximity to a digital system with high noise-pulse levels on the logic supply and ground leads, and via electromagnetic coupling. Additionally, RFI may be present from nearby subsystems. To control the levels of such spurious signals, it is recommended that a combination of the following techniques be considered, depending on noise levels, and economic, miniaturization, and reliability considerations of a specific application:

(1) Minimize the effective length of supply and ground leads by locating a dual regulator adjacent to the μA722.
(2) Maintain analog ground on a bus wire separate from the digital ground (see Fig. 12).
(3) Insert an LC filter into the V^- supply path adjacent to the μA722, with a cutoff frequency <100 kHz.



a. D/A summing amplifier configuration.

b. Comparator configuration.

Fig. 12. Schematics of supply lead problems related to the 2.5 mA step between all "1's" and all "0's" codes. In both cases, (1) use of a common V^+ for μA722 and signal I/O amplifiers is recommended and (2) minimum ground pickup must be maintained between amplifier input reference and external signal ground.

Stabilization and Filtering of the μA722 Internal Regulator

The μA722 internal regulator will normally oscillate unless a capacitor is placed between its stabilization terminal and V^-. As little as 3 pF may stabilize a specific unit (e.g., stray capacitance) but its response to supply transients, such as that resulting from a code change into the μA722, may be underdamped. This is illustrated in Figure 13, where a set of approximate power supply rejection versus frequency curves is given for various values of stabilization capacitance. Normally 1000 pF $\lesssim$ C is recommended. If miniaturization is a problem use C = 200 pF.

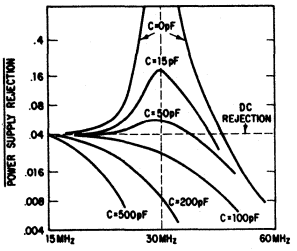


Fig. 13. μA722 power supply response to spurious sinusoidal components between V^+ and V^-, as a function of stabilization capacitance.

Control of Lead Ringing from μA722 Switching

The presence of lead inductance in conjunction with collector-to-substrate capacitances of the μA722 establishes an LC network which can ring when the μA722 switches. The impact of such ringing depends partly on the supply rejection of the μA722, and partly on the integrating properties of the D/A load. The former was seen in the previous paragraph to depend on the value of stabilization capacitance. The problem of reducing the ringing amplitude is analyzed in the Appendix for both resistive and op amp loads, where essentially the following principles are derived:

For the op amp load (see Appendix Fig. 3 & 4 for symbol definitions)

$$V^+(t) - V^-(t) \approx 2.5\ \text{mA}\sqrt{\frac{L}{C_1}}\, e^{-\frac{t}{2R_1C_1}} \operatorname{Sin}\frac{t}{\sqrt{LC_1}} \qquad (5)$$

where $L = L_+ + L_-$.

Both discrete and monolithic high slewing rate op amps have lower high frequency power supply rejection than the μA722, and therefore ringing of the op amp V^+ may have to be reduced despite adequate ringing rejection by the μA722. A convenient and effective damping method is to insert a small resistor (r) in series with the op amp V^+ (see Fig. 12). The damping time constant is then dominated by $\tau = \frac{2L}{r}$ instead of R_1C_1 in Eq. 5, and should be made small enough to assure that the ringing envelope is damped below the necessary error level within the required D/A response time. The maximum value of r is limited by its effect on DC regulation with switching of $0 \leq I_S \leq 2.5$ mA. This effect can be minimized by using a common V^+/V^- supply for both μA722 and transimpedance op amp so that current traversing the μA722 current sources comes either directly from V^+, or from V^+ via the op amp output stage into the μA722 summing line. Experience has shown that for this supply configuration, r = 22Ω is effective for a 10-bit D/A with supply leads up to 3 to 4 feet long.

Recommended Supply and Lead Configurations

Two generic configurations are recommended, one for an op amp sourcing the summing current and the second for a low resistance ($\lesssim$200Ω) source from summing line to ground (as might be used for a current-encoding A/D).

Configuration I is the more important. It is shown schematically in Figure 12. Note that most of the techniques previously discussed in this section are combined in it to give best performance. Some may be dropped for simplicity in specific applications. These techniques are:

(1) Use of an analog ground wire tied to digital ground at only one point, so that no digital signals flow in it.
(2) Minimum line length containing the V^+ current transient by connecting the μA722 directly to V^+, and branch feeding the amplifier with a short lead.
(3) Light loading of the D/A buffer op amp.
(4) LC filtering of V^-.
(5) (r < 50Ω) damping resistor in V^+ line.

In addition, a most important technique, not previously mentioned, is the use of a nearly floating, single analog supply referenced to digital ground by a low-cost zener diode, such as the reverse E-B junction of a transistor. This is made possible by the fact that just 30 μA (about 3 μA per logic input) must be returned to the logic supply from the μA722's V^- current.

For the system already having separate V^+ and V^- supplies, or when high supply levels are needed by the op amp, it is recommended that the above common-supply techniques be retained by use of zener dropping diodes from the op amp supply levels, to supply the μA722 at +6 V.

The recommended configuration is believed to provide the best compromise between cost, complexity, and performance. If performance is the dominant consideration, separate μA723 V+ and V- regulators* are recommended. An example circuit is given in Figure 14.

Configuration II is shown schematically in Figure 15. Since for this case the I_S step switches between two separate leads, V+ and V- ground, it is recommended that:

(1) The V^+/V^- ground/summing-reference lead triangle be composed of physically short leads, and that they be physically close and parallel for inductance cancellation as shown in Figure 15.

(2) The V^+ lead must be physically short to minimize inductance.

(3) A damping RC be connected between V^- and the summing reference (signal ground).

---

* Also see the μA723 Application Note "A Monolithic Voltage Regulator", by D. Lieux.

Values on the order of 50Ω and C $\geq$ 1000 pF should be used, and these components should be checked for fidelity of their characteristics at frequencies up to 30 MHz.

(4) Inductive filtering of V (using the damping RC as an AC shunt load) be used.

(5) (r $<$ 50Ω) damping resistor be placed in V^+ line.

Again, best performance can be achieved with separate V^+ and V^- regulators, but at added cost and component count.

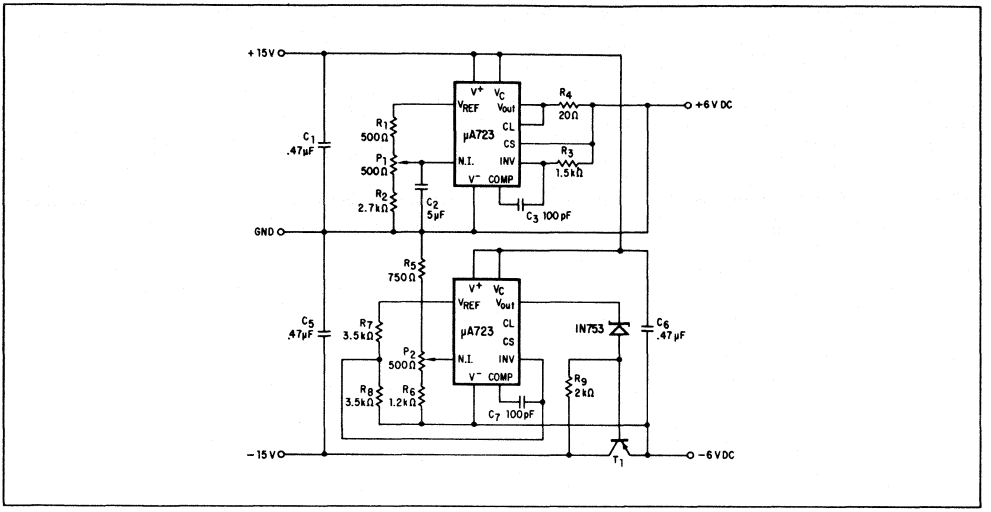


Fig. 14. ±Regulator for best μA722 performance (it is normally unnecessary).

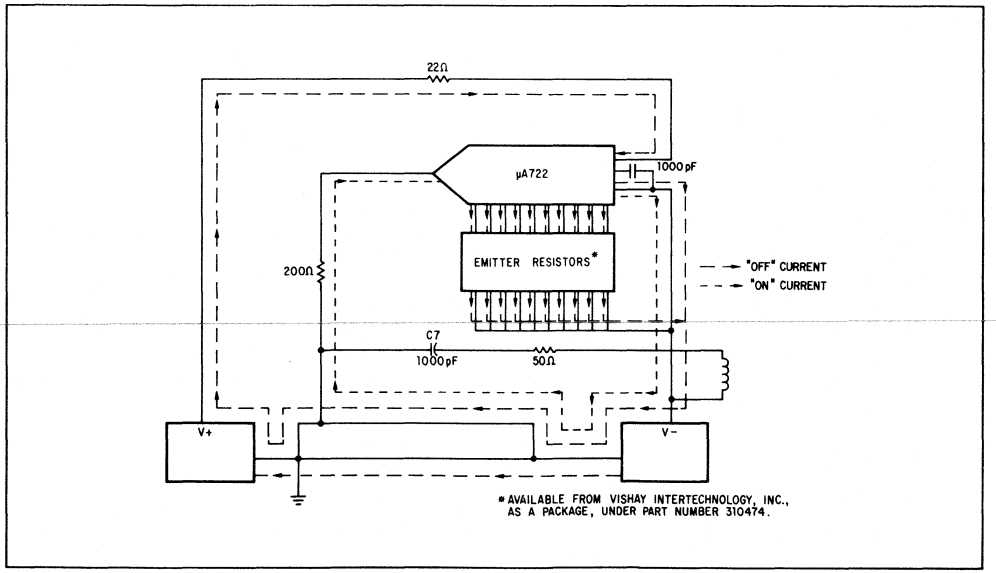


Fig. 15. Recommended ground damping, and filtering configuration for μA722 with grounded resistive source.

Failure Modes

Various types of misuse of the μA722 will result in excess current in a junction or connecting metal, and permanent damage. Supply limiting will save the unit in some cases. The time and current levels necessary for permanent damage are not presently known. Only simple application errors, involving a single type of discrepancy, have been considered. Multiple erroneous connections, except those induced by package symmetry, have been ignored.

A brief description of potential ways to misuse the μA722, and their effects, follows. The symbol "i" in various subscripts refers to the general, i^{th} bit.

Erroneous Insertion of Unit

(1) Package inserted upside down

Pin 12 is interchanged with pin 13; i.e., V^+ interchanged with $V^- \rightarrow 2$ V forward bias on isolation-collector junctions of Q_{1i} and Q_{2i}.

Total current is divided evenly (approximately) among 20 transistors. Therefore, if power supply current is not limited to about 250 mA, failure will occur.

(2) Package rotated 180°

Pin 13 is interchanged with pin 1; i.e., collector bias on D_1 to D_{10} = V^-; substrate is nominally at 0 V via the external summing line resistor, R_S.

Therefore, V forward bias appears on isolation-collector junctions of D_1 to D_{10}, but limited current is available through R_S, and failure will not occur. However, in applications in which the μA722 drives a low resistance to ground, such as a meter movement, the current could reach damage levels.

Exceeding Maximum Logic Levels

(1) $V_{logic} > 6.8$ V for $V^+ = 6$ V

Q_{1i} CB junctions forward-biased -- unlimited current.

(2) $V_{logic} > 8.0$ V for $V^+ > 7.2$ V

EB junctions are broken down, and unlimited current through the Q_{1i}, D_{1i}, Q_{2i}, D_i chain.

Since it is possible that only one or two of the logic drivers exceed the maximum level, current limiting of power supplies will not work.

Shorting Various Combinations of the 24 Leads

(1) Short pin 1 to pin 13; current summing bar to V^-

If any of the logic inputs >2.5 V, then D_i EB junction is broken down, large current flows through the Q_{1i}, D_{1i}, Q_{2i}, D_i chain.

(2) V^+ shorted to ground

V_L forward bias appears at CB junctions of Q_{1i}.

Reversal of Power Connections

(1) Complete reversal is covered under "erroneous insertion (1)".

(2) V^- supply tied to V^+ terminal

Forward-biased Q_{1i} CB junctions into the external logic terminals, and very large currents can flow depending on logic output current capacity.

II. D/A-A/D CONVERSION AND OTHER SUBSYSTEM APPLICATIONS OF THE μA722

DIGITAL-TO-ANALOG CONVERTERS

Low Speed Digital-to-Current Conversion

When a current-operated device such as a strip-chart recorder, meter, or deflection coil is to be driven, no operational amplifier is required. The digital-to-analog meter of Figure 16 illustrates this point. A standard 1 mA meter is driven directly from the μA722. Potentiometer R_P provides a full-scale adjustment by bypassing excess output current. Since analog meters are normally readable to no better than 1%, only a 7-bit input is specified; the unused inputs should be tied to the logic V^+.

The resistor array is made up of 7 resistors: 4 standard value 1% RN55 types, two standard ±5% carbon composition, and one special value .5% unit. The simplicity and small size of the circuit allows the complete digital-to-analog converter to be mounted within, or on the back of, a meter.

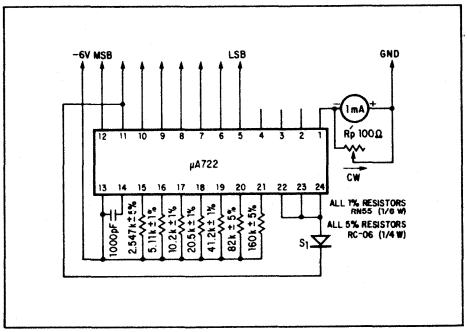


Fig. 16. Digital input meter.

Basic Digital-to-Voltage Conversion with the μA722

If a voltage proportional to the input code is required, an operational amplifier operating in the inverted mode provides the conversion from current to voltage. Figure 5 showed the basic connection.

Operational amplifiers may require a method of nulling out offset currents and voltages, but normally offsets of high quality discrete and IC amplifiers (e.g., μA709) are negligible for 10-bit operation with the μA722.

If the full 10-bit digital input is not required, unused inputs should be tied to the logic power supply.

The μA722 sinks no output current I_S when all digital inputs are high ($\geq$2.5 V), and maximum current when all inputs are low ($\leq$0.5 V). After inversion by the inverting amplifier, this results in a DAC in which all inputs high result in the most negative voltage output; all inputs low, the most positive. For unipolar outputs, the binary inputs should be connected in complemented form to obtain the desired input code to output relationship. The complemented inputs may be easily obtained from a flip-flop holding register by connecting the $\bar{Q}$ outputs to the μA722.

Bipolar Outputs

Since the μA722 acts as a current sink, the operational amplifier output voltage will always be positive or zero. For bipolar or negative voltage outputs, a unity gain inverting amplifier may be switched in, or a positive current I_O may be introduced at the summing point to offset E_{OUT} in the negative direction. The latter case will be described first.

If a highly stable positive voltage V_R is connected through stable resistor R_O, the output voltage is then:

$$E_{OUT} = \left(I_S - \frac{V_R}{R_O}\right) R_S \qquad (6)$$

Since full-scale I_S will vary from nominal, provision must be made to trim I_O a similar amount. By thus biasing the amplifier input so that zero is shifted to half-scale, logic transformation of the input code can give bipolar output (as described later). To eliminate errors due to the operational amplifier input bias currents, both input terminals should "see" equal resistances. The μA722 typically has 1.2 MΩ output impedance; therefore:

$$R_{eq} \cong \frac{R_S R_O}{R_S + R_O} \qquad (7)$$

If no offset resistor (R_O) is required, $R_{eq} = R_S$.

As a result of the current source characteristics of the μA722, the amplifier gain may be assumed equal to unity ($R_{IN} = R_S$) for all practical values of R_S. This has the desirable property of making amplifier frequency compensation independent of output voltage swing.

For bipolar outputs, one of three codes is normally specified. If the DAC is being used with a digital computer, negative numbers will normally be specified in one or two's complement form. For ease of manual inputs, absolute value plus sign may be the most convenient. Table III summarizes these common bipolar codes along with the "natural" μA722 code. In addition, a μA722 code is shown for a resistor array with a modified R_1 resistor. Using this table, proper input connections for these codes are easily obtained.

One's complement input code requires the complementing of all digital inputs except the sign bit, and use of the modified R_1 resistor value. Two's complement code again requires complementing all digital inputs except the sign bit. The standard R_1 value is used.

The procedure for absolute magnitude plus sign code conversion may be seen by inspection of Table III. All inputs but the sign bit must be complemented when the sign bit is low, and transmitted in true form when the sign bit is high. Modified R_1 is used. A typical TTμL implementation of the required logic if shown in Figure 17, but any logic family may be used.

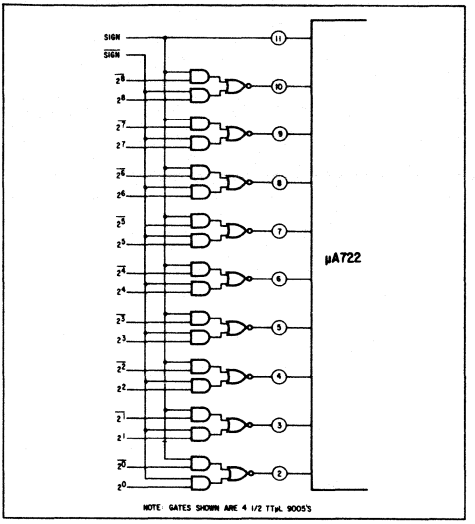


Fig. 17. Absolute magnitude plus sign 10-bit DAC logic.

The modified value of R_1, used for one's complement and absolute magnitude plus sign codes, is required to decrease the current contribution of the sign bit by an amount equal to the least significant bit. In other words, R_1 must be increased so that $I_1 = I_2 + I_3 + \ldots I_n$, where n is the number of bits in the code, thus shifting zero to exactly half-scale of the μA722.

Since the change of R_1 will be small, a simple linear relationship may be assumed between R_1 and I_1 so that:

$$R_{1_{mod}} = \left(\frac{I_1}{I_1 - I_n}\right) R_1 \qquad (8)$$

TABLE III.
SUMMARY OF 10-BIT BINARY BIPOLAR CODES
L = ≤0.5 VOLTS H = ≥2.1 VOLTS

	μA722 DAC BINARY WEIGHTED RESISTOR ARRAY		μA722 DAC MODIFIED R_1		ONE'S COMPLEMENT		TWO'S COMPLEMENT		ABSOLUTE VALUE PLUS SIGN	
	MSB	LSB	MSB	LSB	Sign	LSB	Sign	LSB	Sign	LSB
PLUS FULL-SCALE	LLLLLLLLLL		LLLLLLLLLL		L	HHHHHHHHH	L	HHHHHHHHH	L	HHHHHHHHH
PLUS ONE	LHHHHHHHHL		LHHHHHHHHL		L	LLLLLLLLH	L	LLLLLLLLH	L	LLLLLLLLH
PLUS ZERO	LHHHHHHHHH		LHHHHHHHHH		L	LLLLLLLLL	L	LLLLLLLLL	L	LLLLLLLLL
MINUS ZERO	LHHHHHHHHH		HLLLLLLLLL		H	HHHHHHHHH	L	LLLLLLLLL	H	LLLLLLLLL
MINUS ONE	HLLLLLLLLL		HLLLLLLLLH		H	HHHHHHHHH	H	HHHHHHHHH	H	LLLLLLLLH
MINUS FULL-SCALE	HHHHHHHHHL		HHHHHHHHHH		H	LLLLLLLLL	H	LLLLLLLLH	H	HHHHHHHHH

TABLE IVA.
FIXED RESISTOR VALUES FOR THREE-PLACE BCD RESISTOR ARRAYS

		8 Bit ±1/2 Bit Unit Error Allocated to Resistors = 400 ppm				9 Bit ±1/2 Bit Unit Error Allocated to Resistors = 400 ppm			
Resistor No.	Bit Value	Nominal Resistance Value kΩ	Nominal Resistance Ratio R/R_{E1}	Ratio Tolerance at 25°C %	T.C. max (-20°C -85°C) of resistor ratio ppm/°C	Nominal Resistance Value kΩ	Nominal Resistance Ratio R/R_{E1}	Ratio Tolerance at 25°C %	T.C. max (-20°C -85°C) of resistor ratio ppm/°C
R_{E1}	2.00	2.547	1.000	±10.0*	±20	2.547	1.000	±10.0*	±20
R_{E2}	1.00	5.094	2.000	±.02	± 5	5.094	2.000	±.01	± 2
R_{E3}	.80	6.379	2.504	±.02	± 5	6.379	2.504	±.01	± 2
R_{E4}	.40	12.83	5.036	±.05	±10	12.83	5.036	±.02	± 5
R_{E5}	.20	25.80	10.13	±.10	±20	25.80	10.13	±.05	±10
R_{E6}	.10	51.03	20.03	±.20	±50	51.03	20.03	±.10	±20
R_{E7}	.08	63.36	24.88	±.50	±100	63.36	24.88	±.20	±50
R_{E8}	.04	126.3	49.57	±1.0	±200	126.3	49.57	±.50	±100
R_{E9}	.02	250.1	98.17	±1.0	±200	250.1	98.17	±.50	±100
R_{E10}	.01	495.0	194.3	±2.0	±500	495.0	194.3	±1.0	±200
R_S	5V Full-Scale	1.590	.624	± .50	± 2	1.630	.640	± .10	± 2
R_S	10V Full-Scale	3.180	1.248	± .50	± 2	3.260	1.280	± .10	± 2

* Absolute tolerance on R_{E1}.

TABLE IVB.
R_S' (POT.) VALUES FOR THREE-PLACE BCD RESISTOR ARRAYS

	8 Bit ±1/2 Bit Unit Error Allocated to Resistors = 400 ppm				9 Bit ±1/2 Bit Unit Error Allocated to Resistors = 400 ppm			
V Full-Scale	Nominal Resistance kΩ	Resistance Tolerance	Resolution Ω	T. C. max ppm/°C	Nominal Resistance kΩ	Resistance Tolerance	Resolution Ω	T.C. max ppm/°C
5V	.200	± 5%	.636	± 20	.100	± 5%	.431	± 20
10V	.500	± 5%	1.731	± 20	.200	± 5%	.636	± 20

For example, an 8-bit DAC requiring the modified value would have the following parameters:

$$I_1 = 1280\ \mu A$$

$$I_8 = 10\ \mu A$$

$$R_1 = 2.547\ k\Omega$$

$$R_{1_{mod}} = \left[\frac{1280\ \mu A}{(1280 - 10\ \mu A)}\right] (2.547\text{-}k) = 2.567\ k\Omega$$

The modified R_1 might be implemented simply by adding a 20 ohm resistor in series with R_1.

By using a BCD weighted resistor array (see Table IV), the μA722 may be used to build a 10-bit BCD DAC. The input range will be decimal 000 to 399.

Overall D/A Speed

The delay associated with the conversion of a digital input to a proportional output of specified voltage is a function of the individual speeds of the logic circuit, the μA722, and the operational amplifier.

In general, digital logic speeds are more than an order of magnitude faster than linear circuits, and their delays may be neglected. The speed of the μA722 is dependent on the accuracy required. For example, typical speeds are 0.6 μsec for an 8-bit conversion, 2.5 μsec for 10-bit. These speeds are for logic inputs of 0.5 and 2.3 volts. Where high μA722 speeds are required, voltage reducing networks such as described in the Logic Interface sub-section should be used on the least significant bits.

Overall D/A Accuracy

The overall accuracy of a linear device is a function of many variables; for a digital-to-analog converter, these include accuracy and temperature dependence of the resistor array, μA722, operational amplifier, feedback resistor, power supplies, and, if used, offset reference voltage and resistor. If high quality components are used, the accuracy limiting element will usually be the temperature stability of the μA722.

With temperature control such as supplied by a small oven, and individual trimming of array resistors, very accurate operation may be obtained. The only inaccuracy for this case is noise, which limits operation to about 13 bits at 1 megabit, and about 15 bits at 63 kilobits.

Generally, the overall DAC conversion rate will be determined by the operational amplifier. While small output excursions may take place rapidly, worst-case output swings of 5, 10 or 20 volts normally account for the largest delays. This is due to the early roll-off in open loop gain of the operational amplifier, caused by compensation networks. For example, the typical slew rate of a μA709 with unity closed loop gain and recommended compensation is 0.3 volts/μsec.

High slewing rate operational amplifiers (≈100V/μsec) are available from a number of discrete module manufacturers. By actual test, it was found that these commonly have ringing problems when driven by the μA722 and required to settle to less than ±1/2 bit in 10 bits. The trouble seems to be a combination of power supply ringing and inadequate rejection of the high ringing frequency--typically 3 MHz. Surprisingly, the criterion of settling to D/A accuracy often placed amplifiers with lower slewing rates at higher position. In fact an experimental integrated operational amplifier with rated slewing rate of 20 V/μsec outperformed all discrete operational amplifiers tested. Figure 18 illustrates this. Note that the 8th, 9th and 10th bits are shown switching in practically ideal manner, and that (0.1% = 1 cm) no appreciable ringing is observed. The trace width is due to probe noise.

Figure 18 confirms that speeds of .8 μsec, 1.6 μsec and 3.2 μsec are readily achieved for 8, 9 and 10 bits respectively, without logic dividers.

Some Actual Designs

A moderate speed 10-bit binary, unipolar, serial or parallel input DAC is shown in Figure 19.

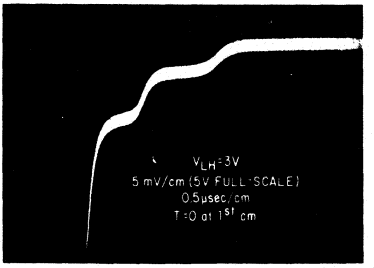


Fig. 18a. μA722/experimental op amp switching ON, as it should with typical logic voltage on least significant bits. Note complete absence of ringing.

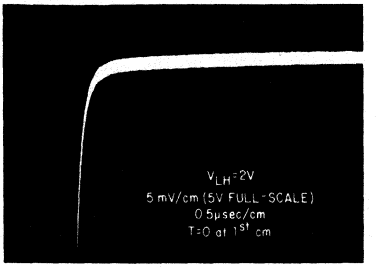


Fig. 18b. μA722/experimental op amp switching ON within .05% in 1 usec with low V_{LH}. Note complete absence of ringing.

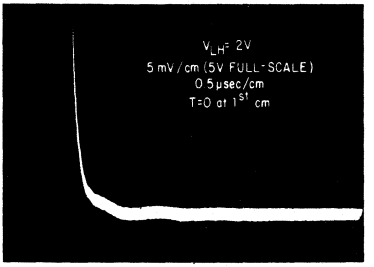


Fig. 18c. μA722/experimental op amp switching OFF within .05% in 1 μsec.

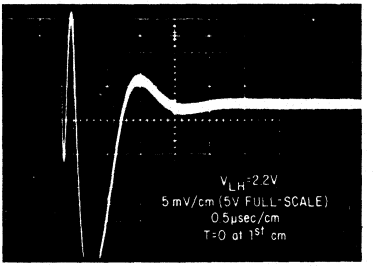


Fig. 18d. μA722 driving a well-known discrete 100 V/μsec op amp. It settles within .05% in 2 μsec.

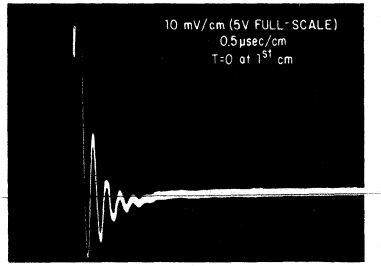


Fig. 18e. A bad example of μA722/experimental op amp ringing on turn off due to capacitive loading (mainly from the scope probe with inadequate op amp compensation). Note that it still settles within .05% in 1.5 μsec.

Fig. 18. Photographs of D/A response using μA722 and an experimental monolithic op amp.

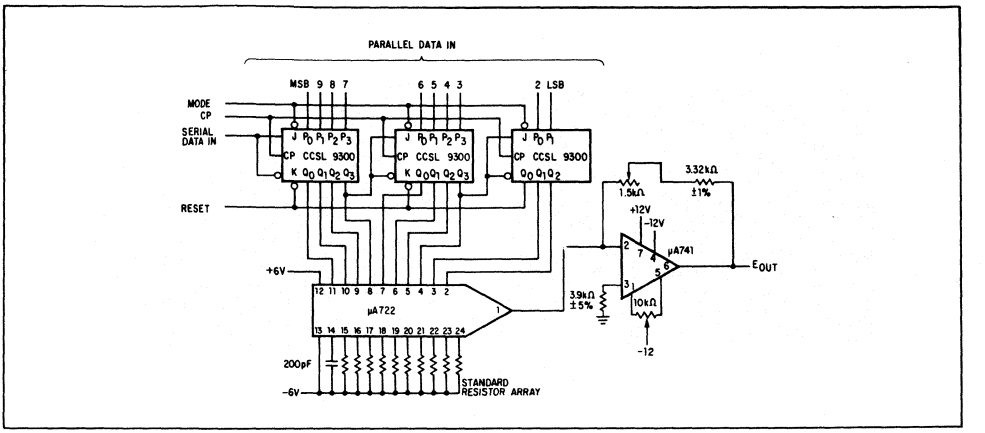


Fig. 19. 10-bit digital-to-analog converter with parallel or serial input.

A holding register of three CCSL 9300 4-bit shift registers provides either parallel input (mode input high) or serial input (mode input low). Both parallel and serial entry are synchronous with the clock.* A parallel asynchronous reset line is provided The 9300 shift register drives a μA722 and a standard value resistor array.

A μA741 integrated circuit operational amplifier is used. For a 0 to +10 V output swing,

$$R_S = \frac{E_O}{I_S} = \frac{10\ V}{2.56\ mA} = 3.91\ k\Omega \qquad (9)$$

Since I_S may vary from nominal, a potentiometer having a range of ±5.5% must be used in series with a fixed resistor to obtain R_S. The nearest standard value is 500 ohms; therefore:

$$R_{S_{FIXED}} = 3910 - 250 = 3660\ \Omega$$

While only ±1% tolerance is required on this resistor, temperature stability must be good. A ±1 PPM/°C temperature coefficient was selected.

Measured performance was 26 μsec transition time to 1/2 LSB (5 mV), .01% linearity, and .25% accuracy over the -20 to +85°C range.

A fast 8-bit DAC is shown in Figure 20. The input code is one's complement provided in parallel, and stored in four TTμL 9020 dual flip-flops. The inputs to the μA722 are taken from the Q output of the sign flip-flop and the $\overline{Q}$ outputs of the other seven outputs to obtain the one's complement code. Voltage-dropping networks are used on the last three stages to increase μA722 speed. The unused inputs are returned to +5 volts.

The resistor array uses a modified value R_1 required for the one's complement code. Since the output is to be ±5 volts, R_S is chosen for a 10-volt swing while the offset resistor R_0 is chosen to offset the output 5 volts negative. While R_1 and R_0 need only have 1% initial tolerance because of the series potentiometers, they must have good temperature stability. A TC of 1 PPM/°C was specified. A high speed discrete component operational amplifier was used to obtain fast transition times from ±5 volts with output currents up to 18 mA. Measured performance of the complete DAC was a maximum delay time of 2.8 μsec to ±1/2 LSB (~20 mV) at room temperature into a 40 pF load.

ANALOG-TO-DIGITAL CONVERTERS

The μA722 is basically intended for D/A conversion, but it can be used in all forms of A/D conversion as a comparison signal generator. And since A/D converters generally require higher bit rates, the speed of the μA722 is especially useful in such applications. The principal types of D/A feedback encoders are:

(1) Staircase counter A/D converter
(2) Up-down counter A/D converter
(3) Successive approximation A/D converter

The first two trade high A/D speed for digital simplicity. The latter has the highest random-sample encoding speed, and is presently the most popular configuration because with multiplexing it offers the greatest conversion power per dollar or pound weight.

A staircase converter using a μA722 can encode to 8 bits in about .25 msec. The up-down counter converter, using the μA722 and T^2L logic, can easily follow a single signal up to 10 kHz. These techniques may prove the most efficient for local conversion systems, because the counters take less digital circuitry. However, because of its popularity, the successive approximation (SA) configuration was selected for an example application of the μA722.

* If a stable D.C. output is required during serial mode input time, a holding register using either 9300's or 9308's should be used.

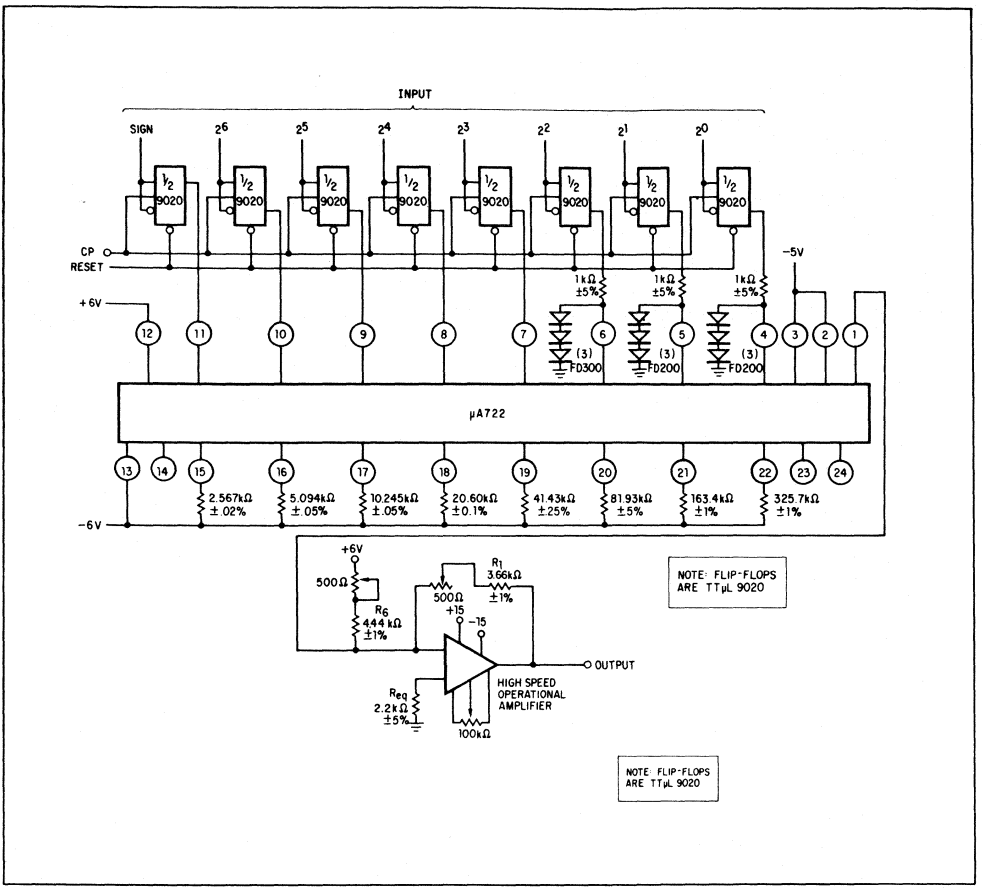


Fig. 20. Fast, 8-bit DAC with one's complement input code. Output is ±5 V, @ 18 mA.

Successive Approximation Converter

An actual μA722 SA converter was constructed and tested. The block diagram is shown in Figure 21. It includes a μA722 D/A converter, a digital programmer and data register block, a comparator, and an input buffer amplifier.

The SA technique is well-known, but for completeness is described for the scheme in Figure 21 as follows:

(1) A voltage to be encoded, V_X, has subtracted from it a voltage $I_S R_S$ via the summing line resistor R_S;

(2) $V_X - I_S R_S$ appearing at the comparator input is compared with 0 V (gnd) by the comparator;

(3) The digital block successively tries μA722 bit currents (I_{Si}) starting with the most significant, or largest I_{Si}, and retaining only those bit currents which do not cause the total I_S to pull the comparator input below zero;

(4) With convergent, arabic codes, such as binary and BCD, the sum of the retained bit currents must approach the condition $I_S R_S = V_X$ within the magnitude of $I_{SLSB} R_S$. Thus with each trial, the I_S "successively approximates" $I_X = V_X/R_S$ closer and closer, and at balance, equals it.

Each block and its interface considerations are discussed in the following paragraphs. Since the μA722 D/A conversion technique has been presented previously, only the comparator, buffer, and digital block are treated.

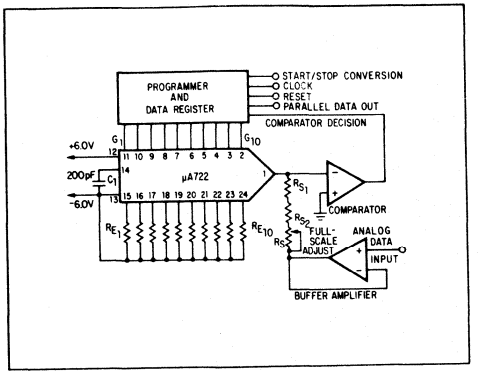


Fig. 21. μA722 successive approximation analog-to-digital converter.

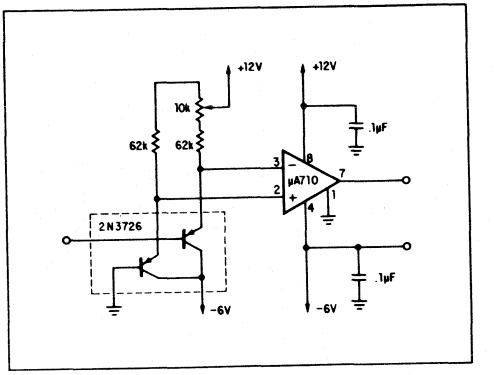


Fig. 22. A/D comparator circuit.

Input Buffer Amplifier

A unity-gain buffer amplifier is often necessary to remove any effects of input voltage source impedance on the converter accuracy, and is required for source impedances above one ohm when 10-bit converter accuracy is targeted. Obviously its output impedance must be under one ohm. Its speed to settle to within the least significant bit (LSB) should be about one bit period, if it is not to reduce overall conversion rate significantly. A developmental high speed IC operational amplifier capable of 1 μsec performance was used in the model, and discrete amplifiers of similar performance are available.

Comparator

The comparison amplifier must have three characteristics:

(1) Be able to resolve the lowest input voltage change $I_{SLSB}R_S$. For 10-bit accuracy and a 5-volt reference, this is .05% of 5 V, or 2.5 mV.

(2) Draw very low current from the μA722 summing line. For 10 bits, I_{SLSB} = 2.5 μA, and therefore the comparator bias offset current should be under 500 nA at minimum temperature.

(3) Switch in a time which is short compared to the μA722 switching time.

The μA710 can handle (1) and (3), but its input bias current is too high to satisfy (2) without a preamp. A single differential stage preamp using the 2N3726 differential pair (Fig. 22) switches in less than 300 nsec. The μA727 can be used if 1 μsec switching is adequate.

Digital Programmer and Data Register

This section provides all the necessary digital sequencing, timing and storage to perform the SA control function described earlier. The logic selected for this example was TTμL to gain the advantage of the complexity available within this family. In practice, any digital integrated family is acceptable since the switching time of the μA722 is much slower than all common bipolar integrated logic families.

Sequential control of the bit trials can be done in a number of ways, but shifting a single "1" through a 10-bit program register was selected. A 10-bit data register for storing the answer is obviously required. These two registers account for the majority of the essential digital circuits. The remaining circuits provide the following:

(1) Flip-flop to store the comparator output.

(2) Timing, shaping, and delays to assure comparator settling before a decision, and to avoid race problems.

(3) Manual start or continuous conversion control (this would be supplied externally in an actual system application).

Complete Circuit

Figure 23 shows the complete SA A/D circuit, using a μA741 as the unity gain buffer amplifier. For higher speed inputs, a higher speed op amp should be used.

The total integrated circuits used are as follows:

PART NUMBER	QUANTITY
μA722	1
μA741	1
μA710	1
TTμL9001	2
TTμL9002	7
TTμL9009	1
TTμL9020	6
TTμL9300	2
	21 for 10 bits

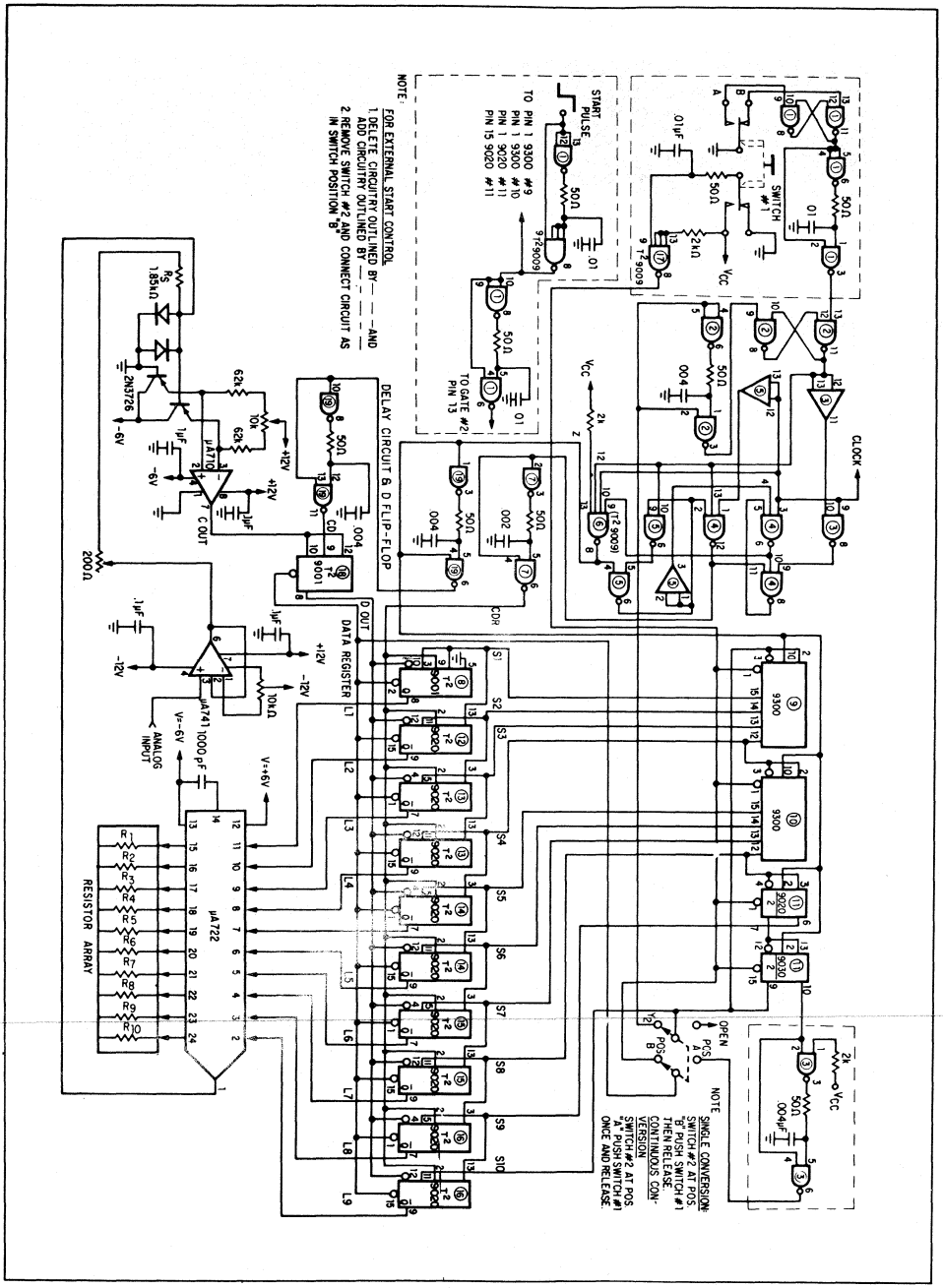


Fig. 23. Complete successive approximation A/D converter circuit schematic.

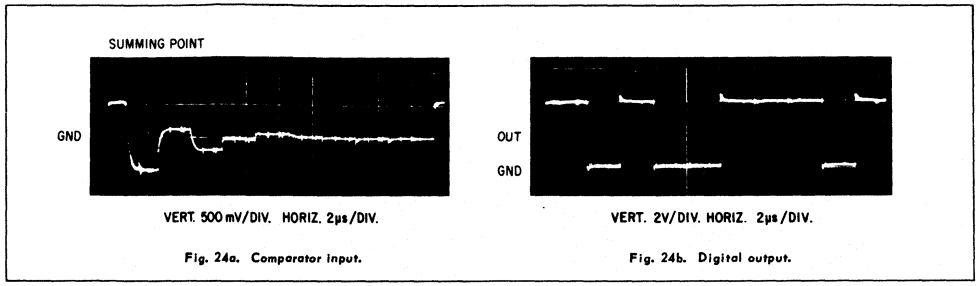


Fig. 24a. Comparator input.

Fig. 24b. Digital output.

Fig. 24.

Performance

The system described is capable of conversion to 10-bit accuracy in 20μs, which is representative of the limitation imposed by the switching time of the least significant bits of the μA722.

For 8-bit accuracy, the clock rate was increased such that the total conversion time was less than 10μs. Applying the recommended temperature coefficient considerations on the comparison amplifier, buffer amplifier, and μA722 resistor array, 8-bit accuracy was readily held from 0 to +55°C.

Figures 24a and 24b show representative 2μs/bit waveforms for the ladder summation point and the digital output, respectively, for the 10-bit SA A/D converter using the μA722.

OTHER SUBSYSTEM APPLICATIONS OF THE μA722

A/D Converter: Extended Resolution and Accuracy

Resolution may be extended beyond 10 bits by cascading A/D converters. With reference to Figure 25, the operational amplifier multiplies the residual error voltage V_S to a level compatible with the second converter $I_S R_S$ full-scale. Tying the stabilization terminals in common will insure a nearly equal operating bias

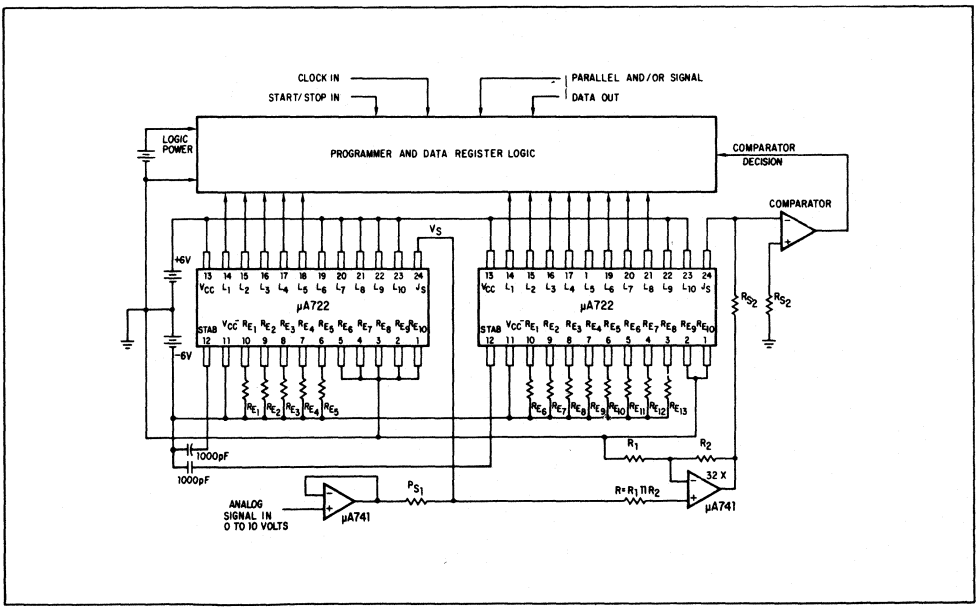


Fig. 25. High resolution analog-to-digital converter.

on each converter. The resolution of the system is limited by the system noise, with 13 to 15 bits being the maximum. This configuration is slower than a single - μA722 converter because of the slewing time required for the 32X amplifier.

A trade-off exists between the speed and accuracy acheivable with the μA722 through the relation between current noise and sampling interval. The accuracy improvement is inversely proportional to the square root of the sampling interval, or bit time. An improvement of one bit is possible at 250 k bits, and 2 bits at 63 k bits. For this reason, the range of accuracy extends from 13 bits at one megabit to 15 bits at 63 k bits.

Accuracy equal to the resolution is attainable only by temperature control. Miniature ovens built by crystal oven manufacturers can hold temperature to ±2°C over the industrial range of 0°C to 70°C, and thus maintain fidelity to the original resistor settings within ±0.01%. At temperatures in the upper military range, leakage current limits accuracy despite thermal control.

Higher Speed D/A

The μA722 can switch its 5th bit in 500 nsec to .05% accuracy. Therefore, two units driving separate operational amplifiers can be summed at 32:1 ratio by a third operational amplifier to provide reliable 10-bit operation at 500 nsec. This is shown schematically in Figure 26.

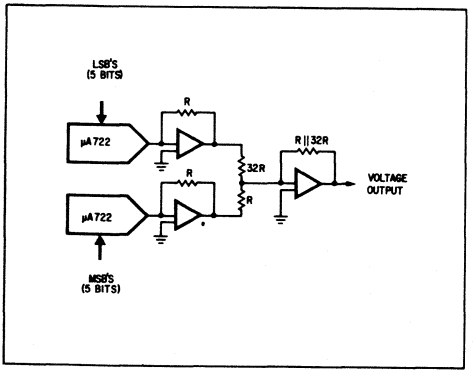


Fig. 26. High speed 10-bit D/A by 5-bit paralleling of μA722.

Function Generation

Numerous functions can easily be generated by setting the individual bit currents of the μA722 to match the desired function with the bits actuated sequentially. This simplifies the digital generator. Two or more converters operated in this manner may be paralleled for greater resolution. Of course, with the standard D/A configuration, any function can be generated digitally with high resolution. But the digital generator may be considerably more complex. In either case, the output is converted to a voltage by a feedback amplifier, and may be smoothed by use of a parallel feedback capacitor.

Logarithmic D/A Converter

The use of a transistor in the feedback loop in the standard DAC allows the formation of the natural logarithm of the digital input value (except 0 value). This is illustrated in Figure 27.* The $V_{BE} = \frac{kT}{q} \ln \frac{I_S}{I_O(T)}$ characteristic of the feedback transistor holds with excellent precision over the μA722 current range. The use of a μA726 temperature controlled pair minimizes temperature variation, balances out I_O, and permits setting the logarithmic base current with R_O. Nominally the base current would be 2.5 μA, i.e., the least significant bit current. Amplification could be set so that the output voltage would increase 1 V for each doubling of the μA722 current. For example, the output voltage would then range from 0 V for 2.5 μA to 9 V for the full-scale current of 1.2775 mA.

$$\left[(2^9 - 1) \cdot 2.5\ \mu A = 1.2775\ mA\right].$$

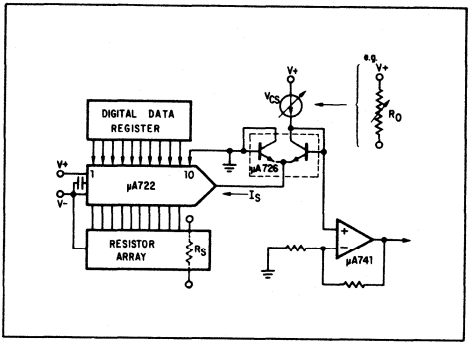


Fig. 27. 9-bit logarithmic D/A converter. Variable current source (VCS) should be adjusted for $E_O = 0$ with $I_S = 5$ μA. External resistor R_{10} should be equal to R_9. For greatest thermal accuracy, R_S should be used to control the VCS.

D/A Multiplier

Hybrid multiplication or division can be accomplished at high speed with the μA722 in conjunction with a stable differential pair such as the μA726 (Fig. 28). It is easily shown for the pair that:

$$\Delta I_c = \frac{q}{2kT} I_s \Delta V_{BE} \quad (10)$$

or

$$\Delta E_{OUT} = K_1 I_s \Delta V_{BE} \quad (11)$$

but

$$I_s = E_{XD} \text{ and } \Delta V_{BE} = E_{XA} \quad (12)$$

$$E_{OUT} = K_2 E_{XD} E_{XA} \quad (13)$$

Thus the analog output is proportional to the product of the digital variable E_{XD} and the analog variable E_{XA}. Note that E_{XA} must be small to satisfy the differential equation above.

* For a more complete circuit, consult the Fairchild LIC Applications Handbook, pp. 150-152.

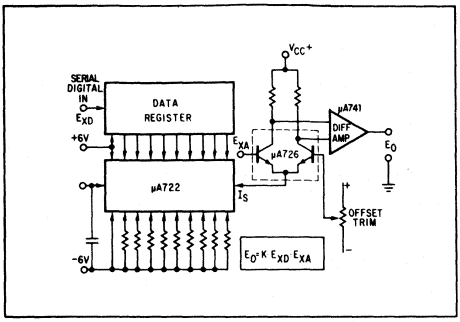


Fig. 28. Digital-to-analog multiplier.

Divider Circuit

The divider circuit, shown in Figure 29, makes use of the differential pair for multiplication. The output is fed back and multiplied with one of the data signals, E_X. This E_X is balanced with the second data signal, E_Y, by equating currents through operational amplifier action until

$$\frac{K_1 E_X E_O}{R_1} = \frac{E_Y}{R_2} \tag{14}$$

or

$$E_O = K_2 \frac{E_Y}{E_X} \tag{15}$$

E_Y may be a direct analog signal or one that is synthesized by D/A conversion.

III. SYSTEM APPLICATIONS OF μA722 SUBSYSTEMS

Major areas of application for D/A and A/D converters and other subsystems described in the previous section occur in both digital and hybrid computer systems. This section briefly outlines the utility of the μA722 in computer systems.

USES OF D/A AND A/D CONVERTERS FOR DIGITAL COMPUTER SYSTEMS

Introduction

A/D and D/A conversion requirements for analog equipment interfacing with digital computers vary greatly in speed and accuracy. Traditionally, higher word speed and accuracy are demanded of converters which measure analog signals (i.e., data acquisition ADCs) than are demanded of D/A converters for driving analog displays and controls. This is because:

(1) High speed transient phenomena may have to be measured in real time (whereas they can be displayed in post time).

(2) Multiple measurements are multiplexed for encoding by a single ADC, whereas DACs commonly are used singularly (for DC response, and because economics permit).

(3) A/D measurement range is often intentionally employed wastefully for greater input flexibility, whereas analog output range tends to be standardized.

(4) Analog displays are limited in accuracy by the resolving power of the analog display devices, and limited in speed by the writing response of the display device or by the flicker response of the eye.

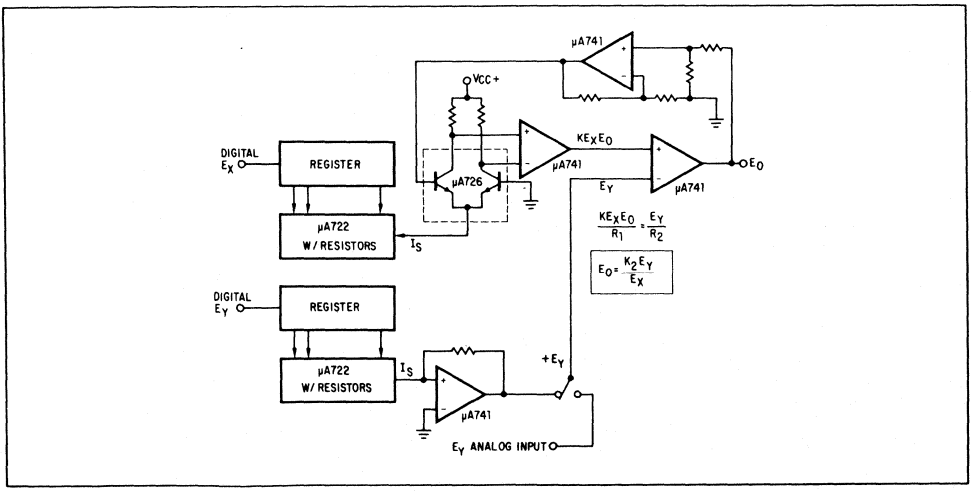


Fig. 29. Divider circuit.

Also, ADCs must operate at higher bit rates because they must operate bit-sequentially, whereas DACs can operate bit-parallel.

The purpose of this section is to relate the applicability of the μA722 on computer peripherals and computerized data acquisition systems.

Data Acquisition and I/O Requirements

The measurement and conversion of analog phenomena to digital quantities is often referred to as "data acquisition". For the purpose of entry into digital computers, a distinction must be made between real time and post time data acquisition. In real time acquisition, the speed of conversion must not be greater than the computer's input speed. In some cases, the instantaneous data rate may be faster than the computer I/O can accept, and the data must be buffered by a high-speed storage medium such as analog tape or peripheral core memory.

Storage and I/O Considerations

Typically, the data rate from high-accuracy ground data acquisition systems is less than 500 k bits/sec. If a buffer composes two words of data per computer word, this can be reduced to 50 k words/sec, which is within the capability of most computer multiplexers. Thus, the computer I/O can handle the data rates of acquisition systems, but storage capacity can be a problem. If greater than one second of data is to be stored at the above rate in core, the cost would be considered prohibitive---20,000 words of memory. Therefore, tape storage is commonly used.

The techniques which must be used for tape storage become more expensive and difficult as the data rate exceeds one megabit. At 1000 bits per inch and 150 inches per second, eight channels are necessary, including a clock, and a packing limitation begins to be reached because of the compromise which skew control demands between channel packing density and number of channels across a tape. Discs are faster than tape, but have less capacity.

For the above reasons, data acquisition rates above one megabit/sec are exceptional, and most requirements are within the nominal 1 megabit/sec capability of μA722 converters.

Data Scaling and Offset by Hybrid Techniques

Digital data measurement systems often require scaling and offset operations upon the samples. This can usually be performed in post time by the digital computer, but often taxes the operation rate of the computer for systems requiring real time usage of the data. In such cases, the D/A multiplying scheme described earlier can be used prior to A/D conversion to perform scaling, and a DAC - operational amplifier algebraic summer can be used to perform offset. This is shown in Figure 30, where the offset and the scaling numbers are derived from a digital table stored in the computer and brought out in blocks to a buffer. Scaling and offset can be performed in about two microseconds, one microsecond for DAC settling time and one microsecond for the arithmetic functions. Also, when necessary, high-speed division such as the ratio of two measurements can be performed by either of the two methods described earlier.

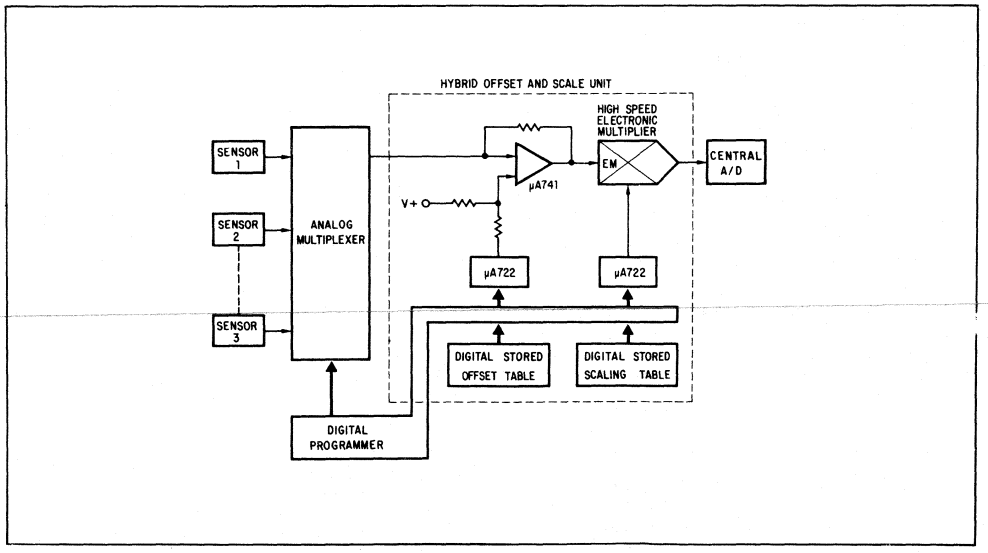


Fig. 30. Illustrative use of hybrid offset and scale computer (to reduce loading of the GP computer).

Local A/D Conversion

With the advent of miniature low-cost A/D conversion made possible by IC's, many systems designers are considering schemes involving local A/D conversion close to the signal generators and sensors. A major objective in such schemes is to reduce the staggering amount of cabling associated with high-accuracy measuring systems. Additional benefits are the increased reliability and simplified maintenance and check-out which result from avoiding dependence on a single A/D converter, as in conventional analog multiplexer approaches. Early applications of this technique are beginning to be seen in military aircraft data monitor systems. These systems detect incipient failure patterns by monitoring many data sources throughout the airplane and operating on the digitized readings with detection algorithms. Eventually, real time closure of the loop will provide protection against dangerous maneuvers with respect to the aircraft structure and stability, or dangerous conditions such as equipment burnout, overheating, overstressing, etc. As shown in Figure 31, a common set of output lines can be shared by all ADCs. Time multiplexing is accomplished by digital code selection as shown.

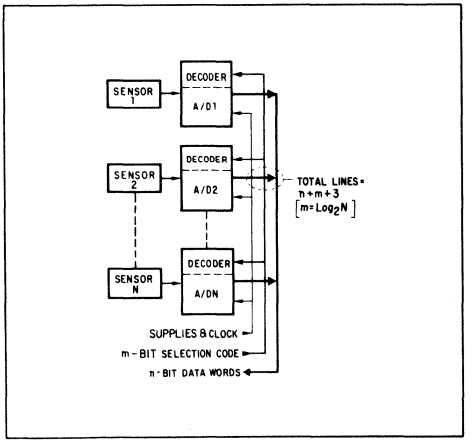


Fig. 31. Local ADC data acquisition system for cable reduction, reliability enhancement.

When cable reduction and economy are both paramount criteria, a compromise hybrid approach in which closely located sensor "clusters" are analog multiplexed into a local converter may be preferable. The speed of the μA722 readily permits handling clusters of 10 or more sensors.

Displays

The availability of low-cost integrated circuit D/A converters is expected to have important benefits in a number of areas in which analog displays are driven by digital computers. Although analog displays are less accurate than the digital type, they can be read and comprehended much faster in cases where high accuracy is unnecessary. Even in cases where high accuracy is necessary, the deviation from the expected value can be displayed in an analog manner with superior human intelligibility. This is of particular importance to special-purpose operational systems employing digital computers, such as those used in aircraft and some ground control stations in which an operator must react quickly. Analog displays are also of great use to those data analysts editing digital data originally of an analog nature, such as in telemetry or picture transmission.

A major area of application is curve plotters such as strip-chart recorders and X-Y recorders or plotters. Here, an interesting competition exists between two techniques: (1) the stepping motor drive, and (2) the DAC-driven servo positioner. Lower cost DACs may have a major effect on the economic balance between these two techniques. The servo positioner is faster and is the sole method when higher speed plotting is required.

Low-cost DAC availability could trigger the abundant use of simple galvanometer needle meters. This is an application which, in the past, has been prohibitive in cost.

DACs are commonly used in the driving of cathode ray tube displays. Examples are light pen design consoles and computer-driven overlay displays for radar target tracking. These are driven by digitally generated sweeps for either X-Y positioning or symbol generation, or both. The speed requirement on the DACs for this type of application varies with the specific design and the time allocated for regeneration of the overlay display. Generally, one microsecond per sample is sufficient for a change in the X-Y coordinates as the speed limitation is primarily in the sweep circuits of the CRT. Other salient considerations in DAC-controlled CRT beam positioners are the high voltage and high current drive requirements. By the transimpedance op amp technique, the μA722 can readily drive special discrete component operational amplifiers intended for such service.

High Speed Analog Storage

The digital computer is capable of spewing out a sequential data list faster than high-speed mass storage media such as tape machines or discs can handle it. In such cases, high-speed D/A conversion can be performed and samples stored in analog fashion. (This obviously is applicable only to data which represents analog samples and whose accuracy is not critical, since good high-capacity analog storage media are limited to deposited magnetics, with attendant poor dynamic range and accuracy). For rates higher than 1 megabit, use of the first 5 bits can push the μA722 as high as 2 to 3 megawords/sec.

USES OF D/A AND A/D CONVERTERS FOR HYBRID COMPUTERS

Introduction

The new generation of A/D and D/A building blocks is expected to have a special impact on the economics of hybrid computers, especially with respect to the digital control of quasi-fixed or fixed analog parameters (viz., potentiometer settings and initial conditions). The three major areas of usage for analog-to-digital and digital-to-analog conversion in hybrid computers are: (1) D/A cross-conversion, (2) condition setting, and (3) high-speed arithmetic and function generation.

Cross Conversion

General purpose hybrid computers demand that errors from individual contributing sources be on the order of 0.01% so that overall error for a computation does not rise above 0.1%; therefore, conversion should be targeted for 13 or 14 bits. This is within the accuracy of the dual μA722 converters. Normally, the DAC's speed will not be taxed, as all bits are converted in parallel. The speed requirement on A/D conversion can be difficult if multiplexers are used to sample many points in the analog portion of the system, or if the digital computer is especially fast in accepting data (e.g., through the use of multi-processors). A microsecond per bit is more than fast enough for A/D conversion if a single analog point is being converted in the analog portion of the hybrid system, because the analog portion will not accurately handle signals above 10 to 100 Hz.

Condition Setting

Whereas the use of A/D and D/A conversion is traditional in hybrid computers, separate digital storage of fixed analog parameters such as initial conditions and gain settings has not been common because of the expense. With the reduced costs made possible by ICs, each initial condition voltage can be injected by a separate DAC whose register digitally stores the setting. Similarly, amplifier gains can be adjusted and held by the DACs through the use of a circuit similar to that shown in Figure 28 for the analog multiplier. Even amplifier drift and offset can be removed by automated DAC zero-setting before each run.

Two interesting economic trade-offs will occur: (1) between (a) the use of higher priced, accurate DACs for initial condition setting as opposed to (b) the use of lower priced, inaccurate (but high resolution) DACs which are sequentially set by comparison against a high-accuracy reference; and (2) between (a) higher priced, low offset amplifiers, and (b) cruder, D/A-zeroed units.

High Speed Arithmetic and Mathematical Function Generation

The last advantageous application of the new low-cost, high-speed bipolar A/D and D/A integrated circuits is in the performance of high-speed hybrid arithmetic. Always available in a hybrid computer is the capability of digitally performing mathematical functions of all kinds. However, some arithmetic functions such as division take considerable time in a digital computer, from 22 μsec to perhaps as long as 100 μsec. By the use of operational amplifiers and D/A current sources in conjunction with the multiplier circuit scheme described previously, it is possible to perform the functions of multiplication and division in from two to ten microseconds, and to accuracies in the range of 0.01% to 0.1%.

Typically, for multiplication, a microsecond is required for the D/A conversion and another microsecond for the analog signal multiplication. For division, if performed in the analog manner shown in Figure 29, a longer time is required because of the need for frequency compensation. If a digital successive approximation scheme is employed, the time is equivalent to A/D conversion, that is, about one microsecond per bit.

CONCLUSIONS

The μA722 monolithic integrated circuit, in conjunction with other IC (or discrete) amplifiers, is capable of conversion at one microsecond per bit with accuracies approaching the best performing discrete component versions (13 to 15 bits). Also, very high speed conversion is possible by paralleling.

The D/A current source technique employed has the advantage not only of high speed, but also of compatibility with such operations as analog multiplication, division, addition, subtraction and function generation.

The speeds and accuracies achievable with the μA722 are applicable to the I/O functions of GP digital computers, namely, data acquisition and displays, and are also applicable to the conversion, condition-setting, and high-speed arithmetic requirements of hybrid computers.

Finally, the low cost, simplicity, and reliability made possible by the existence of integrated circuit building blocks for A/D and D/A conversion will, with time, offer revolutionary system possibilities with respect to the economics of the above applications. This should have a special impact on the computing power versus cost of hybrid computing systems.

APPENDIX

Supply and Ground Lead Ringing Due to μA722 Current Switching

In discussing high speed applications of the μA722, two distinct cases arise:

(1) The current summing bar is loaded by a low resistance (≤200Ω) to ground.

(2) The current summing bar potential is virtual ground; however, current does not come from ground but from the output stage of an operational amplifier.

The effect of switching on all the logic inputs is to steer the full-scale current (≈2.5 mA), which constantly flows in the current sources regardless of the logic state, from the V_{CC}^{+} supply to the current summing bar. The net result is a 2.5 mA current step between the I_S and V_{CC}^{+} terminals. (Actually there are several time-delayed steps, since the bits do not turn on simultaneously; however, bits 1 and 2, which account for 3/4 of the full-scale current, turn on in less than 10 nanoseconds). The equivalent circuit is shown in Figure 1 for case ①.

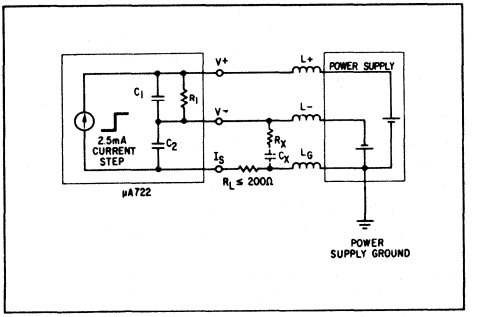


Fig. 1. Equivalent circuit with low resistance load on current summing bar.

R_1 = 1.8 kΩ; V_{CC}^{-} to I_S resistance assumed infinite.

$C_1 \approx 125$ pF = Collector substrate capacitance of Q_{11} - Q_{30}, Q_{41} - Q_{45} and resistor boxes.

$C_2 \approx 70$ pF = Collector substrate capacitance of D_1 - D_{10} + other capacitances, depending on whether the bit is *on* or *off*.

L_+, L_-, L_G are lead inductances from the power supplies to the μA722.

A Y- Δ transformation results in the circuit of Figure 2.

The effect of the current step will be to produce undesirable ringing currents through R_L. Both loop ① and ② will ring.

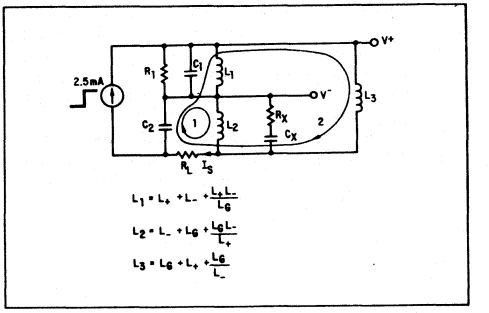


Fig. 2.

A small resistor R_X (≈50Ω) in series with a capacitor C_X (≥1000 pF) for DC isolation will damp both loop currents sufficiently. The damping time constant for loop ① will be approximately $R_X C_2$ or 3.5 nsec. For loop ②, the impedance of the $R_X C_X$ series combination will be considerably less than that of L_L, C_2; hence, a large percentage of the loop current has been diverted from R_L.

For case (2), R_L is replaced by an operational amplifier as shown in Figure 3.

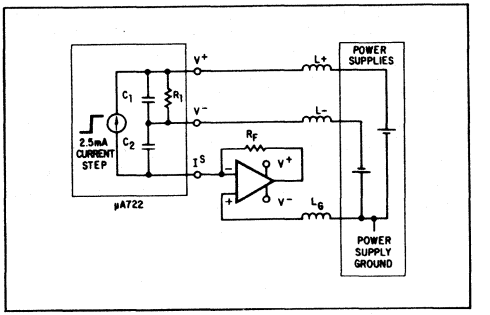


Fig. 3. Equivalent circuit with operational amplifier load on summing bar.

The basic difference between the two cases is that there is no appreciable current flow into the non-inverting terminal of the op amp and therefore L_G is negligible.

Since the response of the operational amplifier is limited by its slewing rate, it will not be able to supply the current required by the μA722 instantaneously; i.e., the equivalent circuit will be as shown in Figure 4.

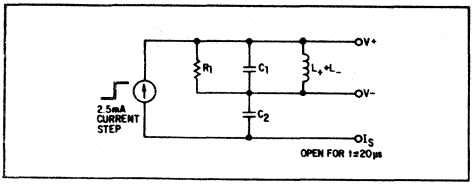


Fig. 4.

The $V^+ - V^-$ waveform will be

$$V^+(t) - V^-(t) \approx 2.5\,mA\sqrt{\frac{L_+ + L_-}{C_1}}\, e^{-\frac{t}{2R_1C_1}} \sin \frac{t}{\sqrt{(L_+ + L_-)C_1}}$$

The time constant ($2R_1C_1 \approx .45\ \mu sec$) does not provide sufficient damping if the lead inductances are too high, notwithstanding the fact that the power supply rejection of the μA722 improves at high frequencies compared to the DC value.

A similar effect occurs with the operational amplifier. A current ramp, the slope of which is determined by the slew rate, can cause ringing as it flows into the V^+ supply. Since op amp power supply rejection falls off at high frequencies, this ringing will show up at the output.

Both of these effects can be damped sufficiently by a small resistor, R_S, in series with the supply leads. The damping time constant is $2L/R_S$, which will be small enough for reasonable lead inductances.

Since the μA722 and the op amp are in close physical proximity, the same supply can be used for both. This will result in only one ringing circuit. Furthermore, switching all logics on effectively steers 25 mA from the μA722 V^+ supply to the operational amplifier V^+ supply, which are tied together; therefore, there is no net change in V^+ supply DC current.

Both the μA722 and op amp can be operated off ±9 V supplies, or zener diodes can be used to drop from ±12 V or ±15 V for the op amp, or to ±6 V for the μA722.

AN IMPROVED SAMPLE-AND-HOLD CIRCUIT USING THE μA740

The sample-and-hold is an often-used circuit in sampled signal processing. The circuit is shown in simplified form in Figure 1. The basic circuit will perform adequately in many applications where speed is unimportant. If fast acquisition time is required, a number of interesting problems present themselves; and these problems limit the usefulness of the circuit. Sampling offset and input signal isolation are special problems to be considered.

Basic Design

First some basic considerations in sample-and-hold design are presented. A practical version of the Figure 1 circuit will be developed as a starting point for further design refinements.

1. Acquisition Time:

The factors influencing acquisition time (the time required to leave the hold mode, sample the input and return to hold) are the source resistance, the "on" resistance at the sampling switch, the value of the holding capacitor and the transient response at the buffer amplifier.

The charging time-constant for the holding capacitor is:

$$T = (R_S + R_{ON})\ C_H \qquad (1)$$

The time allowed for settling must be at least 4.6T for 1% accuracy; 6.9T for 0.1%; 9.2T for 0.01%.

If the buffer amplifier slew rate is faster than the maximum slope of the capacitor voltage, the required acquisition time is determined by T. If the amplifier slew rate is slower than the capacitor voltage slope, then the amplifier affects the acquisition time. The capacitor voltage may reach the correct value before the amplifier has settled, but there is little point in considering the signal to be acquired unless a useful output is available from the circuit.

FAIRCHILD
SEMICONDUCTOR

2. Hold Time:

Performance in the hold mode is determined by the leakage current of the sampling switch, the bias current of the buffer amplifier, and the size of the holding capacitor. The held voltage will gradually change due to the leakage and bias currents flowing through the holding capacitor. If I_C is the net capacitor current, then the slope of the held voltage is given by:

$$\frac{de}{dt} = \frac{Ic}{C_H} \qquad (2)$$

Equation 2 can be used to calculate how long a held voltage will remain within a specified accuracy of its original value.

A Practical Circuit:

Keeping the considerations of equations 1 and 2 in mind, a practical realization of the basic sample-and-hold circuit was developed (Figure 2). The following specifications were assumed:

Signal Range: $\pm$ 5 volts

Accuracy: Better than 0.1% of full-scale input

Acquisition Time: Better than 10μs

Hold Time: 100μs

A good choice for the sampling switch is a J-FET. The device parameters of most importance are "on" resistance and gate leakage current, I_{GSS}. A 2N4382 was chosen because the maximum "on" resistance for this device is 350Ω and the maximum leakage current is 1nA at 25°C.

If the maximum source resistance is 1K, then (from Eq. 1) we have

$$T = (R_s + R_{on})\ C$$

$$T = (1K + 350\Omega)\ C$$

Since the settling time for 0.1% accuracy is 6.9T the maximum value for C can be calculated:

$$6.9T - 10\mu s$$

$$T = \frac{10 \times 10^{6}}{6.9} = 1.45\mu s$$

$$1.45\mu s = (1K + 350\Omega)\ C$$

or

$$C = \frac{1.45 \times 10^{-6}\ s}{1.35 \times 10^{3}\ \text{ohms}} = 1074\ pF$$

C_H was chosen to be 1000 pF

The change in capacitor voltage during the hold mode should be small compared with the accuracy required at the system. The μA740C FET-input operational amplifier was chosen as the buffer amplifier for its good slew rate (6V/μs) and its low input bias current (2nA). The FET leakage and the amplifier bias current partially compensate each other in the Figure 2 circuit. A worst-case estimate of the change in held voltage can be made by assuming that the full amplifier bias current flows from the holding capacitor and that the FET leakage is negligible. Using Eq. 2 we have:

$$\frac{de}{dt} = \frac{2 \times 10^{-9} A}{1000pF} = \frac{2 \text{ volts}}{\text{second}}$$

Thus the slope of the held voltage will be negligible during the 100μs hold interval.

Refining the Design:

At this point we must investigate the problems of sampling offset and input signal isolation. Because of the acquisition time requirement, the holding capacitor is relatively small. Allowing for the accuracy required, the parasitic capacities associated with the sampling FET are significant in comparison to the holding capacitor. This leads us to the following difficulties.

Sampling Offset:

When the J-FET switch is turned "off" a portion of the gate drive signal is coupled onto the holding capacitor. If this coupled voltage were fixed there would be little problem. A fixed amount of charge could be coupled onto the holding capacitor to compensate the offset. The offset is not fixed but is a function of the input signal, since the gate voltage of the sampling switch is equal to V_{in} during the sample mode and goes to V^+ during hold. Furthermore, the gate-to-source capacitance of the FET is a non-linear function of voltage, and thus has a different effective value, depending on signal level..

A compensating scheme that allows for the variation in offset with V_{in} and with device non-linearity is added to the basic circuit in Figure 3. The compensating signal is bootstrapped to the output of the buffer amplifier so that its amplitude is also a function of the input voltage. To compensate for the non-linearity of the FET capacitance, the correction signal is coupled through the gate-to-channel capacitance of another FET which exhibits a non-linearity similar to that of the sampling switch. The amplitude of the compensating signal is reduced by a voltage divider since both the source and drain of the compensating FET are connected to the hold capacitor, giving a larger effective coupling capacitance.

Input Isolation:

During the hold mode, transient changes in the input signal (such as would occur if the input were multiplexed) can be coupled onto the hold capacitor through the stray capacitance of the "off" sampling

switch. With a holding capacitor at 1000pF, only 1pF of combined device and stray capacitance is required to cause a 0.1% error in the held voltage.

Compensation for input transients is accomplished by feeding the input signal through a unity gain inverter and coupling the inverted signal onto the hold capacitor. This cancels the effect of the input transient.

Rather than attempting to obtain a discrete capacitor of a fraction of a picofarad, the input transient compensation is coupled to the hold capacitor through a FET that is always in the off state, as shown in Figure 4. This coupling method provides a capacitance that is very similar to the capacitance of the sampling switch. Circuit layout of similar dimensions for the sampling switch and the coupling FET helps to equalize the effects of stray capacitances.

Overall Performance:

The final circuit for the compensated sample-and-hold is shown in Figure 5. The 20-pF capacitor between the output of the μA740 and its offset-null terminal dampens the overshoot of the amplfier. This overshoot occurs following large (±5 volt) slews of the μA740.

Figure 6 shows the input signal, the sample pulses and a time-expanded view of the difference between the output and the input. The time base for the two input waveforms at the top of Figure 6 is 100μs/cm, and the time base for the output minus the input at the bottom of the figure is 20μs/cm. The first sample-and-hold period shows the effect of the hold voltage changing from -5 volts to +5 volts and still maintaining the +0.1% (i.e., ±5 millivolt) accuracy limit required. The second sample-and-hold period shows the sampling circuit updating, but not changing, the hold voltage. Immediately after acquisition, the output is within 0.5% (i.e., 2.5 millivolts) of the sampled value.

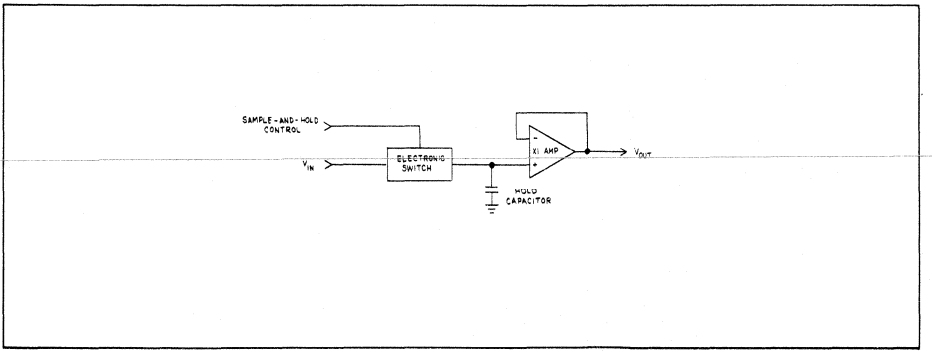


Fig. 1. Basic Sample-And-Hold Circuit

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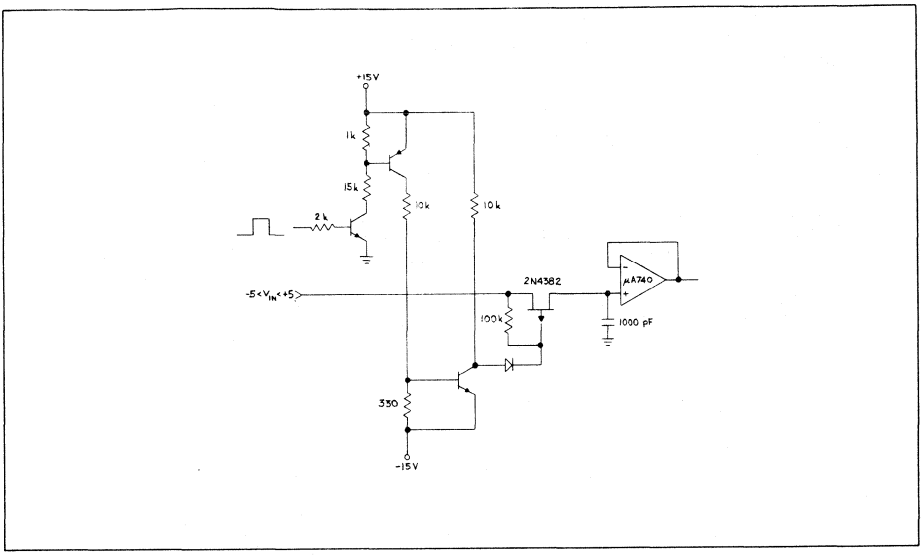


Fig. 2. A Sample-and-Hold Circuit

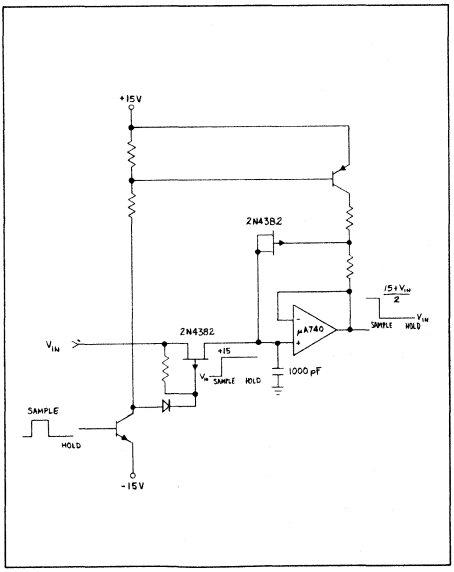


Fig. 3. Sampling Offset Compensation

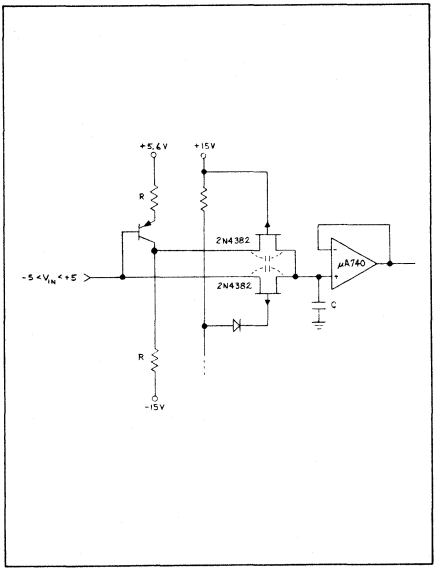


Fig. 4. Hold Mode External Transient Compensation

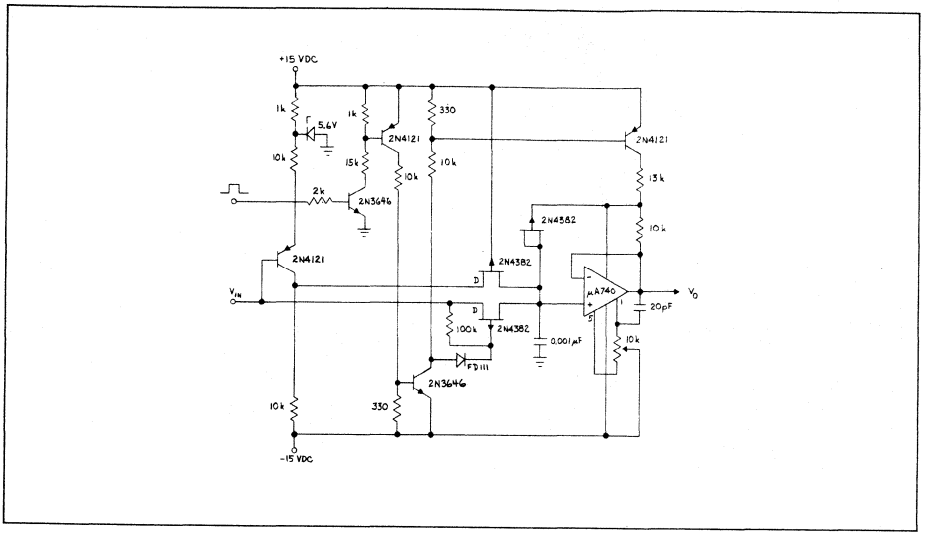


Fig. 5. Sample-and-Hold Circuit with Sampling Offset Compensation and Hold Mode Transient Compensation

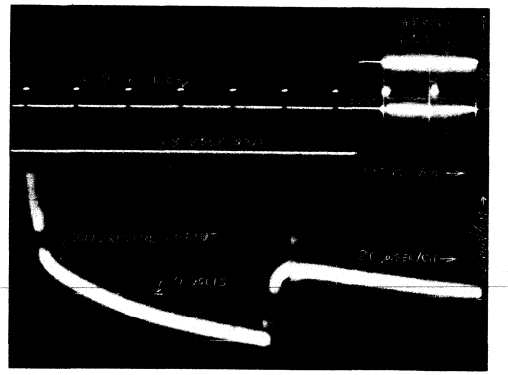


Fig. 6.

APPLICATIONS OF THE μA777

INTRODUCTION

The μA777 is another member of the new generation of non-latching and short-circuit-proof monolithic operational amplifiers. As an added feature it has pin-outs that allow frequency response to be tailored according to the individual user's needs. This paper describes the μA777 and compares it with its very close relative, the μA741. Several application examples are also given to help familiarize the user with some of the μA777's features.

The μA777

The μA777 is an improved version of the μA741 with lower offset and bias currents. It also has the feature that the 30-pF MOS capacitor has been omitted, and the circuit nodes where the capacitor was attached have been brought out to external pins. This change makes possible as much as a 20 times higher gain-bandwidth product for the open-loop frequency response curve. Figure 1 shows the open-loop voltage gains as a function of frequency for three of the possible gain/compensation options. The xl gain curve (C_C = 30 pF) is precisely the same curve as the open-loop voltage-gain plot for the μA741. This fact, coupled with the pin compatability between the μA777 and μA741 makes these devices completely interchangeable except in applications using the expanded gain-bandwidth feature of the μA777.

Pulse Amplifier Using Feed-Forward Compensation

The xl amplifier shown in Figure 2 employs both a feed-forward path and a diode clamp to raise the slew rate and dampen the overshoot in the high-speed pulse response of the μA777. The feed-forward path, consisting of resistor R_2 and capacitor C_2, bypasses the first stage lateral PNP transistors at frequencies above about 355 kHz and thereby raises the slew rate from the specified 0.5 V/μs to approximately 20 V/μs. The two diodes shown in Figure ? minimize the overshoot so that it is less than 1% for any output voltage in the tested range of

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pulse amplitudes from 0.5 to 10.0 volts peak-to-peak.

Wein Bridge Oscillator

The Wein Bridge oscillator shown in Figure 3 uses a junction type field effect transistor, Q_1, operating in its linear resistive region to provide automatic gain control. With the attenuation of the RC network being one-third at the zero phase-shift oscillation frequency, the amplifier gain determined by resistor R_2 and equivalent resistor R_1 must be just equal to three in order to make up the unity gain positive feedback requirement needed for stable oscillation. Resistors R_3 and R_4 are set to approximately 1000 ohms less than the required R_1 resitance. The FET dynamically provides the trimming resistance needed to make R_1 one-half of the resistance of R_2.

The circuit shown in Figure 3 composed of R_5, D_1, and C_1 isolates, rectifies and filters the output sine wave converting it into a DC potential to control the gate of the FET. For the low drain-to-source voltages used, the FET provides a symmetrical linear resistance for a given gate-to-source voltage.

The simplified circuit shown in Figure 4 dispenses with the isolation, rectification and filtering at the cost of slightly higher distortion.

Figure 5 shows the distortion percentages as a function of peak output voltages for each of the two circuits. The curves shown represent data taken with potentiometer R_6 set at a fixed position and with potentiometer R_3 varied to provide the amplitude control. The lowest distortion values result when the set-up procedure is as follows: set R_3 at the midpoint of its range, adjust R_6 until output clipping just begins, and finally use R_3 to reduce the output amplitude to the desired level. Because of the precise nature of the x3 gain requirement, the 1% tolerances specified for R, C, R_2, and R_4 are vital in order to insure proper circuit operation. The median distortion value in the 1 to 5-volt peak output region for the Figure 3 circuit is approximately 0.025%.

Variable Gain Differential Amplifier

The differential amplifier shown in Figure 6 uses the differential form of the resistive T feedback network to achieve a wide variation in gain using a single potentiometer. The differential gain of the circuit is:

$$\frac{V_o}{V_B - V_A} = \frac{2 R_2}{R_1} \left(1 + \frac{1}{k}\right)$$

where k is less than or equal to one. The gain control factor 1 + 1/k varies in a fairly linear manner for values of k similar to one, but it increases very quickly in the high-gain region where k is much less than one. For circuits requiring more linear gain control in the high-gain region, a series range resistor and a potentiometer with a lower resistance significantly improve the gain control resolution.

In order to achieve good common mode rejection in this circuit, the three A-suffix resistors on the top should be symmetrically balanced with the three B-suffix resistors on the bottom. This is particularly important for the two input resistors R_{1A} and R_{1B} and their associated source impedances. Inserting a trimming potentiometer, R_3, in either the A or the B side will aid in this balancing. With the addition of a small trimming capacitance, C_1, to balance AC impedances at the plus and minus input nodes, the circuit exhibits as much as 60 db of common mode rejection ratio independent of the value of k and of the frequency of operation.

As an example of AC imbalance, the breadboard circuit shown in Figure 6 (using an R_3 value of 500 ohms) had a common mode rejection ratio of only 40 db at the null setting of R_3 until a 1-pf trimmer was added (shown as C_1 on Figure 6). The rejection ratio then increased to 60 db, independent of either gain settings or frequency variations.

Conclusion

The μA777 is a versatile monolithic operational amplifier for use in signal generation and processing. The individual frequency response tailoring, exemplified in the pulse amplifier with feed-forward compensation circuit, demonstrates the high-speed operation possible with this device. The 0.025% distortion figure attainable using the μA777 in a Wein Bridge Oscillator shows the quality of performance one can expect from this device.

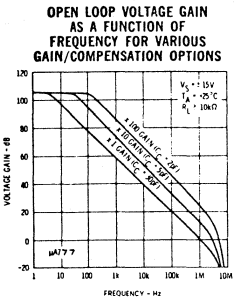
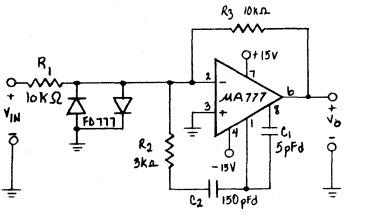
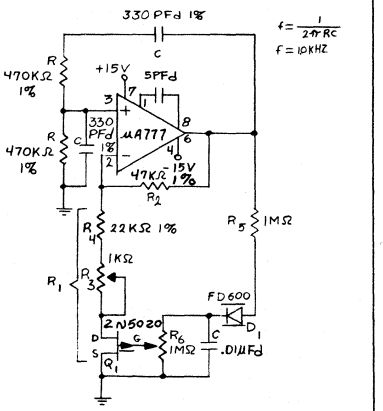


FIG. 1



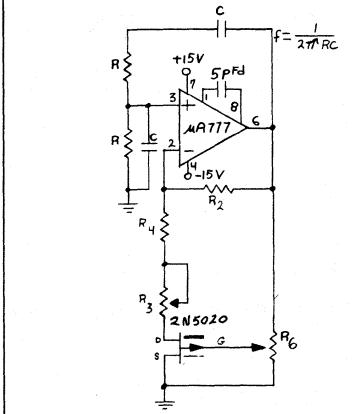
PULSE AMPLIFIER

FIG. 2



WEIN BRIDGE OSCILLATOR

FIG. 3



SIMPLIFIED WEIN BRIDGE OSCILLATOR

FIG. 4

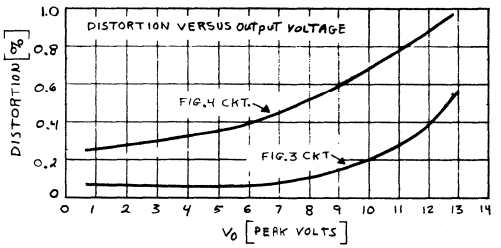


FIG. 5

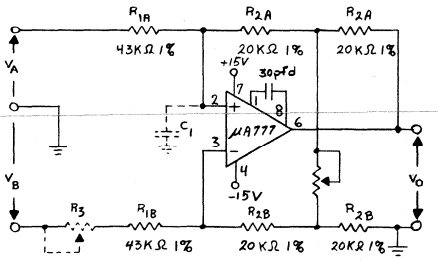


FIG. 6

THE POWER AMPLIFIER USING THE μA777

INTRODUCTION

The circuit described in this paper provides a quick and efficient design for transforming an integrated circuit operational amplifier into a power amplifier capable of driving ampere-level currents at supply voltages in the ±30-volt range or more. Amplifier response is flat from DC to about 100 KHz with distortion values ranging from 0.05% to 0.1% at 1 KHz, dependent on the output currents required.

Applications of this circuit configuration include servo drivers, audio amplifiers and a variety of control circuits in which flat response and medium power characteristics are desirable.

BASIC CIRCUIT

The operation of the circuit shown in Figure 1 depends largely on the high power supply rejection ratio (typically 13 μV/V) and the Class B configuration found in the output stage of the μA777. The effect of these two factors is that any positive current signal flowing through resistor R_1 appears in undistorted form at the positive voltage supply terminal (pin 7) and any negative current signal through R_1 appears undistorted at the negative voltage supply terminal (pin 4). Capacitor C_2 supplies stabilizing negative feedback for the output stages and has no significant effect on the forward current amplification of the circuit. Zener diodes D_{Z_1} and D_{Z_2} cause a level shift of the plus and minus current signals from the $\pm V_{source}$ requirements of the μA777 to whatever supply voltages are required to drive the load.

Transistors Q_1 and Q_2 amplify these currents and drive the bases of the Class B output power transistors Q_3 and Q_4. Diode D_3 and resistor R_3 develop just enough voltage from the amplified standby current of the μA777 to keep transistors Q_3 and Q_4 biased ON and thereby minimize crossover distortion when the amplifier output passes through zero volts. Resistors R_2 and R_f determine the amplifier's net voltage

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gain, while capacitor C_1 in conjunction with R_f determines the 3-db down or high-frequency rolloff of the circuit.

DESIGN CONSIDERATIONS

The first requirement in using the basic circuit configuration shown in Figure 1 is to choose the appropriate supply voltage and related zener voltage values for a given load resistance and load power requirement. Allowing a conservative 6-volt minimum drop across Q3 and Q_4, the equation relating output power, load resistance, and source voltage is;

$$P_{out} = \left(\frac{V_s - 6}{\sqrt{2}} \right)^2 \quad \frac{1}{R_L} \qquad (1)$$

Taking an example of 35 watts through an 8-ohm load yields:

$$V_s = \sqrt{2\ R_L\ P_{out}} + 6 \qquad (2)$$

$$V_s = 30 \text{ volts} \qquad (3)$$

The zener voltage should be equal to the source voltage minus the operating voltage of the µA777. Choosing a 15-volt supply for the µA777 gives:

$$V_{zener} = V_s - 15\ V \qquad (4)$$

And for the given example with $V_s = \pm 30$ volts:

$$V_{zener} = 15 \text{ volts} \qquad (5)$$

The only remaining requirement is that the four transistors Q_1 through Q_4 be capable of handling the two times V_s standoff voltage (in this case 60 volts) without breaking down.

BREADBOARD CIRCUIT RESULTS

Figure 2 shows distortion versus load current for the circuit. Distortion remains relatively constant at about 0.05%, except at the lower output current levels. This increase at low signal levels is due to the emergence of noise as a factor with respect to the signal level.

The frequency response shown in Figure 3 demonstrates that the 3-db down frequency is 180 KHz using an R_f resistor value of 30 KΩ and a parallel capacitance of 30 pF.

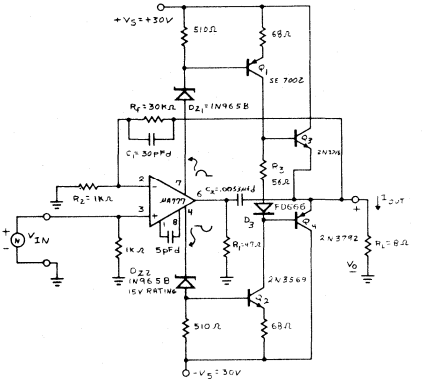


Figure 1. Schematic Diagram

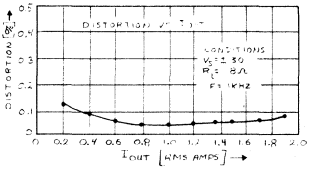


Figure 2. Distortion vs. Load Current

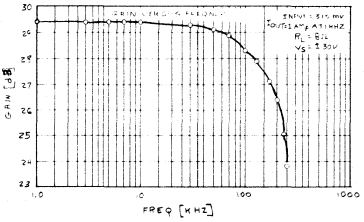


Figure 3. Frequency Response

APPLICATIONS OF THE μA785 TV SIGNAL PROCESSING INTEGRATED CIRCUITS

INTRODUCTION

The purpose of this Application Brief is to familiarize the video designer with the monolithic μA785 video signal processing integrated circuit and to present several applications for the device. Principal uses of the μA785 are in TV receivers, video numeric generators, servo controls for video tape recorders, monitoring of video levels and for video clamping.

The following functions of the device are described:

1. Video preamplifier
2. Noise separator
3. AGC (automatic gain control) and delayed AGC
4. Sync separator
5. Horizontal phase detector
6. Vertical separator

A complete schematic of the device also is included (Figure 10).

The μA785 internal circuits are shown in block diagram form in Figure 1.

VIDEO PREAMPLIFIER

The video preamplifier is fed at pin 10 with a 2-volt (peak-to-peak) negative-going signal, Figure 2. After passing through two stages of amplification and a buffer stage, a 6-volt (peak-to-peak) composite video signal appears on pin 12, across an external 390-ohm resistance, R_1. The preamplifier has a gain of 3, with a bandwidth greater than 5 MHz. A positive-going pulse between 1 and 5 volts can be applied at pin 11 to provide blanking of the output video. The output from the first video stage feeds the input circuits of the noise separator,

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the AGC circuit and the sync separator.

NOISE SEPARATOR

The noise separator consists of an amplitude noise detector and a frequency-selective noise detector. The output of both detectors is fed to an OR gate, and the output of the OR gate is used to turn off both the AGC circuit and the sync separator circuit when noise is present. The external resistor and capacitor (R_2 and C_1) connected between pins 8 and 9 provide a path to the OR gate input for large amplitude noise.

AGC (AUTOMATIC GAIN CONTROL)

The gated AGC provides a DC voltage of 1 to 8 volts (proportional to the amplitude of the sync signal) across capacitor C_2 at pin 4. The delayed AGC voltage of 1 to 7 volts is generated across C_3 at pin 6. The amount of AGC delay is determined by the voltage at pin 7 and can be adjusted by a potentiometer. The 1 to 5-volt gating pulse is applied at pin 3.

SYNC SEPARATOR

The sync separator assures a slicing level at a point about 30% below the top of the sync pulse. This slicing level is independent of the input video level. A constant slicing level is maintained since the bias on capacitor C_4 (connected to pin 13) varies with the video level. The output of the sync separator drives both the horizontal phase detector and the vertical separator.

HORIZONTAL PHASE DETECTOR

As shown in Figure 3a, the horizontal phase detector consists of an AND gate, an amplifier stage and a clamp transistor.

A sawtooth waveform is generated by integrating a negative-going flyback pulse. This sawtooth is applied to the collector of the clamp transistor at pin 2 and is clamped to the reference voltage applied at pin 1.

The amplified output pulse of the AND gate turns the clamp transistor on and off during coincidence of the sync pulse and the flyback pulse. The average DC voltage of the clamped sawtooth waveform shown in Figure 3b will be either above or below the reference voltage depending on whether the phase of the flyback pulse is leading or lagging in respect to the sync pulse. This phase detector has a sensitivity of 0.75-volt/μs and is used to control the horizontal oscillator. Typical holding and catching ranges are 1 kHz and 800 kHz, respectively (for an oscillator-reactance stage with a control sensitivity of 450 Hz/V).

VERTICAL SEPARATOR

A positive-going vertical pulse of 10 volts is obtained from pin 15. With an external capacitor (C_5) equal to 0.02 µF, the vertical pulse will have a width of 15 µs.

APPLICATIONS FOR THE µA785

The µA785 can be used in a variety of applications, depending on how the circuit functions are used.

TV RECEIVERS

In a TV receiver (for which the µA785 is primarily designed), all six functions described above can be used to process the video signal in the luminance channel. In this case, the output of the video detector is fed to pin 10 of the video preamplifier, Figure 4. The output of the amplifier at pin 12 feeds the delay line with the signal that drives the video output stage. Horizontal and vertical blanking pulses are connected to pin 11. The forward IF and delayed RF AGC are fed from pins 4 and 6 to the respective amplifiers. The amount of delay is determined by the voltage applied at pin 7. The phase detector, used as described in the block diagram, controls the horizontal oscillator by integrating the clamped sawtooth waveform at pin 2. The vertical output pulse from pin 15 triggers the vertical oscillator.

The µA785 also is very useful in applications that need sync pulses and vertical pulses from a composite video signal, such as a video numeric generator, a servo control for a video tape recorder, special effects generator, or a video switcher. In this type of application, the clamp transistor of the phase detector can be used as a switch by connecting pins 2 and 3 to the supply voltage through a 3-KΩ resistor and by biasing pin 1 at 4 volts, as shown in Figure 5. The output at pin 2 is a composite sync signal, except that the vertical serration is of opposite polarity. A separated composite sync may be taken from pin 3. A few such applications are briefly described in the following.

VIDEO-NUMERIC GENERATOR (Figure 6)

A video-numeric or character generator electronically generates characters which can be fed into a standard TV raster-scan display along with the normal video. Channel number, time, temperature or any other information can be displayed in this manner.

The generator requires both horizontal and vertical sync which can be obtained conveniently from the µA785.

Figure 6b shows how the vertical and horizontal outputs can be converted to standard logic levels to drive character generators.

SERVO CONTROL FOR VIDEO TAPE RECORDER (Figure 7)

In the record mode of a video tape recorder, the servo system locks the rotational rate of the scanner head to the field rate of the

incoming video signal. The vertical pulse is recorded on the edge of the tape and is used as a control track during playback. The servo system also uses the horizontal pulses of the incoming video to control the capstan motor. The µA785 can provide these two horizontal and vertical pulses from an incoming video signal.

MONITORING OF VIDEO LEVEL

In applications where the video level is monitored on a DC meter (either to adjust a video recording level or to open the lens of a TV camera), the AGC and delayed AGC of the µA785 can be used as shown in Figure 8. The delayed AGC in this case may be used to turn on a red warning light when the amplitude of the signal is above a level preset by the voltage at pin 7.

VIDEO PROCESSORS

In some video processors, such as TV cameras, the signal from the video amplifier is AC coupled to a gamma-correcting network or to a delay line. To restore the DC level, the phase detector of the µA785 may be used as a clamp with a reference DC voltage set at pin 1 as shown in Figure 9.

CONCLUSION

The µA785 (video signal processing circuit) is used in both color and black-and-white television sets. It performs six functions, all of which are useful in many other video circuits as well as in television receivers. Four practical combinations of the device's internal circuits have been described. Modern integrated circuit technology used in designing and manufacturing the µA785 assures its reliability and uniformity.

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3. Integrated Signal Processing Circuit for TV Receiver (TAA700) Philips Report: 16PV1X by A. Cense and Jvan Straaten.

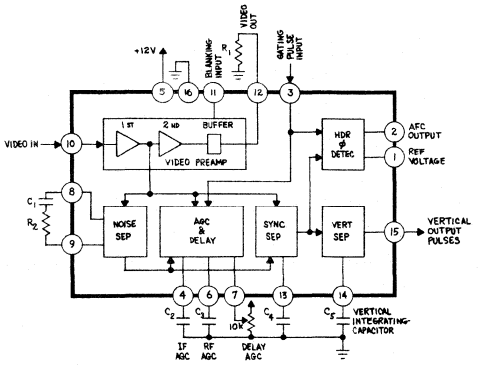


Figure 1. Block Diagram

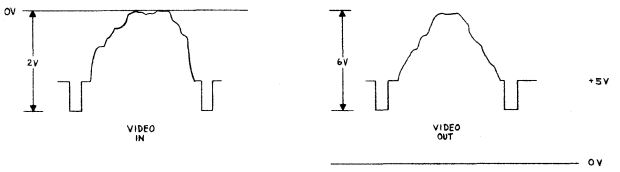


Figure 2. Peak-to-Peak, and DC Level at the Input and Output of the Video Preamp.

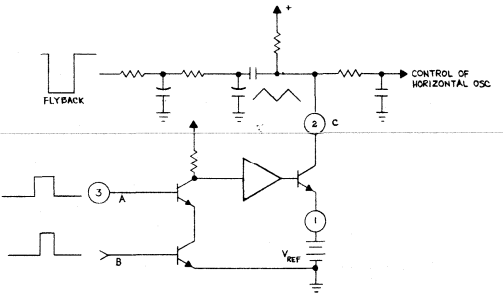


Figure 3a. Horizontal Phase Detector.

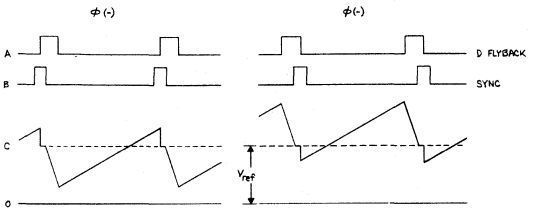


Figure 3b. Average DC Error Voltage Generated by the Horizontal Phase Detector for Leading and for Lagging Flyback Pulse with Respect to Horizontal Sync.

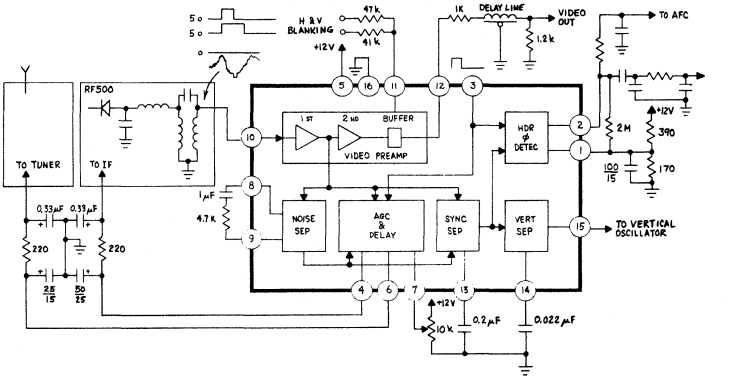


Figure 4. μA785 for Television Receivers.

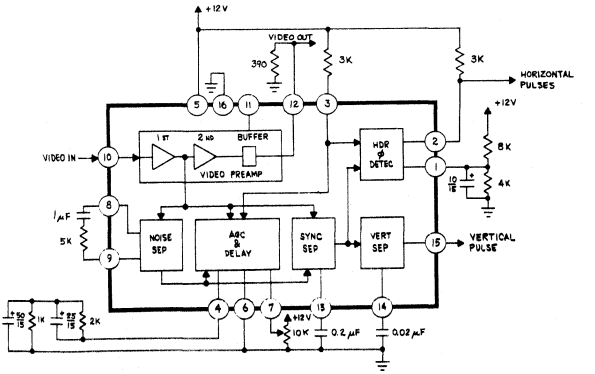


Figure 5. Sync Pulses and Vertical Pulses for a Special Effects Generator or a Video Switcher.

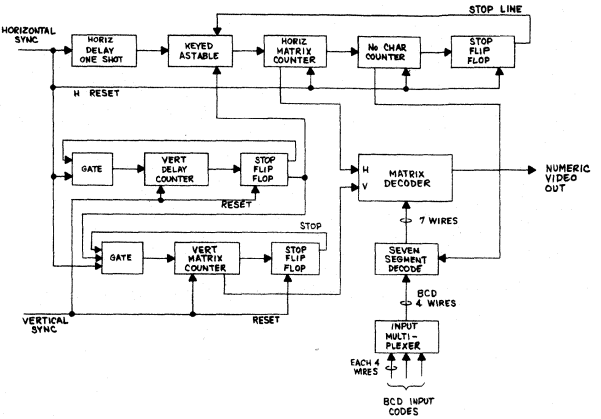


Figure 6a. Block Diagram for a Video Numeric Generator.

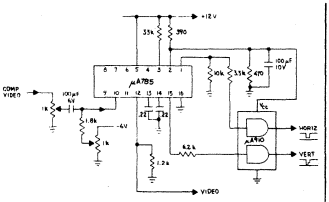


Figure 6b. Conversion of Horizontal and Vertical Pulses to Standard Logic Level.

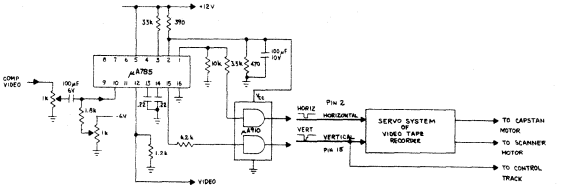


Figure 7. μA785 in Conjunction with Servo Control of Video Recorder.

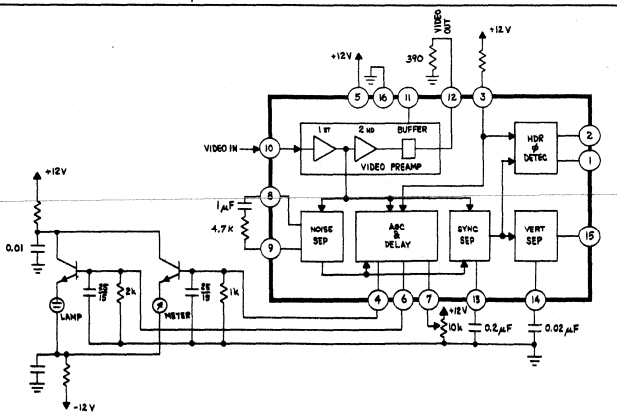


Figure 8. μA785 Used to Generate Analog DC Voltage Corresponding to Video Level.

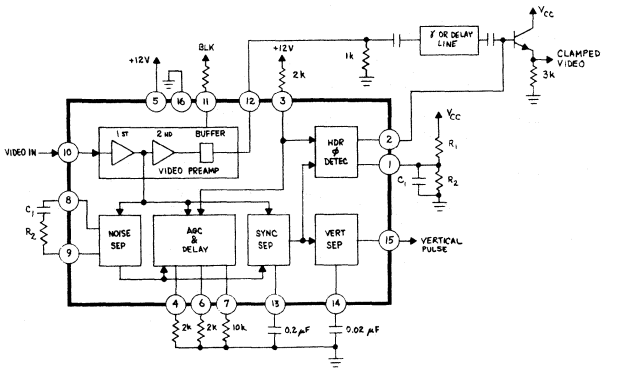


Figure 9. Video Amplifier and Video Clamp.

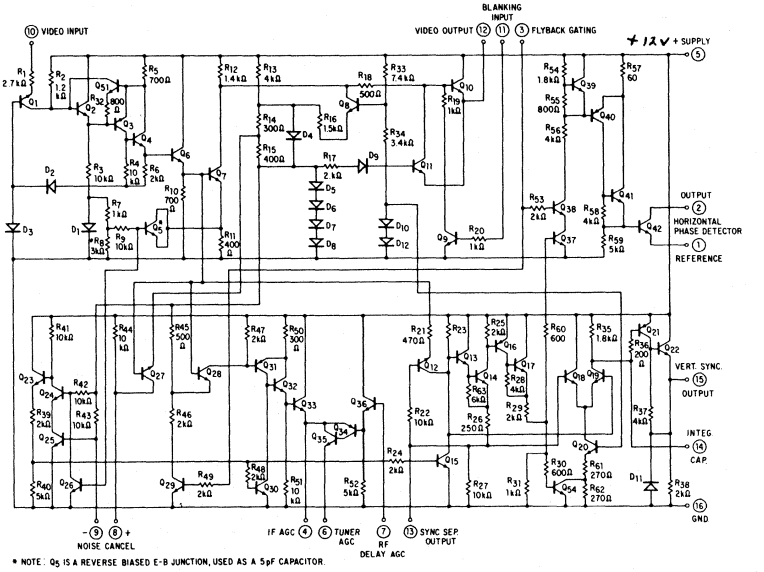


Figure 10. Schematic of the μA785.

APPLICATIONS OF THE μA739 AND μA749 DUAL PREAMPLIFIER INTEGRATED CIRCUITS IN HOME ENTERTAINMENT EQUIPMENT

INTRODUCTION

The μA739 and μA749 circuits consist of two identical amplifiers with common bias. They are designed as low-cost dual operational amplifiers for general industrial and consumer applications. Three applications for home entertainment are discussed in this paper: a high fidelity phonograph preamplifier, a stereo tape amplifier, and a TV remote control amplifier. The power supply rejection, linearity, low noise, and flexibility of the circuit make it an ideal building block in home entertainment systems.

PHONOGRAPH PREAMPLIFIER

A phono preamplifier circuit must have good signal-to-noise ratio, wide dynamic range, low distortion, good channel separation, and should also be reproducible on a volume basis. The μA739 and the μA749 satisfy these requirements and can be used in phono circuits in a wide variety of configurations to suit individual needs. In the circuits described in this paper, the gain is 40dB at 1kHz, a typical value for phono circuits.

D-C Considerations

With a single power supply, the d-c output voltage should be adjusted so that the maximum signal can be obtained from the amplifier. If equal bias source resistances are used, the d-c operating point will depend on the magnitude of the offset current in the IC and not on the bias current. To reduce both the charge on the coupling capacitors and the size of filter capacitors for the bias network, the plus input of the IC is biased at 10% of the power supply voltage. The d-c gain of the circuit is set at 5 by the feedback to the minus input, thus setting the output at 50% of supply. Both plus inputs are biased from the common bias point to reduce the parts count. In a high fidelity circuit, the ground for the bias circuit should be returned to a good audio ground to eliminate hum from the input. The power supply turn-on and turn-off time constants should be sufficiently long to allow the output capacitor to charge without introducing pops and thumps in the system output.

Allowances should be made in the power supply for current drain fluctuations caused by resistance fluctuations in the IC. These resistance fluctuations (±20%) must not cause the power supply voltage to exceed the maximum allowable voltage (36 volts). The μA749 reduces the severity of this problem. The outputs are uncommitted on this configuration, and the total current drain depends on the tolerance of the resistors used for d-c loads on the output of each half. An additional advantage of the μA749 is that the output current can be set as high as 5 mA so that the IC can drive a lower impedance load.

The μA739 can operate with fewer components if both plus and minus power supplies are used. There are two reasons for this: First, the bias for the plus inputs of the IC are referenced to ground directly, eliminating the need for a bias source with nominally 1μV of hum from the power supply. Second, the filter requirements for the power supplies are reduced considerably by the power supply rejection of the IC.

With a dual supply, the output swing will be maximum if each side of the μA739 is biased from the same source impedance. Since the feedback is a-c coupled, the d-c gain is unity and the output stays at a nominal zero volts. An additional advantage of this bias is that the capacitors coupling the output, feedback, and input do not charge to large d-c voltages. As a result, turn-on and turn-off thumps are reduced. The choice of 1MΩ bias resistors is based primarily on a-c considerations. (It should be noted that the bias current could cause as much as 2.5 volts drop across these resistors).

Compensation

The amplifier must be compensated for the unity gain that phono circuits have at high frequencies. Since the open loop phase of the μA739 is 180 degrees at 1.5 MHz, the amplifier must have less than unity gain at this frequency. Several methods of shaping the forward gain response will satisfy this requirement, and it is instructive to learn what differences can be expected with different compensating circuits. In the following paragraphs we will describe four different compensations: (1) Normal voltage follower compensation, (2) Second stage compensation, (3) Feedback compensation, and (4) Single component compensation.

FAIRCHILD
SEMICONDUCTOR

(1) Normal Voltage Follower Compensation

This compensation, shown in Figure 1A, gives the frequency response curve shown in Figure 2A by combining two different compensations:

- Feedback compensation around the output stage of the amplifier
- Loading compensation between the collectors of the input stage of the amplifier.

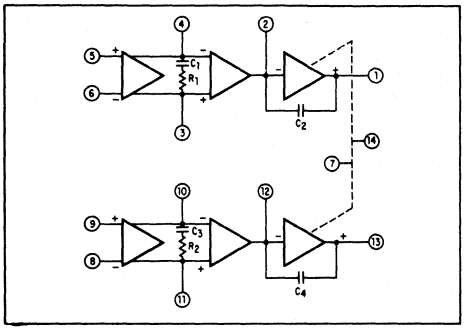


Fig. 1A. Voltage follower compensation.

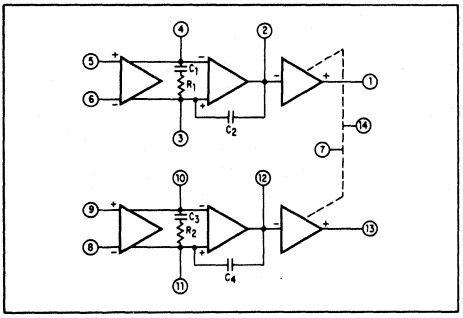


Fig. 1B. Normal phono compensation.

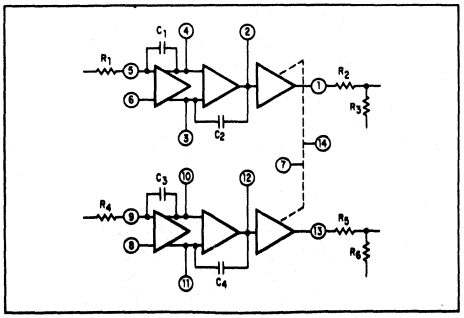


Fig. 1C. Wide band phono compensation.

Figure 2B shows the contribution of each component to the overall compensation of the circuit. The compensation at the input collectors does most of the gain reduction. With the compensation shown, the input R-C network produces 60dB of gain reduction. The output compensation is effective at high frequencies to complete the desired amplitude response.

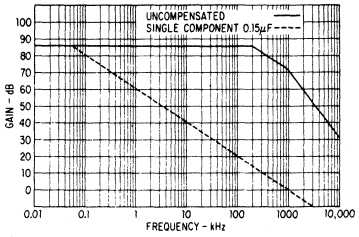


Fig. 2A. Open loop response and simple compensation.

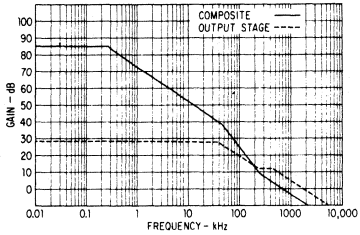


Fig. 2B. Open loop response for voltage follower operation.

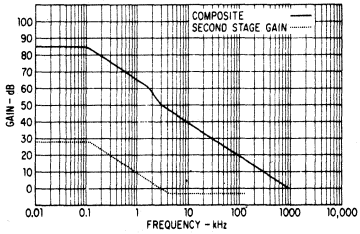


Fig. 2C. Open loop response for normal phono.

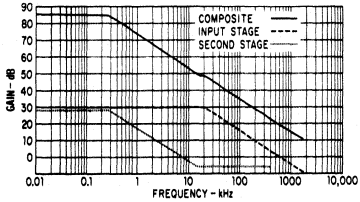


Fig. 2D. Open loop response for maximum slew rate.

Normal voltage follower compensation stabilizes the amplifier for any input and output loading, but it has one peculiarity. When the amplifier is operated at high frequencies, the input stage can no longer supply enough current to the second-stage transistors, and the amplifier is slew-rate limited. For normal unity gain operation, the output rises (or falls) at a rate determined by the component values and the current available. However with phono compensation, the feedback phase is such that the overdrive on the input causes the compensating capacitor C in Figure 1A, to charge in one direction until the capacitor is offset sufficiently to produce an unbalance in the second stage. This unbalance then causes the capacitor to charge in the other direction. Thus the amplifier has a low frequency oscillation superimposed on the signal. An oscillatory condition of this sort will occur in phono circuits for most types of compensation. However, the frequency at which the oscillation starts, as well as its magnitude, can be controlled. A variation on this compensation, in which the output compensation is accomplished by loading the amplifier output with capacitance, is suitable for some applications.

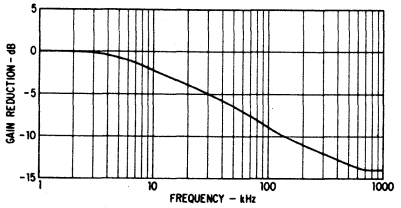


Fig. 3. Reduction of output stage gain due to equalization loading.

Note that the phono equalizing circuit changes the forward response as shown in Figure 3. In a typical application the total compensation inserted by the equalizing network can be used as part of the amplifier compensating network. Changing the impedance level of the feedback equalization eliminates one part from the circuit and also reduces the high frequency output capability. (See the curves of voltage output versus frequency for various compensations shown in Figure 4).

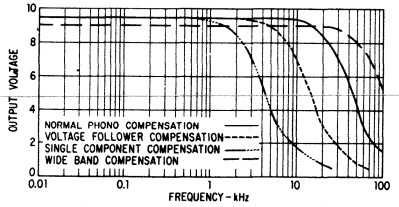


Fig. 4. Output voltage as a function of frequency for various circuits. Harmonic distortion - 1%.

(2) Second Stage Compensation

Feedback compensation around the second stage can bring about an improvement in high-frequency voltage output. This compensation inserts a gain reduction 6dB greater than the gain of the second stage, has only a second order effect on the output capability, and can be easily inserted in the low-frequency spectrum without using large capacitors. The second stage is converted to a voltage follower by means of a capacitor as shown in Figure 1B.

Figure 2C shows the contributions of each compensating section. The R-C combination across the input collectors completes the compensation in a manner similar to that shown in Figure 1A. This type of compensation has two advantages: (1) It results in an amplifier that is stable for any source and load condition. (2) It allows the amplifier to deliver full output to a higher frequency, as shown in Figure 4.

(3) Feedback Stage Compensation

In very high quality phono circuits, full output capability through the entire audio band is desirable but requires additional compensating components. The compensation shown in Figure 1C can give maximum output to beyond 50kHz. In all, five components are required for this configuration whose use is restricted to the μA749 with the uncommitted output collectors. Feedback compensation is used around both the second stage and the first stage. The R-C network on the first stage acts as a Miller integrator to roll off the input stage gain. The resistor in series with the output isolates the amplifier from capacitive loads, and the resistor in series with the feedback equalization isolates the amplifier from the loading of the equalization network. The forward response of the circuit is shown in Figure 2D.

Schematically it would appear that this is a stable unity gain configuration. This would be true if the first stage were in fact an ideal amplifier. But at high frequency (above 1 MHz) the first stage open loop gain decreases, and the feedback capacitor feeds signals through directly from the input. This anomaly makes the role of R_3, the series feedback resistor in Figure 1C, a dual one. (1) It isolates the amplifier output from the capacitive load presented to the feedback. (2) It limits the feedback above 50kHz so that the amplifier has 16dB of gain at high frequency.

For circuits requiring full output to high frequency, this circuit offers a method of obtaining the desired performance. One side benefit of this compensation is the absence of motorboating associated with high-frequency, large-signal operation. By the time the amplifier becomes slew-rate limited, the feedback signal is in phase with the output and the capacitors charge equally on both halves of the signal cycle. The output in the audio band is slightly lower owing to the voltage drop across R_2 in Figure 1C, as is seen in Figure 4.

(4) Single Component Compensation

In some equipment the output is connected to a known load, and the input has a known source impedance. The μA739 can be used in these systems by compensating only at the input collectors. The amount of compensation inserted by the network at the input collectors is determined by the total impedance of the network between the collectors. If the total contact resistance plus the capacitor ESR is two ohms, the network will insert 80dB of attenuation. This attenuation, together with the compensation inserted by the equalizing network, gives stable operation in a fairly broad range of source and load impedances. This compensation is advantageous in systems that are sensitive to total component count and total cost.

Noise Performance

The noise output from a phono circuit is a function of the equivalent input noise and the gain. For any compensation, the audio passband (10Hz to 10kHz) noise must by definition be the same for the same gain and same terminating impedances. One would expect that the audio passband noise and compensation are independent, as indeed they are. However, if the noise is measured on a wide band meter, then the out-of-passband noise -- 1/f noise and high frequency noise -- does in fact differ for different compensations.

1/f noise is a function of the low frequency terminating impedance and the low frequency gain. The phono feedback arrangement has a gain vs frequency response shown in Figure 5. The components might vary in different systems, but the shape is relatively fixed for the application. Hence the low frequency noise is dependent on the value of the input capacitor.

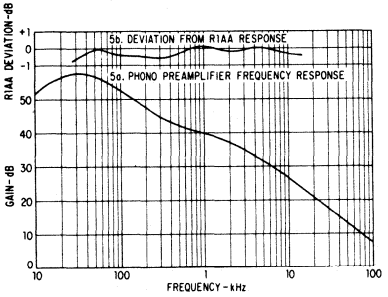


Fig. 5

High frequency noise output depends on the phase margin of the amplifier. The amplifier, when connected as a phono amplifier with 40dB of 1kHz gain as shown, will have unity gain at about 200kHz. Peaking of the response at high frequency will cause noise output in a narrow band about the peaking frequency.

TABLE I.
Noise Outputs and Phase Margins for Three Circuits

CIRCUIT	WIDE BAND NOISE	PHASE MARGIN	AUDIO PASSBAND NOISE
1A	550 μV	25°	120 μV
1B	220 μV	70°	120 μV
1C	130 μV	90°	120 μV

The variation in wide band noise output, shown in Table 1, demonstrates the differences in high frequency peaking. Audio passband noise output from 20Hz to 20kHz is, as expected, the same for all compensations. However wide band noise is not constant and in fact is a function of phase margin. The dependence of wide band noise on phase margin is shown in Table 1. Note that the circuit in Figure 1C, which has the largest gain bandwidth product, has the lowest wide band noise output. This is another indication that the high frequency noise is a function of phase margin rather than high frequency noise figure.

A key feature of the μA739/μA749 is an input noise as low as the input noise in the best discrete designs. Typical performance of 1.2μV input noise gives signal-to-noise ratios of 78dB for 40dB 1kHz gain.

Linearity

Figure 6 shows plots of distortion versus frequency for the phono circuit. The μA739/μA749 has considerably less distortion (typically <0.1%) than discrete designs.

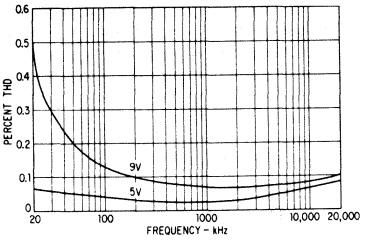


Fig. 6. Distortion vs frequency @ $V_O = 5V + 9V$.

Comments

The μA739 or the μA749 can be used in a wide range of phono circuits. The flexibility of operating supplies and compensation networks makes the μA739/μA749 suitable for any phonograph requirement. This flexibility, along with low cost, gives the user a wide range of system applications for the μA739 and μA749. Complete schematics for stereo phono pre-amplifiers are shown in Figures 7A, B, and C.

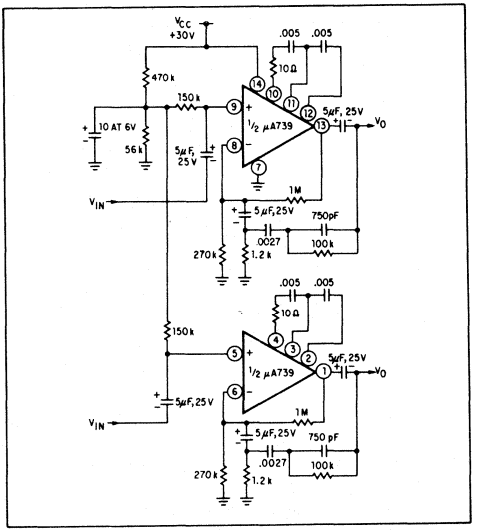


Fig. 7A. Phono preamp single supply.

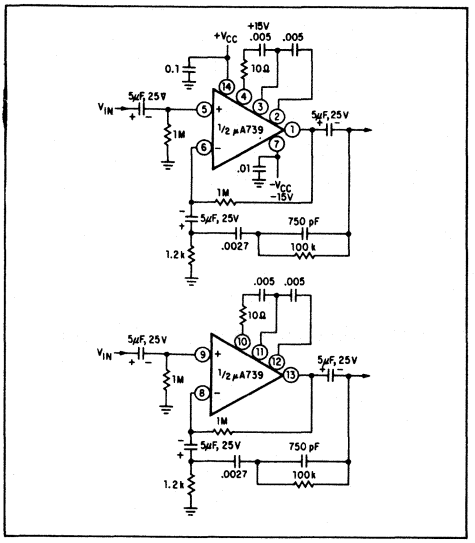


Fig. 7B. Phono preamp dual supply.

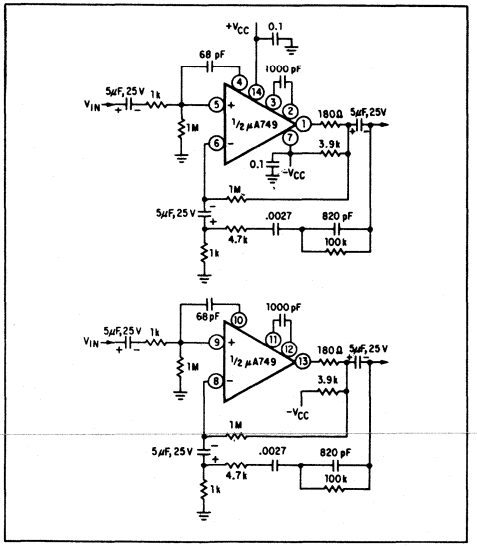


Fig. 7C. Phono preamp wide band.

Stereo Tape Amplifier

Tape deck amplifiers for cartridge tape systems must have high gain and good signal-to-noise ratio. The dynamic range requirement is not severe, but the recording level is usually so low (typically 200 μV), that interference from tape motors, power supply circuits, and switching circuits often influence performance. The μA749 minimizes the problems associated with extraneous signals in the amplifier input, and in general performs better than discrete designs.

Circuit Description

D-C Biasing

The schematic is shown in Figure 8. R_1 and C_1 are power supply decoupling for the circuit. Since the power supply rejection of the μA749 is typically 80dB, no further filtering is needed for the supply. R_2, R_3, and C_2 bias the plus input of the μA749. The bias current for the input (less than 2.5μA) flows through the playback heads. R_6 and R_7 bias the minus input with feedback from the output of each amplifier. R_{10} and R_{11} are the collector loads to ground for the output stage.

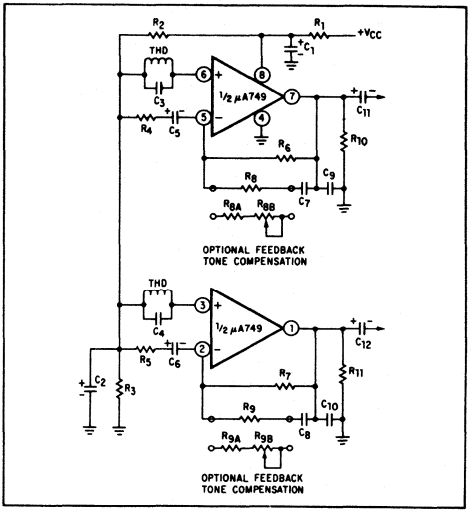


Fig. 8. Tape preamp.

Compensation

Compensation for each amplifier is provided by C_3, C_4, C_9, and C_{10}. The output compensation, C_9 and C_{10}, rolls the amplifier open loop gain off to insure stability with tape equalization. C_3 and C_4 terminate the tape head and provide a low source impedance for the plus inputs at frequencies above the audio passband.

A-C Considerations

The gain and playback equalization are fixed by the feedback components R_4, R_5; C_5, C_6, R_6, R_7; C_7, C_8; R_8, R_9. The value of C_5, C_6 and R_4, R_5 determine the low frequency rolloff below 50Hz. The shape of the equalization is established by R_6, C_7, R_8, and R_7, C_8, R_9. R_8 and R_9 can be used as tone control pots as shown in Figure 8 if there is sufficient compensation to insure

stability of the amplifier in the full cut position. Two sets of values are listed in Table 2 for different closed loop gains. Both sets of values are for nominal 13-volt battery operation.

TABLE II
Values for Tape Amplifier

50H Av	CIRCUIT 1 75 dB	CIRCUIT 2 65 dB
R_1	220	220
R_2	1.5M	1M
R_3	1.5M	1M
R_4	100	270
R_5	100	270
R_6	1.5M	1M
R_7	1.5M	1M
R_8	33k	22k
R_9	33k	22k
R_{10}	10k	4.7k
R_{11}	10k	4.7k
C_1	250μF, 15 V	250μF, 15 V
C_2	1μF, 15V	1μF, 15 V
C_3	470 pF	470 pF
C_4	470 pF	470 pF, μF
C_5	25μF, 3 V	5 μF, 3 V
C_6	25 μF, 3 V	5 μF, 3 V
C_7	.002μF	.0015 μF
C_8	.002μF	.0015 μF
C_9	.0047μF	.0047 μF
C_{10}	.0047μF	.0047 μF
C_{11}	5μF,15 V	5 μF, 15 V
C_{12}	5μF,15 V	5 μF, 15 V

Circuit Performance

The frequency response of a tape circuit is shown in Figure 9. Feedback equalization makes the response uniform for variation in supply voltage, temperature, etc.

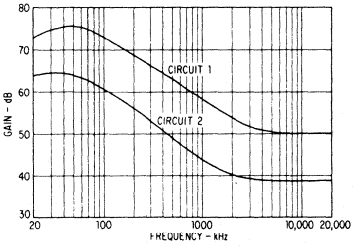


Fig. 9. Tape preamp frequency response.

Harmonic distortion is plotted in Figure 10. The high output capability and high gain of the μA749 give the user a choice of operating gains up to 75dB at 50Hz. The signal-to-noise ratio for the amplifier is typically 55dB (bandwidth 50Hz to 10kHz, reference level 200 μV at 4000Hz). The common mode rejection of the μA749 reduces motor hum, switching transients, etc. by 75dB. Frequency response is changed less than 0.25dB by variation in power supply voltage from 10V to 16V.

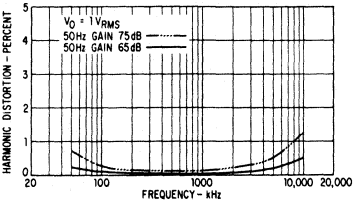


Fig. 10A. Harmonic distortion as a function of frequency.

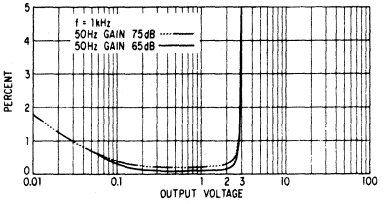


Fig. 10B. Harmonic distortion as a function of output voltage.

TV REMOTE CONTROL RECEIVER

General Description

The TV remote control receiver consists of a high gain amplifier, a transformer and coil for selectivity, and a relay driver. The signal from the transmitter is detected by a condensor microphone and fed to the amplifier. This amplifier must have high gain and low noise, and the μA749 connected in cascade satisfies both these requirements. After amplification, the signal is applied to the base of the relay driver through a frequency-selective output transformer. The amplified and rectified signal activates the relay. Since the signal strength is a function of the position of the transmitter with respect to the receiver, operation must be maintained for a wide range of signals. The performance must be unaffected by fluctuations in line voltage or temperature.

Circuit Description

The operating point of the μA749 shown in Figure 11 is established by the d-c bias network R_1, R_3 and C_3, feeding the plus input through R_2. A feedback loop from the output of the first amplifier through R_5 to the minus input completes the bias and also stabilizes the operating point. The second amplifier is direct-coupled to the first. The minus input of the second amplifier is biased in the same way as in the first amplifier through R_8. R_6 and R_9, the load resistors of the two outputs, set up the quiescent current of the output stages of each amplifier.

Compensation

The capacitors C_5 and C_7 (from the output of each amplifier to ground) provide the compensation for stability and optimum frequency response of each amplifier section.

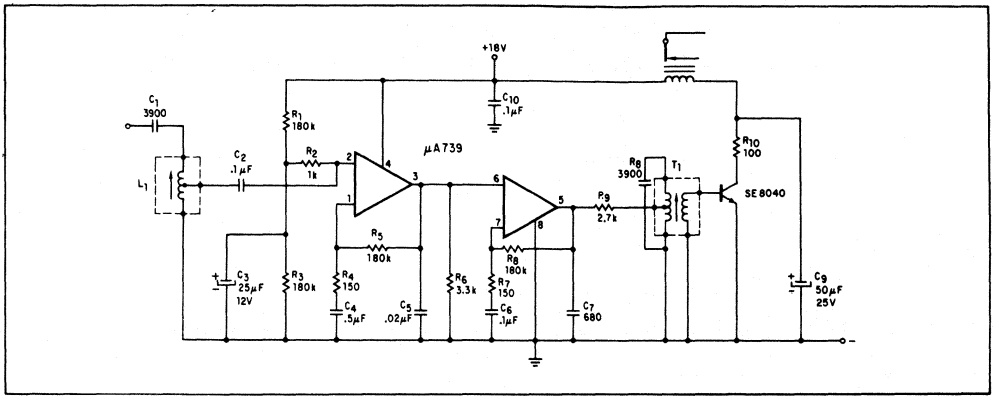


Fig. 11. TV remote control receiver.

A-C Considerations

Figures 12A and 12B show the untuned frequency response. The frequency range in this circuit is 8kHz to 60kHz, and the operating range of the tuned circuits is 20kHz to 50kHz. In order to minimize the noise output and leave the frequencies above 20 kHz unaffected, the frequency response has been rolled off below 10kHz.

Due to the low output impedance of the amplifier, the output transformer is driven through load resistor R_9. This arrangement gives an optimum signal-to-noise ratio. A mismatch of the output of the second stage into the output transformer causes a 15dB loss in the overall gain but results in a lighter loading of the transformer, a higher Q, and a better signal-to-noise ratio.

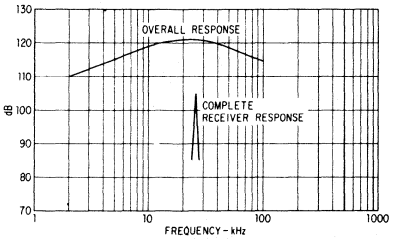


Fig. 12A. TV remote control amplifier.

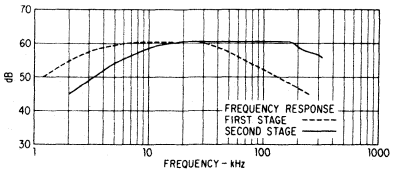


Fig. 12B. TV remote control amplifier.

Circuit Performance

The performance of the circuit satisfies all requirements for reliable operation. It has excellent signal-to-noise ratio and high sensitivity over a wide range of temperature and supply voltages. Table 3 gives the performance measurements of the receiver.

TABLE III.
T.V. Remote Control Receiver.

Gain at 25 kHz	121dB	without tuned circuits
Gain at 25 kHz	121.6dB	at 0°C
Gain at 25 kHz	120.2dB	at 70°C
Gain at 25 kHz	105dB	with tuned circuits, measured at base of relay trans.
Sensitivity for		
relay on at 26 kHz	4μV	18 V supply
relay off at 26 kHz	5.1μV	18 V supply
relay on at 26 kHz	5μV	14 V supply
relay off at 26 kHz	7.8μV	14 V supply
relay on at 26 kHz	4μV	24 V supply
relay off at 26 kHz	5.1μV	24 V supply
Noise output	25mV	measured at the base of relay transistor.
Bandwidth 3dB	1kHz	
S/N Ratio	25dB	at sensitivity Level

T_1 L = 10mH, Q loaded = 35, Turns ratio = 1:15, Tap at 15% — L_1 = 10mH, Tap at 15% — Magnavox #360964-1

Magnavox #360944-1 or equivalent

THE μA739
A LOW-NOISE DUAL OPERATIONAL AMPLIFIER

INTRODUCTION

The μA739 is a dual monolithic integrated circuit operational amplifier designed for low-noise industrial signal processing equipment and for preamplifiers in consumer home entertainment equipment. Designed as a low-cost building block, it has performance features that make it attractive in both industrial and consumer systems. Low package count, low power consumption, excellent noise figure, gain stability, and economy are its major features.

This paper describes the circuit and operating characteristics of the μA739 and covers the following topics: d-c circuit performance, low-frequency analysis, power consumption, noise, short-circuit protection, amplifier isolation, and compensation techniques.

D-C CIRCUIT PERFORMANCE

The μA739 consists of two identical operational amplifiers on a single chip, sharing a common bias supply. Each amplifier is a mirror image of the other. In this section, we will consider the bias circuit and one amplifier. (See Figure 1A.)

The amplifier consists of three gain stages: a differential input stage; a differential in, single-ended out second-stage; and a class A composite PNP/NPN output stage.

Transistors Q_1 and Q_2 form the differential input pair with Q_3 acting as a current source. Bias for the base of Q_3 is obtained from the combined V_{BE} drops of D_5 and D_6. Assuming for the moment that $V_{BE} = 0.6V$ for all transistors and diodes, it is clear that the voltage across R_3 is 0.6V, and hence the current in R_3 is 200 μA. This current divides equally between the collector loads R_1 and R_2 causing a voltage drop of 1 volt across each load resistor. Consequently, the collector voltages of both Q_1 and Q_2 are V_A - 1 volts.

The transistor differential pair, Q_4 and Q_5, is supplied by the current source Q_6, which derives its bias from the same point as Q_3. This current source delivers 350 μA and (assuming perfect matching and negligible Early effect) divides equally between Q_4 and Q_5. If the base current of Q_7 can be neglected, the collector voltage of Q_5 will be V^+ -1.6V.

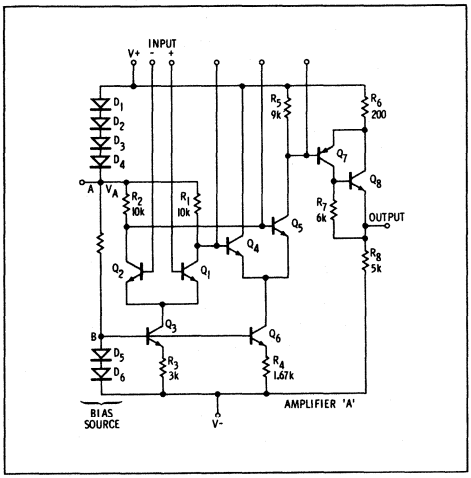


Fig. 1A. μA739 Amplifier 'A' with bias source.

We must now consider the worst case collector base reverse bias voltages on Q_4 and Q_5. If a large positive differential voltage is applied to the amplifier input, the entire current from Q_3 (200 μA) will pass through Q_1, and Q_2 will be off. The collector voltages of Q_1 and Q_2 will then be:

$$V_{C1} = V_A - 2V$$

$$V_{C2} = V_A$$

Q_5 will be turned fully on, since its base will be 2 volts higher than the base of Q_4. Under these conditions, saturation of Q_5 is prevented by the four diodes, D_1 through D_4. The highest voltage then appearing on the base of Q_5 is V^+ -2.4V.

FAIRCHILD
SEMICONDUCTOR

With a 30V supply and 200 μA in R_5, the output stage saturates when Q_5's collector is 1.8 volts below V^+. The reserve current from the 350μA source is 150 μA. This reserve current is available to drive the maximum base current of pnp transistor Q_7. Thus, the collector potential of Q_5 cannot fall below its base potential.

The output stage, which consists of the composite PNP combination, Q_7 and Q_8, brings about level translation. A single integrated lateral PNP device, such as Q_7, would not do the job here since it does not furnish adequate h_{FE}. By adding Q_8, one gets the necessary gain without changing the basic structure of the class A common emitter output stage. Figure 1B shows how h_{FE} is increased. R_7 is added to Q_7's collector load in order (1) to decrease the loop gain and phase shift in the local feedback loop of the composite PNP device, and (2) to increase slew rate.

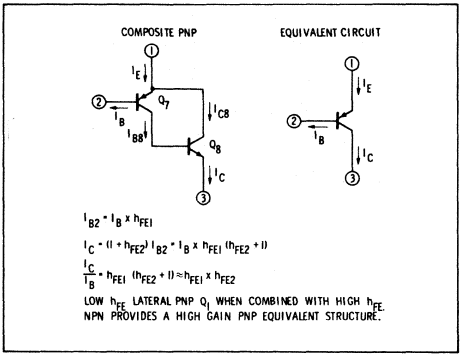


Fig. 1B. Composite PNP Configuration.

LOW FREQUENCY GAIN

First stage gain A_{V_1}

The gain of the first stage is given by $g_m R_L$, where $g_m = 40I_e$ (I_e in mA) and R_L is the parallel combination of the load resistance and the input impedance of the next stage.

$A_{V_1} = g_{m1} R_L$

$g_{m1} = 40 \times 0.1 = 4.0$ mA/V

input impedance of second stage $\approx 2\beta r_{e_2} \approx 16k\Omega$

load resistance (R_1 and R_2) = 10kΩ

$R_L \approx 6.2k\Omega$

$A_{V_1} \approx 4.0 \times 6.2 = 25$

Second stage gain A_{V_2}

The gain of the second stage is given by 1/2 $g_m R_L$. (The factor of 1/2 is needed for a single-ended output).

$A_{V_2} = g_{m2} R_L$

$g_{m2} = 40 \times 0.175 = 7.0$ mA/V

input impedance of the third stage $\approx \beta (Q_7, Q_8) \times R_6 \approx 40k\Omega$

load resistance (R_5) = 9kΩ

$R_L \approx 7.4k\Omega$

$A_{V_2} \approx 1/2 \times 7.0 \times 7.4 = 26$

Third stage gain A_{V_3}

The output stage gain is given by the ratio R_8/R_6, and in this case is 25.

To summarize the low frequency gain, we have:

$A_{V_1} = 25$, $A_{V_2} = 26$, $A_{V_3} = 25$

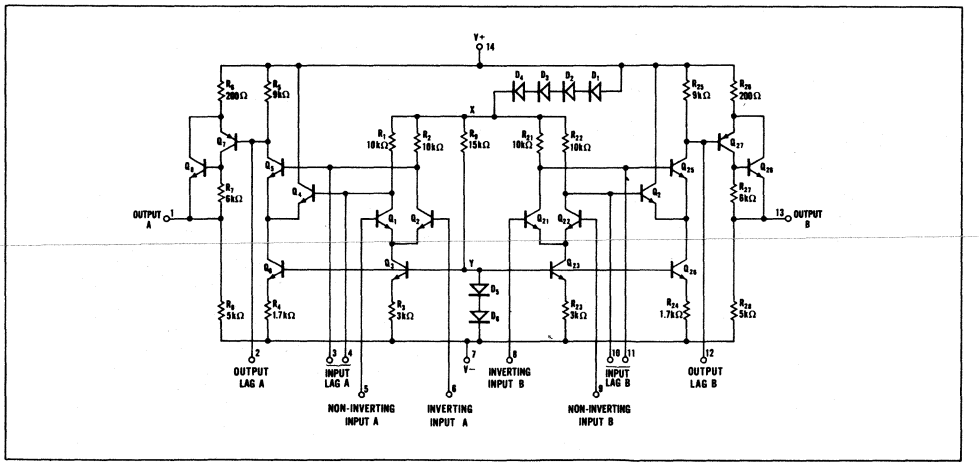


Fig. 1C. μA739 circuit diagram.

Total gain from input to output is, therefore:

$$A_{VO} = 25 \times 26 \times 25 = 16{,}250 \text{ or } 84 \text{ dB (Typical)}$$

Note that this gain is relatively constant for wide variations in absolute value of the individual resistors in the circuits. This comes about in the first two stages owing to the proportionality of g_m to emitter current, which is in turn inversely proportional to the resistor in the emitter of the current source. Therefore, the ratio of current source resistor value to collector load resistance determines the gain. The gain of the output stage is also dependent upon resistor ratios.

Calculation of the full temperature and supply voltage dependence of the gain is a lengthy procedure and is not included here. The measured variation of gain with temperature and supply voltage is shown in Figure 2A and 2B.

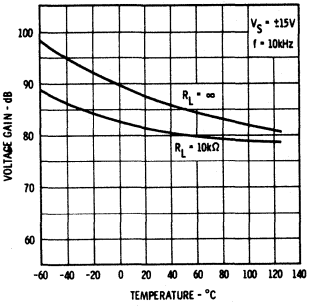


Fig. 2A. Uncompensated open loop gain as a function of temperature.

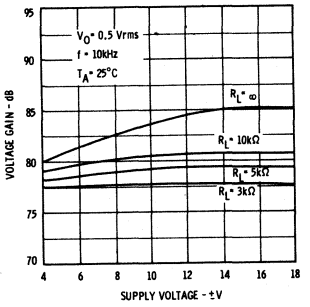


Fig. 2B. Uncompensated open loop voltage gain as a function of supply voltage.

BIAS STABILITY & SIGNAL HANDLING CAPABILITY

Offset voltage is also a function of temperature and supply. Input bias current and offset current are shown as functions of temperature and supply in Figure 3 and 4. The bias scheme used in the μA739 gives excellent gain stability and enables the

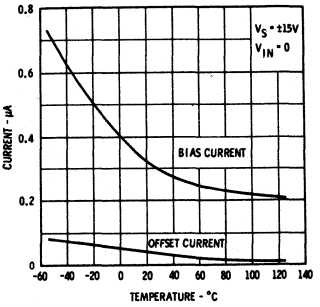


Fig. 3. Input offset current and bias current as functions of temperature.

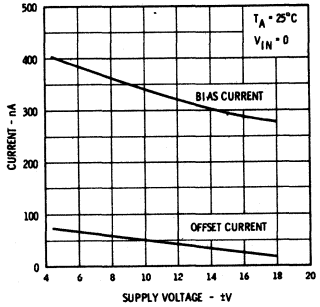


Fig. 4. Input offset current and bias current as functions of supply voltage.

amplifier to be operated at supply voltages between 9 V and 36 V. The common mode range is limited to the base voltage at Q_3 ($2V_{BE}$) and the collector voltage of Q_1 and Q_2 ($V^+ - 4V_{BE} - 1$). Thus, for operation at ±15 volts, the common mode range may be exceeded without causing latch-up. Common mode range is shown in Figure 5.

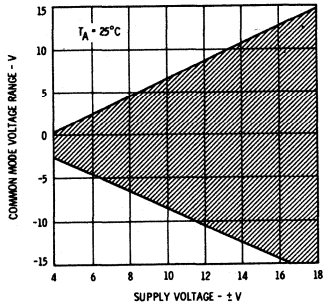


Fig. 5. Common mode range as a function of supply voltage.

The output swing is limited to within 2.5 volts of the supply in the positive direction by (1) the saturation voltage of Q_8 and (2) the voltage across R_7, i.e., +12.5 volts for a +15-volt supply. Negative output swing is limited by the load on the output. Output swing is given in Figures 5, 6A, and 6B.

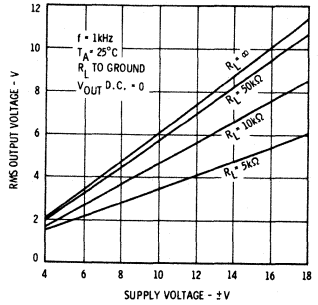


Fig. 6A. Output capability as a function of supply voltage.

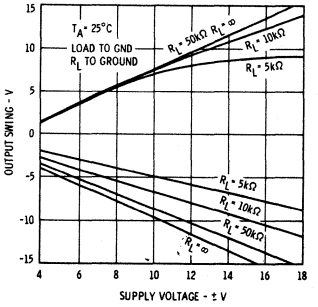


Fig. 6B. Typical output voltage swing as a function of supply voltage.

POWER DISSIPATION

Typical dissipation of the μA739 with a 30-volt supply is 350 mW. Figure 7A shows the variation of total supply current for different load resistances and supply voltages; Figure 7B gives the variation of supply current with temperature; and Figure 7C gives the device dissipation as a function of load resistance and supply voltage. These specifications are for an output voltage halfway between the positive and negative supplies — the normal quiescent mode in a linear amplifier circuit. The maximum permissible dissipation for the package is 500 mW derated linearly at 7.7 mW/°C above 60°C.

SHORT CIRCUIT PROTECTION

Short circuit output current is limited by the available drive. Consider the case where the output terminal is shorted to the negative supply. Maximum output current exists when the entire collector current of Q_6 passes through R_5. This assumes infinite h_{FE} for the output composite PNP, a worst case for this mode. The voltage across R_5 will be 4.1 volts, and the voltage across R_6 will be 3.4 volts.

The maximum current in R_6 and into the short circuit is therefore 17 mA. Dissipation in Q_8 when operating from ±15 volts will be approximately 460mW — close to the maximum for the package. A continuous short circuit would raise the temperature about 60°C.

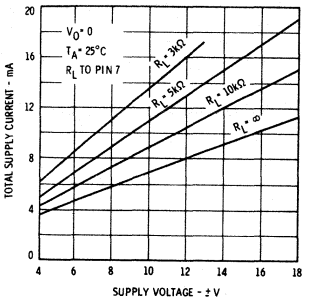


Fig. 7A. Total supply current as a function of supply voltage.

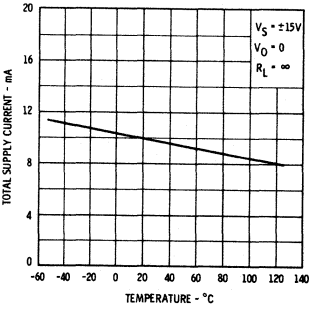


Fig. 7B. Total supply current as a function of temperature.

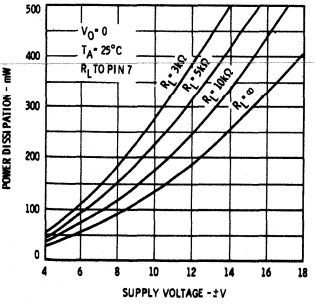


Fig. 7C. Total circuit dissipation as a function of supply voltage and load.

No damage will occur to the device under these conditions for normal ambient temperatures. Simultaneously shorting both outputs, however, could raise the chip temperature above the maximum allowed for the package, with the possibility of mechanical failure as a result.

CHANNEL ISOLATION

Figure 1C shows how the second channel of the μA739 is added to the channel we have just been considering. Any signal emanating from a channel to the bias circuit will be attenuated by the common mode rejection. It will then be further attenuated by the low impedances at X and Y (Figure 1C) and will appear at common mode points in the other channel. The isolation at 1 kHz will be at least equal to the combined common mode rejections of the two amplifiers. At very high frequencies, most of the coupling will be between the device leads and the accompanying circuit wiring. At low frequencies, inadequate power supply and bias decoupling may reduce the isolation. And, at very low frequencies, thermal coupling across the chip will cause some slight interaction.

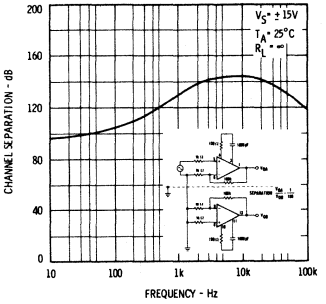


Fig. 8. Channel separation as a function of frequency.

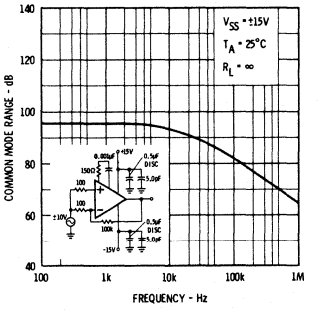


Fig. 9. Common mode rejection as a function of frequency.

These effects are illustrated in Figure 8. Channel isolation is so dependent upon external circuit and signal conditions that it is difficult to give a precise specification for this parameter. Figure 8 demonstrates that the isolation is entirely adequate for most operations. Figure 9 shows common mode rejection as a function of frequency.

NOISE

The choice of input stage collector current depends upon the source impedance for which the circuit is to be optimized. High source impedances call for low collector currents in order to keep noise current down; low source impedances require low emitter resistances and therefore higher collector currents for lowest noise voltage. For best signal-to-noise ratio, the noise figure is optimized for low-impedance sources(500Ω to 50kΩ). Spot noise voltage and current are plotted in Figures 10A and 10B, and wideband noise voltage and current are plotted in Figures 11A and 11B.

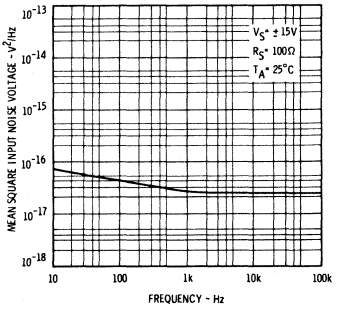


Fig. 10A. Input noise voltage as a function of frequency.

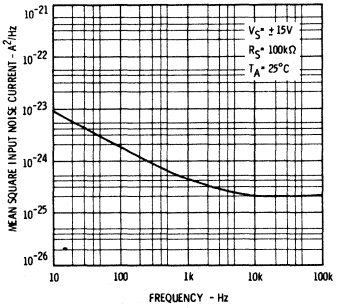


Fig. 10B. Input noise current as a function of frequency.

Other sources of noise are 1/f noise and "popcorn" noise. In particular, "popcorn" noise (also termed "burst" noise or "multi-state" noise) is most objectionable. Frequently encountered in bipolar semiconductor devices, it is characterized by discrete pulses superimposed on the normal wideband noise. The amplitude of these pulses is generally constant, while the frequency and length are completely random. "Popcorn" noise is probably caused by recombination effects at the silicon chip surface and is most prevalent at low temperatures with high source impedances. Process improvements applied to the μA739 have resulted in reduced "burst" and 1/f noise.

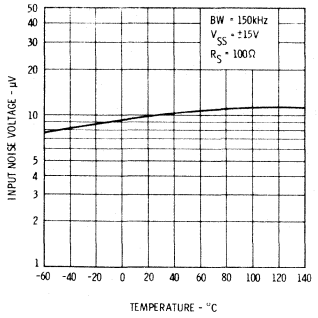


Fig. 11A. Wide band noise voltage as a function of temperature.

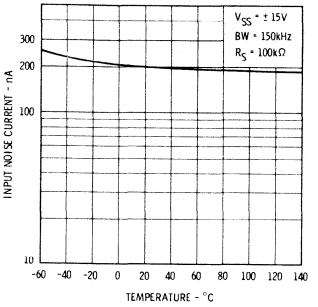


Fig. 11B. Wide band noise current as a function of temperature.

COMPENSATION

Compensation of the μA739 can be tailored to each individual circuit. For a given application, output voltage swing and closed loop gain determine the compensation required.

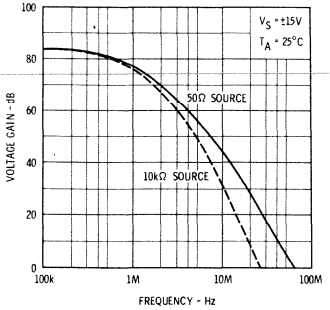


Fig. 12A. Uncompensated open loop frequency response.

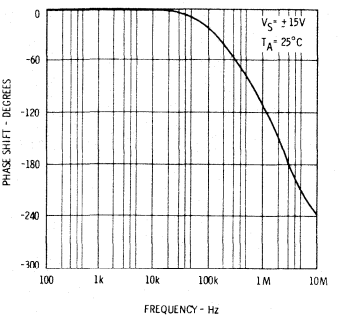


Fig. 12B. Open loop phase shift without compensation.

The open loop gain and phase responses are plotted in Figure 12. The dominant pole at 600 kHz is caused by the transit delay in the lateral PNP. Two other major poles at 1 MHz and 2 MHz are caused by the phase shift at the collectors of the differential gain stages. For very high source impedances, the input capacitance will add a pole as shown by the dashed line in Figure 12. Variation of 180° phase shift frequency with supply voltage is shown in Figure 13. The compensation networks given apply over the voltage range of 8V to 30V.

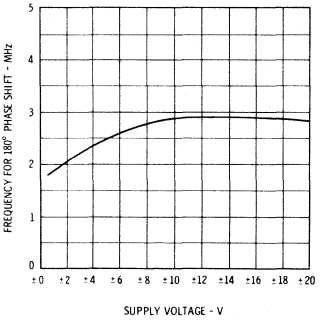


Fig. 13. Open loop 180° phase shift frequency as a function of supply voltage.

For many applications, a single capacitor is sufficient to ensure stability of the circuit. Single component compensation can be accomplished between pin 1 and ground, between pin 3 and pin 4, and from pin 2 to either supply or ground. If compensation is used to shunt pin 2, the compensation should go between pin 2 and pin 14 (V^+) rather than between pin 2 and ground. Examination of the output circuit in Figure 1C indicates the reason for this. If the capacitor is grounded, signals on the power supply are amplified through the output stage (as in a common base circuit), and the result is reduced high frequency power supply rejection. If, however, the capacitor is placed between pins 2 and 14, high frequency power supply signals become a common mode input to the output stage.

Frequency response for various capacitor values are shown in Figures 14A, B, and C.

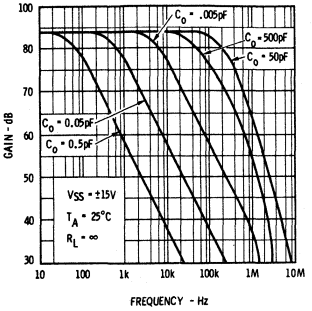


Fig. 14A. Frequency response output compensation - pin 1 to ground.

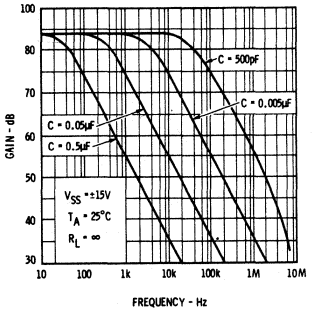


Fig. 14B. Frequency response second stage lag compensation — pin 2 to pin 14.

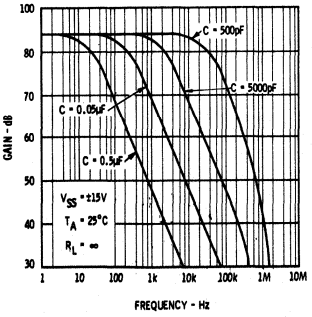


Fig. 14C. Frequency response input compensation — pin 3 to pin 4.

Feedback compensation can be used to control the amplifier frequency response. Capacitors can be placed between pins 1 and 2, or 2 and 3. Compensation around the output stage is similar to lag compensation from pin 2 to pin 14; the capacitor value is smaller, and the pole caused by the output stage is better controlled in the region from 0.1 MHz to 1 MHz. Second stage feedback compensation converts this stage to a voltage follower. An advantage of this compensation is that it produces both a pole and a zero in the forward response. The amount of attenuation inserted is equal to the second stage gain plus 6 dB. Frequency response of the μA739 for feedback compensation is shown in Figure 15A and 15B.

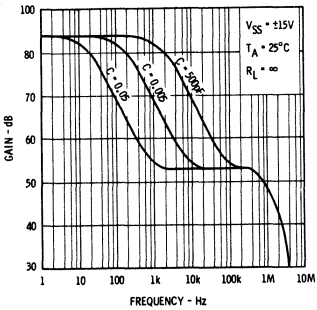


Fig. 15A. Frequency response with second stage feedback compensation — pin 2 to pin 3.

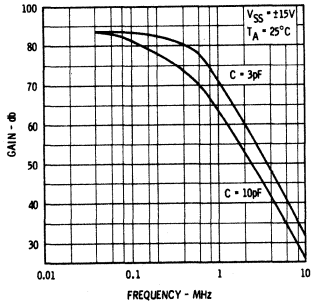


Fig. 15B. Frequency response output stage feedback — pin 1 to pin 2.

Unity gain compensation for phono preamplifiers, integrators, and most d-c applications requires compensation around more than one stage for adequate phase margin. For applications where slew rate is not a factor, output compensation combined with second stage feedback compensation (Figure 16A) can be used for minimum parts count. For maximum output swing, input compensation and feedback compensation around the output stage will give 60° of phase margin with 3V/μs slew rate. Phase lead must be included in the input compensation as shown in Figure 16B.

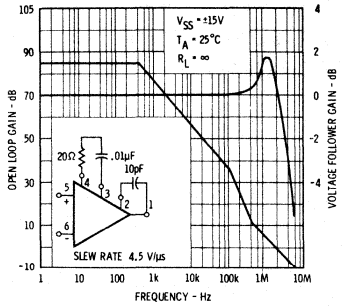


Fig. 16A. Low slew rate unity gain frequency response.

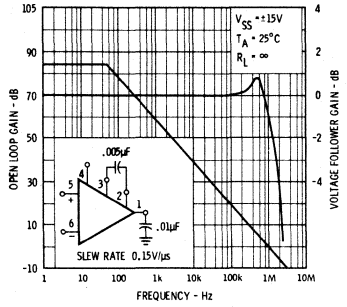


Fig. 16B. Maximum slew rate unity gain frequency response.

The slew rate can be predicted for any value of capacitor. Figure 17 gives the slew rate versus capacitance for the compensation networks indicated. This may be calculated from the equation

$$\text{Slew Rate} \quad S = I/C\ A$$

where I is the available current to charge the compensating capacitor, C is the capacitor value, and A is the gain from the compensating point to the output. For example, if .01μF is used between pins 3 and 4 and I = 200μA, A = 25.7 x 25, and S = 12.8 V/μs.

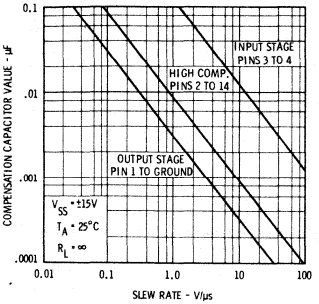


Fig. 17. Maximum slew rate for various compensations.

OPERATING SAFEGUARDS

When connecting the μA739 in a circuit, attention should be given to proper orientation. If the μA739 is installed in reverse, V^+ and V- will be interchanged, excessive currents will flow in the substrate diode, and the IC may be damaged.

When using the μA739, bypass capacitors should be connected from the supply terminals to ground to eliminate the effects of power supply lead inductance. A 0.01 μF disc mounted close to the IC pin provides enough decoupling to eliminate the effects of this inductance.

CONCLUSION

The μA739 dual low-noise amplifier provides two well-isolated operational amplifiers in a single package. Each amplifier features high open-loop voltage gain over a wide range of supply voltages and good thermal stability.

External frequency compensation enables the amplifier to be used in applications ranging from DC through audio and up to ultrasonic frequencies. Common mode range and output swing are high and latch-up is prevented.

A MARKER BEACON AND INDICATOR USING INTEGRATED CIRCUITS

INTRODUCTION

A marker beacon receiver (Figure 1) is a specialized airborne receiver that tunes only one frequency (75 MHz) and is operated at very short range—typically 1600 feet for the outer marker, 300 feet for the middle marker, and up to 40,000 feet for the "Z" marker. Since antenna signal strength is high at these ranges, receiver sensitivity requirements are not demanding. Receiver and display selectivity must be adequate to ensure that the set will not be accidentally triggered by television signals whose frequencies are close to 75 MHz.

Many marker designs are currently available, two of the most common being TRF and single conversion. Circuit complexity varies. Some circuits use a single tube with only an audio output, while other circuits have over 10 transistors and automatic photosensor lamp dimming. Sensitivities range from about 50 μV to 1 mV; selectivities range from around 200 kHz to more than 2 MHz.

This paper describes a marker beacon receiver and display. Three topics are covered:

The design of a superheterodyne receiver using AGC transistors and an IC IF amplifier (the μA719)

The design of tone filters and lamp drivers using op amps (the μA739 and μA741) in active filter configurations

A digital tone discriminator and lamp driver design using MSI circuits (the 9300 shift register and the 9301 one-out-of-ten decoder)

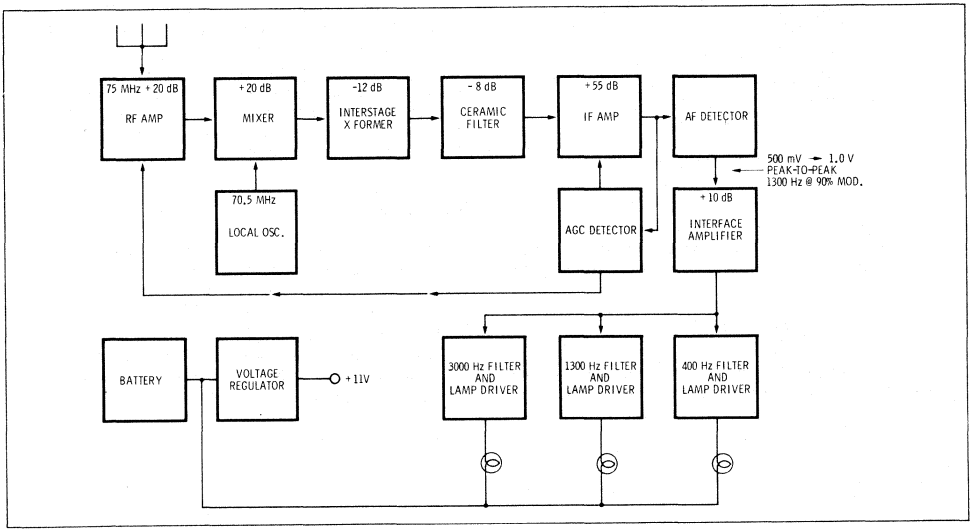


Fig. 1: Block Diagram Marker Beacon Receiver.

FAIRCHILD
SEMICONDUCTOR

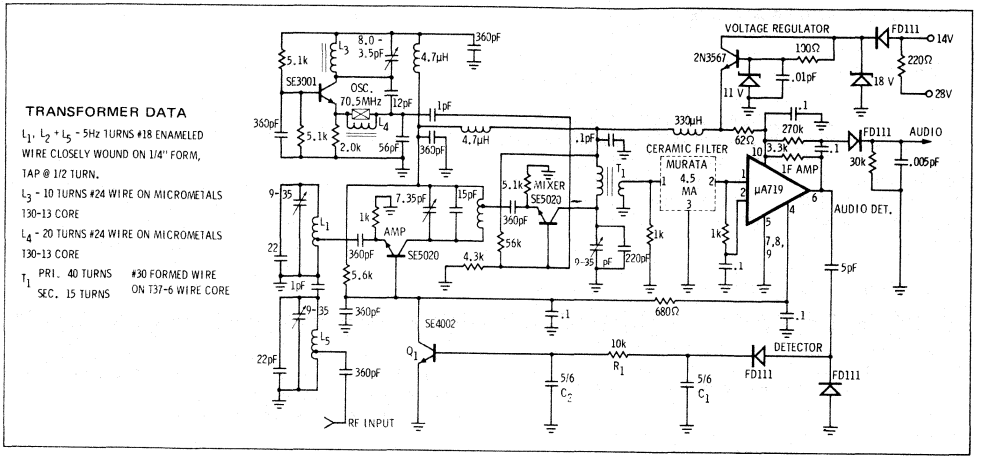


Fig. 2: A Single-Conversion Superheterodyne Receiver.

SUPERHETERODYNE RECEIVER

A Single-conversion superheterodyne receiver is illustrated in Figure 2. The RF amplifier is a common-base stage with tuned circuits in the emitter and collector. Each of these tuned circuits has a loaded Q of about 100. AGC is achieved by reducing the collector current.

The crystal-controlled local oscillator was designed using the method suggested by Cote. [1,2] Inductor L_4 tunes out the crystal holder capacitance and ensures operation on the desired overtone.

In the common-base mixer, the RF signal is applied to the emitter, and the local oscillator signal is fed to the base. Transformer T1, which is tuned to the IF frequency, matches the impedance of the collector circuit to the ceramic IF filter. The latter is loaded with 1 kΩ on the input of the μA719, an IF amplifier that provides a gain of 55 dB with a 3.3 kΩ resistive load. (With a tuned load, 75 dB gain is possible.)

An IF frequency of 4.5 MHz was chosen to force the image frequency to be 66 MHz. Figure 3 shows VHF frequency allocations near 75 MHz. Since the local oscillator is 4.5 MHz below 75 MHz, the image is 4.5 MHz below 70.5 MHz—that is, at 66 MHz. Note that TV channels 3 and 4 are separated at 66 MHz. This separation should make 66 MHz a "quiet" frequency.

Diodes serve as the audio detector and the AGC detector. Q_1 is the AGC amplifier; R_1, C_1, C_2 constitute the AGC filter. (See Figure 2.) Reverse AGC is applied to the RF amplifier and the μA719 IF amplifier.

The performance of the superheterodyne receiver is given in Table 1 In Appendix A, and Figure 4.

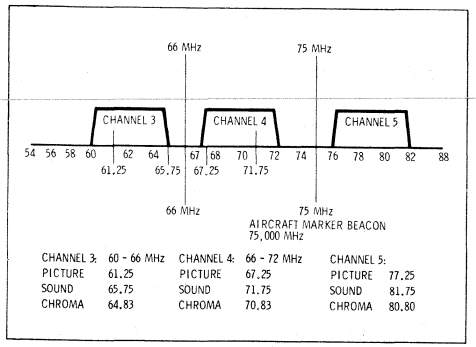


Fig. 3: VHF Frequency Allocations Near 75 MHz.

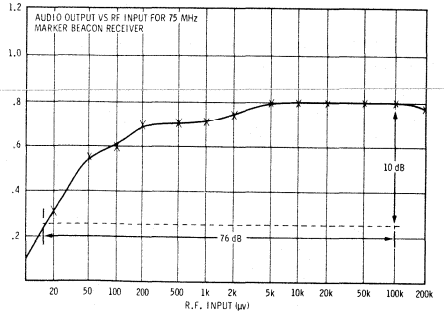


Fig. 4: Audio Output vs RF Input for 75 MHz Marker Beacon Receiver.

TONE FILTERS AND LAMP DRIVERS

General Discussion

Tone filters are required for 400 Hz, 1300 Hz, and 3000 Hz. Although most current marker beacon designs still use an ordinary LC circuit for tone filtering, the best type of tone filtering circuit for this application is a multiple feedback active bandpass filter. (Mechanical filters and digital tone discriminators offer no advantages and are rarely, if ever, used.)

A multiple feedback active bandpass filter whose feedback loop contains an RC network can be seen in Figure 5. In this circuit, the center frequency can be easily adjusted by a single variable resistor (R_2), thus eliminating the need for costly close-tolerance (1%) components. It is this feature that makes this type of filter ideal for marker beacon applications.

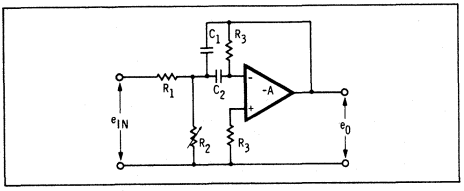


Fig. 5: Multiple Feedback Path Active Bandpass Filter.

The design equations for a multiple feedback path active filter are given below: (see reference 3).

$$K = \frac{c}{2\pi f_o}$$

$$\alpha = \frac{1}{Q}$$

$$H = \frac{|A_o|}{Q}$$

Resistor values are determined from the following equations:

$$R_1 = \frac{1}{HK}$$

$$R_2 = \frac{1}{(2Q-H)K}$$

$$R_3 = \frac{2Q}{K}$$

A simple Super Basic program that can be used to calculate the resistor values required in the active filter.

Example

want: $f_o = 400$ Hz
$Q = 10$
$A_o = 6$

Choose: C = .01 μFd. The value of C is chosen on a cut-and-try basis. A reasonable value of C is one that is significantly larger than the circuit stray capacitance and which also leads to reasonable values for the resistors.

The Super Basic program is listed below. One advantage of using a computer to calculate the resistor values is that it is almost painless to make several trial runs and then look at the values of resistors and capacitors to see if they are sensible in light of other circuit requirements, such as stray capacitance and input current to the operational amplifier.

Program

```
-SBASIC

>TAPE
10 PRINT "TYPE A0, Q1, F0, C1,"
20 INPUT A0, Q1, F0, C1
25 K = 2*PI*F0*C1
28 PRINT "K = ", K
30 H = A0/Q1
33 PRINT "H = "; H
35 R1 = 1/(H*K)
40 R2 = 1/((2*Q1 - H)*K)
45 R3 = 2*Q1/K
48 PRINT
50 PRINT R1; "= R1", R2; "= R2", R3; "= R3"
```

Sample Run

```
>RUN
TYPE A0, Q1, F0, C1,
? 6, 10, 400,.01E-6
K =              2.5132741E-05
H =     .6

 66314.56 = R1  2050.9658 = R2  795774.72 = R3
```

Rounding off the values

$R_1 \simeq 68K$

$R_2 \simeq 2K$ use 2.5K pot

$R_3 \simeq 750K$

The availability of low cost, low voltage IC operational amplifiers makes active filters practical in marker beacon tone filters.

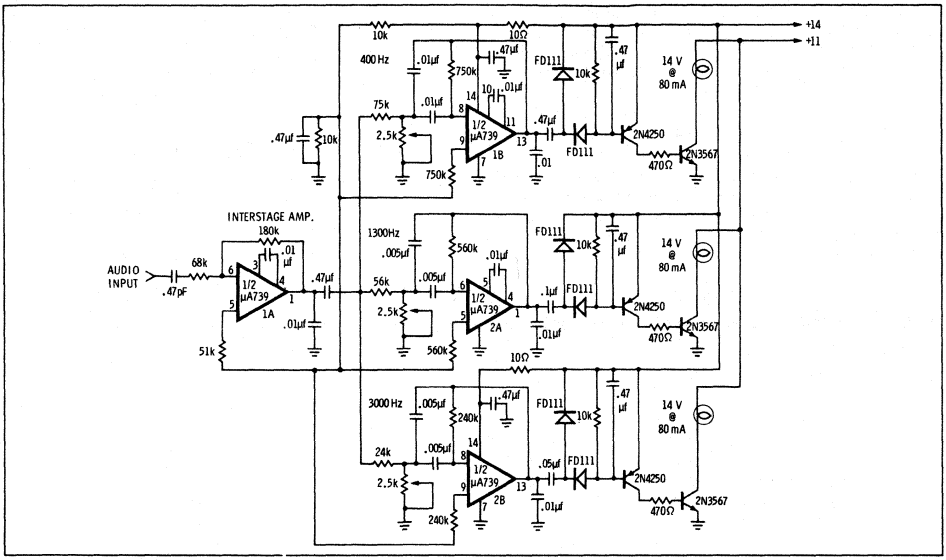


Fig. 6: Marker Beacon Display Circuit Using μA 739 Operational Amplifiers.

Tone Filters and Lamp Drivers Using the μA739

Figure 6 is a schematic of a three-light marker tone filter and lamp driver. Two μA739 dual operational amplifiers in the tone filter amplifier section 1A act as an impedance transformer/line driver. Amplifiers 1B, 2A, 2V are multiple-feedback-path active bandpass filters. Amplifier 1B is tuned for 400 Hz, a gain of 6, and a Q of 10. Amplifier 2A is tuned for 1300 Hz a gain of about 5, and a Q of about 10. Amplifier 2B is tuned to 3000 Hz, a gain of about 5, and a Q of about 10.

The tone filter outputs are capacitively coupled to the lamp drivers. The tone input is clamped to the +11V by one diode and pulse stretched with the other diode and a 0.47 μFd capacitor. Transistor 2N4250 is a driver for the 2N3567, which serves as a switch. The lamp is rated at 14V and 80 na.

Tone Filters and Lamp Drivers Using the μA741

With the internally compensated μA741, it is possible to build a tone filter that has a minimum of external components. The μA741 amplifiers are packaged as single units which makes it possible to design a simple lamp driver circuit.

The audio output from the detector circuit (Figure 7) is amplified by a common-emitter stage (SE4002) with a voltage gain of approximately three. The amplified signal drives the three tone filters, which are connected in parallel, and the output terminal of each operational amplifier is "strapped down" through a capacitor. When a signal of the proper frequency is applied to a tone filter, the power supply current to the amplifier increases, causing a voltage to be developed across the 330-ohm resistor in series with the negative supply lead of the μA741 (pin 4). When the voltage across the 330-ohm resistor exceeds the V_{be} of the 2N3567, the lamp is activated.

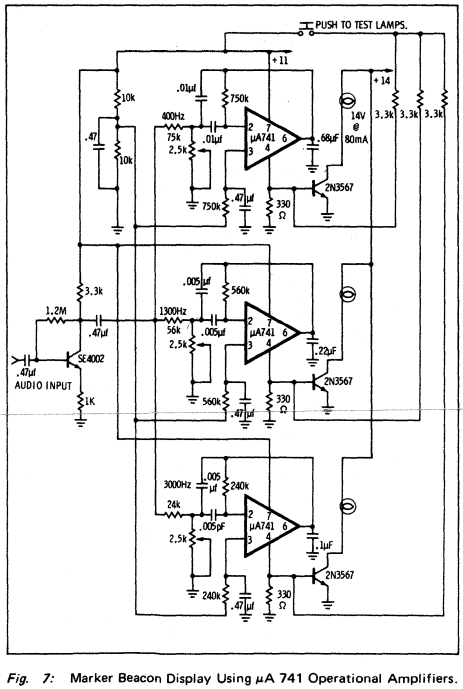


Fig. 7: Marker Beacon Display Using μA 741 Operational Amplifiers.

W

The circuit has been temperature tested from −55°C to +85°C and performs satisfactorily. The temperature coefficient of the resistors and capacitors in the tuning network must be appropriate for the desired operating temperature range.

Digital Tone Discriminator and Lamp Driver

The circuit consists of a tone-squaring circuit, a 10.4 kHz oscillator, two 9300 4-bit shift registers, and a one-out-of-ten decoder. One 9300 is used as a counter, the other as a holding register. The circuit block diagram is shown in Figure 8, and the circuit schematic is shown in Figure 9.

The operation of the digital tone discriminator illustrated in Figure 9 is as follows:

1) The input tone is squared.

2) The inverted tone activates the PE, (Parallel Enable) and when the clock pulse goes high, the counter is set to its initial condition–which is 0101. The 0101 is a wired "program" connected to inputs P0, P1, P2, and P3 of the 9300 counter.

3) The counter remains at 0101 as long as the inverted tone is low.

4) When the inverted tone goes high, the counter begins to count the 10.4 kHz clock pulses. The counting continues as long as the PE is high. The number of pulses accumulated in the counter is a function of the time of one-half the tone period.

5) The decoder provides a continuous decode of the state of the counter. These decodes of the counter's state are supplied as inputs to P0, P1, P2, and P3 of the holding register.

6) The holding register's PE is wired low, so that each time the CP goes high, the inputs to the holding register are transfered to the outputs: P0 to Q0, P1 to Q1, and P2 to Q2. The holding register will "hold" this state until the next CP occurs or the Master Reset goes low.

7) When the squared and inverted tone at the PE of the counter goes low, the counter loads 0101 when the clock goes high.

8) There is one gate delay between the normal and inverted tone. This delay time is used to load the holding register before the counter is reset.

9) A light will be on when its controlling signal from the holding register is high.

The timing diagram is illustrated in Figure 10.

Consider the following frequency-time relationships.

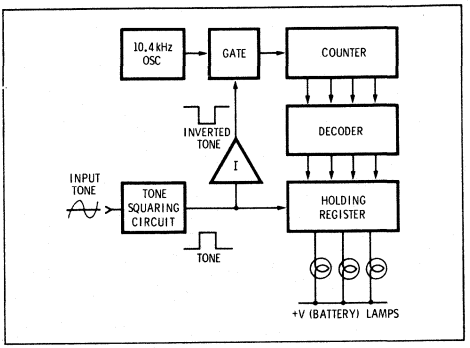


Fig. 8: Digital Tone Discrimination and Lamp Driver.

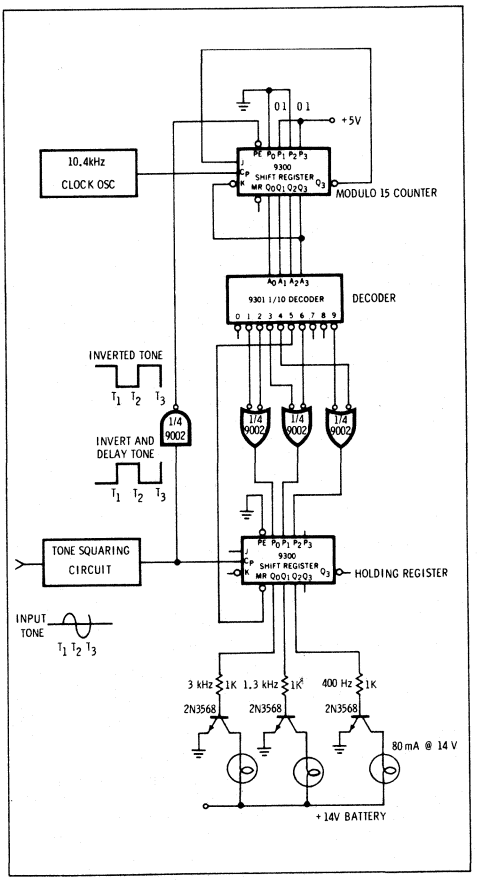


Fig. 9: Marker Beacon Tone Discrimination Circuit.

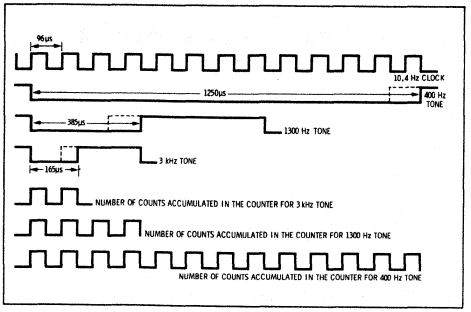


Fig. 10: Dotted Line Indicates the Amount the Period of the Tone could Vary and Still Be Decoded - The Circuit "Q".

$$\#CP_{/Period} \qquad \#CP_{/\frac{Period}{2}}$$

Clock Period = $T_{10.4\ kHz} = \frac{1}{10.4\ K} = 96\ \mu S$

Clock Period = $T_{400\ Hz} = \frac{1}{400} = 2.5\ mS = 2500\ \mu S$ $\quad \frac{2500}{96} = 26 \quad \frac{26}{2} = 13$

Clock Period = $T_{1300\ Hz} = \frac{1}{1300} = .77\ mS = 770\ \mu S$ $\quad \frac{770}{96} = 8 \quad \frac{8}{2} = 4$

Clock Period = $T_{3\ kHz} = \frac{1}{3K} = .33\ mS = 330\ \mu S$ $\quad \frac{330}{96} = 3.44 \quad \frac{3.44}{2} = 1.72$

Using a 10.4 kHz clock one-half the tone period, we obtain the following:

Tone	Number of 10.4 kHz Clock Pulses in One-Half the Period	Decode
400 Hz	13	12 & 13
1300 Hz	4	3 & 4
3000 Hz	1.72	1 & 2

Table 2, Appendix B, Illustrates the Counting Sequence of the Counter and the Decoded States.

REFERENCES

1. A. J. Cote, Jr. "Matrix Analysis of Oscillators and Transistor Applications". IRE Transaction on Circuit Theory, September 1958, P. 181, 188.

2. A. J. Cote, Jr. Correspondence, IRE Transactions on Circuit Theory, June 1959, P. 232, P. 233.

3. Handbook of Operational Amplifier Active RC Networks, Burr-Brown Research Corporation.

ACKNOWLEDGMENT

The authors wish to acknowledge the contributions of John Gregory in designing the digital tone discriminator.

TABLE 1 (APPENDIX A)

Marker Beacon Receiver Specifications

Usable Sensitivity: 50 µV

A G C Figure of Merit: 75 dB (100 mV reference)

Audio Output: 500 mV P-P @ 1300 Hz 90% Mod 50 µV input.

Bandwidth: (for 1300 Hz lamp to light)

1 mV input	400 kHz
10 mV input	800 kHz
100 mV input	3.5 MHz

I F rejection: 73 dB

Spurious rejection: >54 dB

Image rejection: 50 dB

TV Spectrum Interference: 60 mV input (simultaneously on all channels) causes no false triggering of lamps and each lamp still lights with a 100 µV input signal.

Power Consumption: 40 mA → 150 mA @ .14 V

TABLE 2, (APPENDIX B)

COUNTING SEQUENCE
OF THE COUNTER AND THE DECODED STATES

CLOCK PULSES	COUNTER				DECODE AND SEQUENCE
CP	P_0	P_1	P_2	P_3	
0	0	1	0	1	INITIAL STATE WIRED PROGRAM
1	0	0	1	0	
2	1	0	0	1	> 3 kHz DECODE
3	1	1	0	0	
4	0	1	1	0	> 1.3 kHz DECODE
5	1	0	1	1	
6	1	1	0	1	
7	1	1	1	0	
8	0	1	1	1	
9	0	0	1	1	
10	0	0	0	1	
11	0	0	0	0	
12	1	0	0	0	> 400 Hz DECODE
13	0	1	0	0	
14	1	0	1	0	DECODE MASTER RESET FOR HOLDING REGISTER

CONCLUSION

The design of a superheterodyne marker beacon receiver has been discussed. Active tone filter designs incorporating IC operational amplifiers give good performance and provide the designer considerable choice in the gain and Q of the circuit. The digital tone discriminator described here furnishes the designer an additional method of mechanizing a tone filter.

THE μA795, A LOW-COST MONOLITHIC MULTIPLIER

I. INTRODUCTION

This paper gives information helpful in setting up and optimizing the operation of analog multiplier circuits using the μA795. The circuits section demonstrates how to use the μA795 as a voltage-controlled amplifier, a modulator, a multiplier with level shift, a voltage-variable low-pass filter, and a squaring and frequency-doubling circuit. These circuits are intended to familiarize the user with some of the μA795's capabilities. The appendix contains a theoretical analysis of the operation of the μA795 Four-Quadrant Multiplier and shows how a group of exponentially non-linear devices can be interconnected to form a linear multiplier.

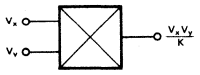


Fig. 1

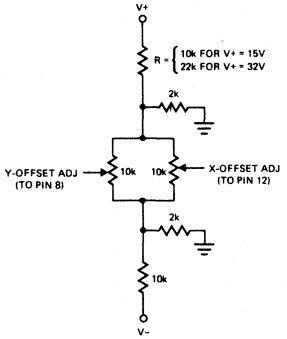


Fig. 2

II. FUNDAMENTAL EXPLANATION

The basic multiplier shown in Figure 1 has two inputs, V_X and V_Y, each of which can vary between +10 volts and −10 volts. Since this presents the possibility of a 10 times 10 or a 100 volt output, the device hookup includes a factor of 10 division called the K factor.

This allows the inputs to vary over their full range while maintaining reasonable power supply requirements.

III. NULLING TECHNIQUES

The circuit shown in Figure 2 provides the necessary X and Y offset adjustment voltages for all μA795 applications.

The following procedures provide two methods for zeroing a multiplier using normally available test equipment.

1. AC Method Using an Oscilloscope or AC Meter
   a. When using an operational amplifier for level shifting, ground the V_X and V_Y inputs of the μA795 and adjust the level shifter's offset-adjust potentiometer until the shifter's output is at zero volts.
   b. For initial balancing of all μA795 circuits, first ground V_X and apply a 1.0 kHz, 1.0 V (p-p) sine wave to V_Y. Adjust the x input offset-adjust potentiometer for minimum AC output voltage. Second, ground V_Y and apply the same sine wave to V_X. Adjust the y input offset-adjust potentiometer for minimum AC output voltage. Repeat steps 1a and 1b until a null is achieved.
   c. When using circuits having a K-factor-adjust attached to pin 3 of the μA795, apply 5.0 volts DC to both V_X and V_Y and adjust the K-factor potentiometer until the output voltage is 2.5 volts DC. For applications requiring high accuracy, check the setup adjustments by applying −5.0 volts DC to V_X and V_Y. If the output of the level shifter is not +2.5 volts DC, repeat steps 1a through 1c.

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2. DC Method Using a High-Accuracy Voltmeter
   a. Follow the procedure outlined in steps 1a through 1c above, with the exception that the 1.0 kHz, 1.0 V (p-p) sine wave mentioned in 1b should be replaced by a 5.000 volt DC source.

IV. FREQUENCY LIMITATIONS

The high-frequency performance of the μA795C is determined primarily by two conditions.

1. By the load resistors and the associated stray output capacitance of the multiplier.
2. By the operational amplifier used at the output.

For maximum frequency of operation, low value load resistors and a μA715 wideband high slew rate operational amplifier should be used.

Phase shift at higher frequencies (due to load resistors and output stray capacitances) and relative phase shift between x and y channels should be considered for maximum accuracy. As an example, if the input-to-output phase shift is only 0.6°, the output product of two sine waves will exhibit a vector error of 1%. A 3° relative phase shift between the input signals will result in a vector error of 5%.

The normal circuit precautions should be taken to avoid parasitic oscillation. Leads should be as short as possible and each power supply should be decoupled with a 0.1 μF high-frequency capacitor. An R-C parasitic suppression network consisting of a 510 Ω resistor in series with 10 pF capacitor from each input to ground can be used to reduce the Q of a source-tuned circuit (which may cause oscillation).

V. CIRCUITS

VOLTAGE-CONTROLLED AMPLIFIER – The circuit shown in Figure 3 offers a convenient method of controlling the gain of a system over a range of 100 or more simply by applying a positive control voltage to the V_C input. This control voltage may be either externally supplied or may originate internally from a closed-loop feedback system.

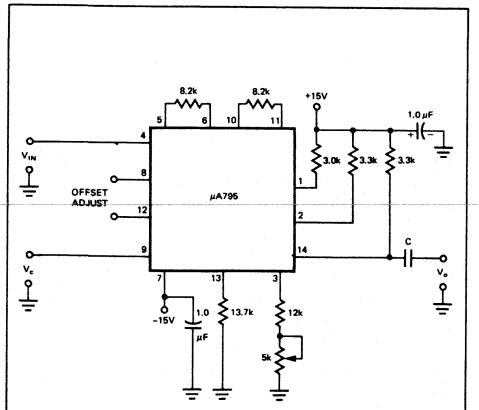


Fig. 3

Causing the control voltage V_C to go negative will invert the output and repeat the gain control range of 100 or more for the inverted output. The circuit as shown accepts inputs of ±5 volts peak amplitude on either the V_{in} or the V_C terminal. The output is:

$$V_o = \frac{V_{in}\, V_C}{10}$$

and this output is coupled by the capacitor, C, whose size is determined by the required frequency of operation.

Figure 4 demonstrates the excellent linearity available from the circuit. With a 1.0 kHz, 10 V (p-p) sine wave input, the output varies linearly over two decades.

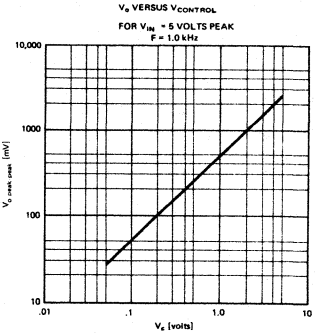


Fig. 4

This 40 dB of bipolar gain control finds many applications in AGC systems and wherever AC voltage control of gain is required.

The response of the multiplier is such that V_C may vary at any rate up to several hundred kilohertz.

MODULATOR – The modulator shown in Figure 5 is capable of both balanced modulation and amplitude modulation as a function of the position of the modulation index control.

With the wiper of the potentiometer at ground, the modulation index is zero. This gives double sideband suppressed carrier (balanced) modulation. Mathematically, this means that if:

$$V_Y = A \cos(\omega_m t)$$
$$V_X = B \cos(\omega_c t)$$

then the output voltage is:

$$V_o = \frac{AB}{10} \cos(\omega_m t) \cos(\omega_c t)$$

$$V_o = \frac{AB}{10} [\cos(\omega_m + \omega_c) t + \cos(\omega_m - \omega_c) t]$$

Note that the carrier frequency ω_c is completely missing from the output, as one would expect with balanced modulation.

Upward motion of the wiper introduces a DC term into the modulation V_Y input. The output is now an amplitude modulated waveform with close to 100% modulation. Further upward motion of the wiper causes a decrease in the percentage of modulation until, at the top, the modulation is about 3%. Defining the DC voltage term introduced by the potentiometer as D, the output becomes:

$$V_O = \frac{B}{10}[D + A\cos(\omega_m t)]\cos(\omega_c t)$$

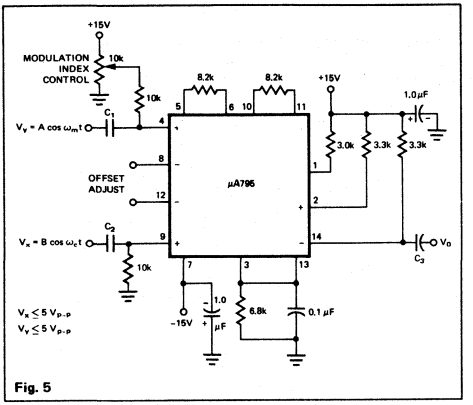


Fig. 5

Note that the carrier frequency ω_c now appears as an element of the output frequency spectrum. Figure 6 shows the two input waveforms and the resulting output waveform for a modulation index of 95%.

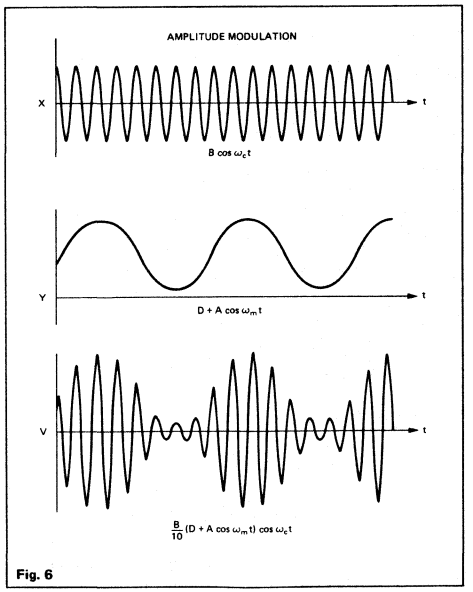


Fig. 6

MULTIPLIER WITH LEVEL SHIFT

The multiplier configuration shown in Figure 7 provides a DC level shift which causes the output to vary plus and minus with respect to ground rather than with respect to the +12 volt level observed in the circuit shown in Figure 5.

For applications requiring polarity reversals, either the V_X and x offset-adjust or the V_Y and y offset-adjust pin connections may be reversed due to the internal symmetry of the multiplier.

One application of the circuit shown in Figure 7 is the measurement of power. The V_X input receives a signal proportional to the instantaneous voltage across the load, and the V_Y input receives a voltage proportional to the instantaneous current through the load. The load voltage and current may be DC, AC sine waves, or any complex combination of frequencies, as long as the highest significant component frequencies are in the low megahertz region.

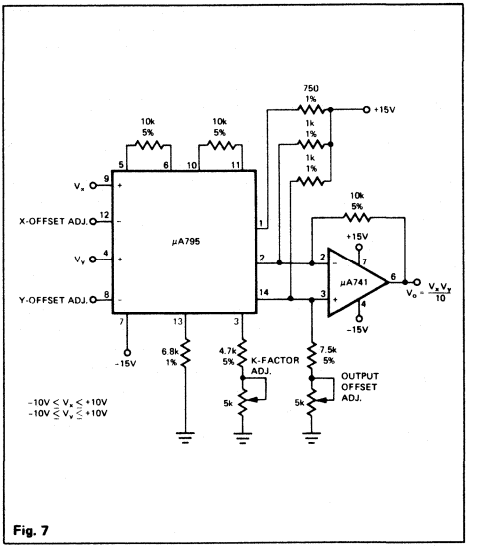


Fig. 7

The multiply with level shift circuit is one of the more popular circuit configurations for the multiplier and also provides one of the basic building blocks for DC closed-loop applications.

VOLTAGE-VARIABLE, LOW-PASS FILTER – A multiplier-with-level-shift circuit inserted in the resistance portion of an integrator feedback loop allows the DC control of a low-pass filter's break point. The f_2 or 3-dB-down rolloff frequency becomes a linear function of the control voltage V_c applied to the multiplier. Figure 8a shows the effect on the f_2 as V_c varies in the circuit shown in Figure 8b.

The transfer function of this circuit is derived as follows. From operational amplifier theory:

$$\frac{V_{in}}{R1} = -\left(\frac{V_o}{R2} + j\omega C V_X\right)$$

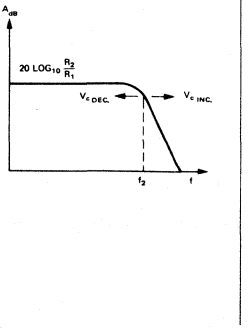


Fig. 8a

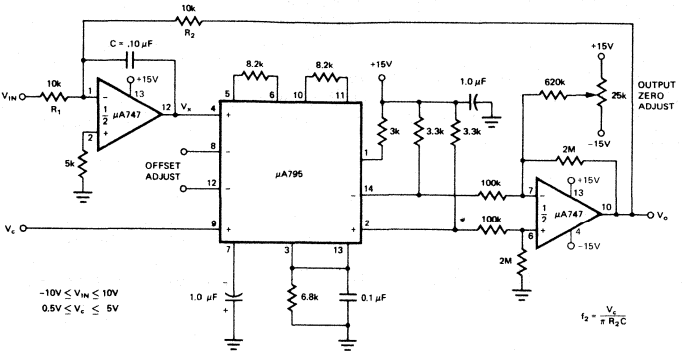


Fig. 8b

Since the level shifter in Figure 8b has a gain of 20, the output of the multiplier and level shifter is:

$$V_o = \left(\frac{V_X V_c}{10}\right) 20$$

Combining these two equations and eliminating V_X gives the net transfer function:

$$\frac{V_o}{V_{in}} = \frac{-R_2/R_1}{1 + j\,\frac{R_2\,\omega C}{2\,V_c}}$$

The 3-dB-down point of the transfer function is therefore:

$$f_2 = \frac{2V_c}{2\pi R_2 C}$$

which demonstrates that the rolloff frequency is a linear function of V_C.

Figure 9 shows the breadboard results using the circuit shown in Figure 8b.

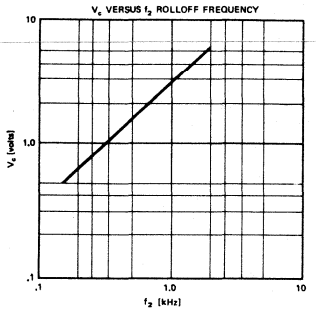


Fig. 9

It is possible to provide two decades of range with a slight degradation in linearity by increasing the gain of the level shifting stage to X100.

SQUARING AND FREQUENCY DOUBLING – Tying the two inputs of the multiplier together provides the squaring function. If V_X equals V_Y equals A cos ωt the output is:

$$V_o = \frac{A^2}{10}\cos^2 \omega t$$

$$V_o = \frac{A^2}{20} + \frac{A^2}{20}\cos 2\omega t$$

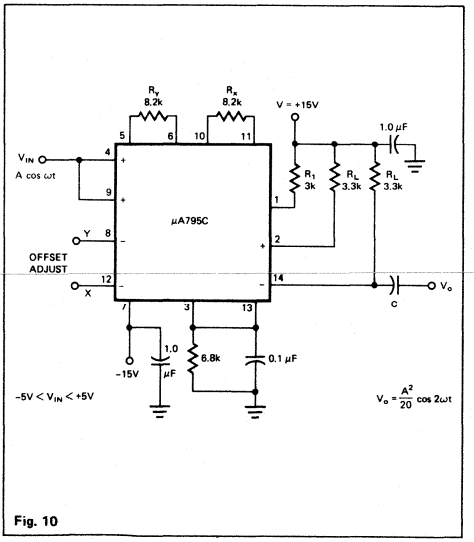


Fig. 10

The AC term coupled through the output capacitor shown in Figure 10 is a sine wave at double the frequency of the input waveform. This may be fed in turn to another doubler, etc., until any desired number of doubled and sychronized frequencies are obtained.

The input waveform is not restricted to sine waves. If the input is a set of triangle waves, then the squared output is a continuous set of unipolar parabolas, as shown in Figure 11.

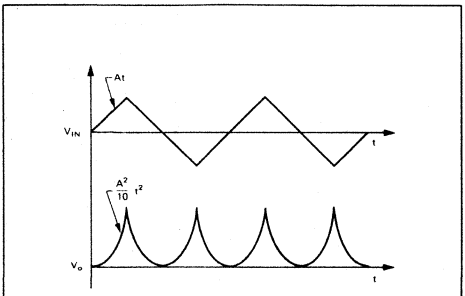


Fig. 11

Any required function may be generated by arranging an array of multipliers and providing a given function of x, namely $f_{(x)}$, as an input. For example:

$$y = A\,f_{(x)} + B\,f^2{}_{(x)} + C\,f^3{}_{(x)} + D\,f^4{}_{(x)}$$

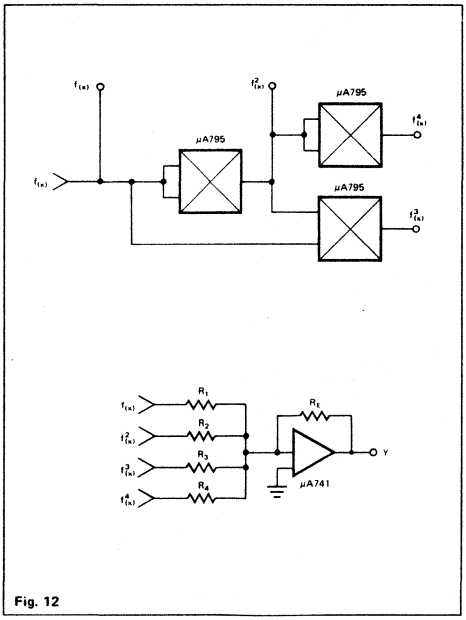


Fig. 12

may be implemented with three multipliers and one operational amplifier, as shown in the block diagram of Figure 12.

The resistors R_1, R_2, R_3, and R_4 produce the required weighing factors A, B, C, and D. It is important to keep in mind the K-factor introduced by each multiplier as previously described.

VI. CONCLUSION

The μA795 multiplier is an inexpensive and versatile new building block for linear circuit designers. It provides a quick, dependable modulator or doubler when used in the AC configuration, and it finds application in many closed-loop circuits when used as a multiplier with level shift. With its wide input voltage range and excellent linearity, the μA795 multiplier should prove to be a useful new IC device.

APPENDIX

This section gives a mathematical analysis using the μA795 functional model shown in Figure 13. This analysis assumes that base currents are negligible with respect to their associated collector currents, and that diode and transistor parameters do not vary significantly from one device to another. The first assumption is based on the use of high beta transistors in the μA795, while the second assumption is the result of the monolithic fabrication of the circuit.

In essence, the multiplier has two voltage-to-differential-current conversion circuits, a diode preconditioner, and a pair of differential amplifiers cross-connected at the output. The voltage-to-differential-current convertor consisting of Q_1 and Q_2 sends differential currents to the diodes D_1 and D_2, which produce an output voltage proportional to the difference of the logs of their input currents. The two differential amplifiers take the antilog of the difference between the logs of these currents and produce an output current. This output current is the linear product of the input voltage V_y and another input voltage V_x from the voltage-to-differential-convertor made up of transistors Q_3 and Q_4, located in the emitter circuits of the differential amplifiers.

VOLTAGE-TO-DIFFERENTIAL-CURRENT CONVERSION

Because of the symmetry of the circuit, no current flows in the resistor R_y unless an input voltage V_y is applied. Since Q_1 and Q_2 act as x1 emitter followers (the actual circuit uses a pair of high-beta Darlingtons in place of Q_1 and Q_2), the current I_y (when V_y is present) is simply:

$$I_y = \frac{V_y}{R_y} \qquad (1)$$

This current adds to Q_1's collector current and subtracts from Q_2's collector current in equal amounts, due to the equal current sources located in the emitter circuits of Q_1 and Q_2.

Q_3 and Q_4 act in the same way with the net result that:

$$I_x = \frac{V_x}{R_y} \qquad (2)$$

and the collector currents of Q_3 and Q_4 are as shown in Figure 13.

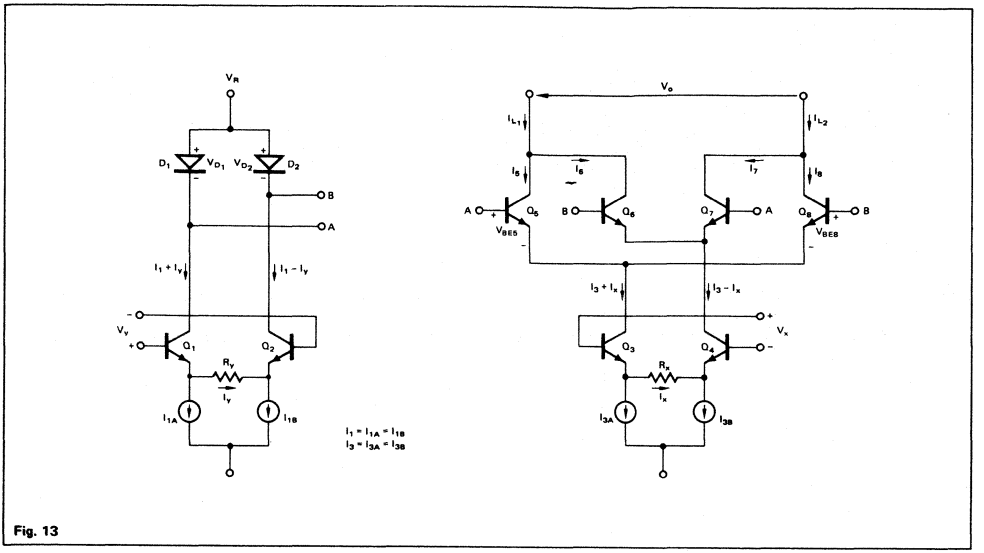


Fig. 13

PRECONDITIONING

Diodes D_1 and D_2 precondition the voltage sent to the differential amplifiers made up of Q_5, Q_6, Q_7, and Q_8.

The voltage found at points A and B is respectively:

$$V_A = V_R - V_{D_1} \tag{3}$$

$$V_B = V_R - V_{D_2} \tag{4}$$

and, therefore, the output of the preconditioner is:

$$V_{AB} = V_A - V_B \tag{5}$$

$$V_{AB} = V_{D_2} - V_{D_1} \tag{6}$$

Using the normal approximation for a forward-biased diode:

$$I_{diode} = I_o e^{\frac{V_{diode}}{V_T}} \tag{7}$$

where;

$$V_T = \frac{kT}{q} = 26 \text{ mV at } 25^\circ C$$

I_o = reverse saturation current

The expression of the diode currents in terms of the voltage across them yields:

$$I_1 + I_y = I_o e^{\frac{V_{D_1}}{V_T}} \tag{8}$$

$$I_1 - I_y = I_o e^{\frac{V_{D_2}}{V_T}} \tag{9}$$

and solving for V_{D_1} and V_{D_2} gives:

$$V_{D_1} = V_T \ln \frac{I_1 + I_y}{I_o} \tag{10}$$

$$V_{D_2} = V_T \ln \frac{I_1 - I_y}{I_o} \tag{11}$$

The output of the preconditioner therefore is:

$$V_{AB} = V_{D_2} - V_{D_1} = V_T \ln \frac{I_1 - I_y}{I_1 + I_y} \tag{12}$$

DIFFERENTIAL AMPLIFIERS

The following analysis considers the differential amplifier made up of Q_5 and Q_8, and it applies equally as well for the differential amplifier composed of Q_6 and Q_7.

Using the Ebbers-Moll model of a transistor, and assuming the base-emitter junction to be forward-biased and the collector-base junction to be heavily reverse-biased gives:

$$I_{collector} = a_1 e^{\frac{V_{BE}}{V_T}} \tag{13}$$

where a_1 is a proportionality constant which is a function of I_{eo} and the alphas of the transistor. The collector currents are then:

$$I_5 = a_1 e^{\frac{V_{BE_5}}{V_T}} \tag{14}$$

$$I_8 = a_1 e^{\frac{V_{BE_8}}{V_T}} \tag{15}$$

and the ratio of these two currents is:

X

$$\frac{I_5}{I_8} = e^{\frac{V_{BE5} - V_{BE8}}{V_T}} \quad (16)$$

Note that the input voltage, V_{AB}, to the transistor pair is:

$$V_{AB} = V_{BE5} - V_{BE8} \quad (17)$$

therefore:

$$\frac{I_5}{I_8} = e^{\frac{V_{AB}}{V_T}} \quad (18)$$

The total emitter current is:

$$I_E = I_3 + I_x = I_5 + I_8 \quad (19)$$

Defining the differential output current as:

$$I_{diff} = I_8 - I_5 \quad (20)$$

and combining equations 19 and 20 to eliminate I_8 yields:

$$I_{diff} = I_E - 2I_5 \quad (21)$$

Also, combining equations 18 and 19 to eliminate I_8 gives:

$$I_5 = I_E \frac{e^{V_{AB}/V_T}}{1 + e^{V_{AB}/V_T}} \quad (22)$$

Inserting this value for I_5 into the I_{diff} equation number (21) and simplifying yields:

$$I_{diff} = I_E \frac{1 - e^{V_{AB}/V_T}}{1 + e^{V_{AB}/V_T}} \quad (23)$$

Replacing I_{diff} and I_E with their actual values results in:

$$I_8 - I_5 = (I_3 + I_x)\frac{1 - e^{V_{AB}/V_T}}{1 + e^{V_{AB}/V_T}} \quad (24)$$

which defines the differential amplifier's output current as a function of its input voltage.

Similarly for Q_6 and Q_7 the differential output current is:

$$I_7 - I_6 = (I_3 - I_x)\frac{1 - e^{V_{AB}/V_T}}{1 + e^{V_{AB}/V_T}} \quad (25)$$

Since the voltage V_{AB} shown in equations 24 and 25 is the output of the preconditioner, as given in equation 12, the differential current equations simplify as follows:

$$I_8 - I_5 = (I_3 + I_x)\left[\frac{1 - e^{\left(\frac{V_T \ln \frac{I_1 - I_y}{I_1 + I_y}}{V_T}\right)}}{1 + e^{\left(\frac{V_T \ln \frac{I_1 - I_y}{I_1 + I_y}}{V_T}\right)}}\right] \quad (26)$$

$$I_8 - I_5 = (I_3 + I_x)\left[\frac{1 - \left(\frac{I_1 - I_y}{I_1 + I_y}\right)}{1 + \left(\frac{I_1 - I_y}{I_1 + I_y}\right)}\right] \quad (27)$$

$$I_8 - I_5 = (I_3 + I_x)\left[\frac{I_y}{I_1}\right] \quad (28)$$

Similarly equation 25 becomes:

$$I_7 - I_6 = -(I_3 - I_x)\left[\frac{I_y}{I_1}\right] \quad (29)$$

The total differential output current of two differential amplifiers is:

$$I_{L1} - I_{L2} = (I_5 + I_6) - (I_7 + I_8) \quad (30)$$

which rearranged is:

$$I_{L1} - I_{L2} = (I_5 - I_8) - (I_7 - I_6) \quad (31)$$

Using the known values of these two current pairs from equations 28 and 29 gives:

$$I_{L1} - I_{L2} = -(I_3 + I_x)\frac{I_y}{I_1} + (I_3 - I_x)\frac{I_y}{I_1} \quad (32)$$

or

$$I_{L1} - I_{L2} = -\frac{2 I_x I_y}{I_1} \quad (33)$$

Which, after inserting the values of I_x and I_y in terms of V_x and V_y from equations 1 and 2, becomes:

$$I_{L1} - I_{L2} = \frac{2 V_x V_y}{I_1 R_x R_y} \quad (34)$$

The output voltage developed across a pair of equal load resistors whose resistance value is R_L yields:

$$V_o = \frac{2 R_L V_x V_y}{I_1 R_x R_y}$$

which shows that the output of the multiplier is a linear function of the two input voltages.

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1. R. L. Pritchard, "Electrical Characteristics of Transistors", McGraw Hill, pp. 35-43, pp. 85-88, 1967.

THE μA776, AN OPERATIONAL AMPLIFIER WITH PROGRAMMABLE GAIN, BANDWIDTH, SLEW-RATE, AND POWER DISSIPATION

INTRODUCTION

The μA776 operational amplifier has a wide range of acceptable supply voltages from ±1.2 to ±18 volts and it is pin compatible with the popular μA741. A unique feature of the μA776 is the dependence of the gain, bandwidth, slew rate, and quiescent power dissipation on the master bias current setting.

This paper describes methods for setting the master bias current, discusses amplifier frequency response as a function of the master bias current, and shows some practical circuits using the unique features of the μA776.

MASTER BIAS SETTING

The master bias or I_{SET} range of the μA776 varies from as much as 100μA down to the surface leakage limit (less than 1pA at 25°C). Figure 1 shows the equivalent circuit of the

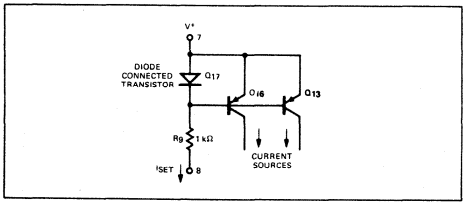


Fig. 1. Master bias circuit

internal master bias. Figure 2a shows the most straightforward method of supplying a constant set current to the μA776.

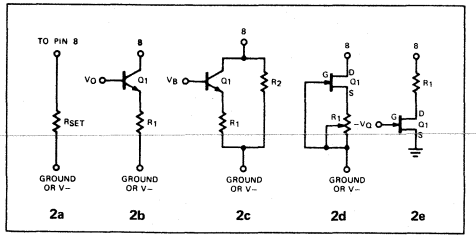


Fig. 2. Methods of current setting

Since pin 8 (pin numbers refer to the 8 lead metal can) is approximately one diode drop less than the positive supply voltage the value of R_{SET} is either:

$$R_{SET} = \frac{V_+ - 0.7}{I_{SET}} \text{ where } R_{SET} \text{ is connected to ground}$$

$$\text{or } R_{SET} = \frac{2\,V_+ - 0.7}{I_{SET}} \text{ where } V_+ = V_- \text{ and } R_{SET} \text{ is connected to } V_-.$$

Inserting Q_1 as shown in Figure 2b allows for the modulation of I_{SET} using various values of base voltage V_B. Q_1 should be a low leakage type transistor such as the Fairchild 2N5962. The scheme shown in Figure 2c provides a constant set current through R_2 plus a modulated set current controlled by V_B. The use of an FET current source as shown in Figure 2d provides a method of attaining the full range of possible set currents without requiring the many megohms of R_{SET} resistance needed by the other schemes. The FET circuit shown in Figure 2e combines the advantages of the previous circuit with the added feature of being able to cover the entire range of set currents in response to as little as a 0.5 volt change in $-V_G$ when using a low pinch-off voltage FET such as the 2N3687. The FET circuits have the disadvantage of requiring temperature compensation circuits when used in applications in which operating temperatures vary widely from the set-point temperature.

AMPLIFIER FREQUENCY RESPONSE

The inverting amplifier shown in Figure 3 has a gain equal to the ratio of R_2 to R_1. This gain value remains constant as a function of frequency until the response of the amplifier rolls off due to either the internal compensation break frequency or a slew rate limitation. The internal compensation break frequency (small signal f_2) and the slew rate limiting

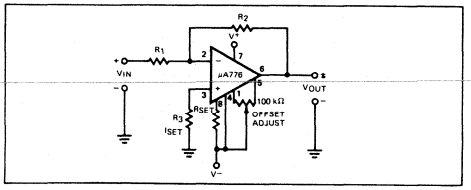


Fig. 3. Inverting amplifier

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frequency (large signal f_2) of the μA776 both are functions of the set current.

Choosing a set current and a pair of supply voltages will determine a gain-bandwidth product, GBW, for a given instance. The small-signal f_2, or 3 dB down rolloff frequency, then will be equal to:

$$f_2 = \frac{GBW}{GAIN}$$

The gain referred to in the above equation is the closed-loop gain of the amplifier. For example, assume that a given set current and supply voltage yield a GBW of 10^6. For a closed-loop gain of 5, the small-signal f_2 then would be 200 kHz. This means that for signals in the <1-volt peak-to-peak amplitude region the response of the amplifier will be 3 dB below the x5 gain level at 200 kHz and will continue to fall at a rate of 6 dB per octave of frequency for frequencies greater than 200 kHz.

If, for the same set current and supply voltages, the slew rate is 0.15 volts per microsecond, the large-signal response of the amplifier will be limited at the high frequency end by the slew rate. The amplifier must slew at a rate equal to the maximum rate of change of the input waveform, which occurs at the zero crossing for a sine wave. This maximum slewing requirement for a given frequency and amplitude is:

$$V_{out} = V_{peak} \sin 2\pi ft$$

$$\frac{dV_{out}}{dt} = V_{peak}\, 2\pi f \cos 2\pi ft$$

$$\left.\frac{dV_{out}}{dt}\right|_{t=o} = V_{peak}\, 2\pi f$$

Figure 4 shows the minimum required amplifier slew rate necessary to prevent triangularization, or slew rate limiting, of the output waveform as a function of a signal frequency and peak amplitude. For the sample slew rate of 0.15 V/μs, the circuit would pass a one-volt peak sine wave at 23 kHz, but would produce undistorted eight-volt peak sine waves only at frequencies of 3 kHz or less. Note that the slew rate limitation due to amplitude is referred to the output only. Therefore, the above large-signal calculation procedure applies regardless of the closed-loop gain of the circuit.

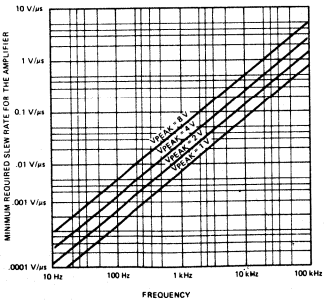


Fig. 4. Minimum required slew rate versus frequency versus peak amplitude

FIVE-DECADE, CURRENT-CONTROLLED OSCILLATOR WITHOUT EXTERNAL CAPACITORS

The current-controlled oscillator or CCO shown in Figure 5 exhibits five decades of frequency range in response to a similar range of set currents fed to pin 8 of the amplifier. This linear change in frequency as a function of set current is possible because the slew rate of the μA776 is directly proportional to the current out of the master bias-setting pin of the device.

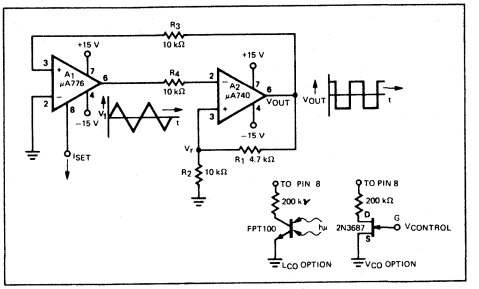


Fig. 5. Current-controlled oscillator

Amplifier A_2 acts as a comparator whose reference voltage, V_r, is equal to:

$$V_r = \frac{V_{OUT}\, R_2}{R_1 + R_2}$$

V_{OUT} oscillates between the maximum possible high and low output voltages that A_2 is capable of delivering. When the output of A_1 just exceeds the reference voltage in the positive direction, the comparator output flips to its negative extreme. A_1 begins slewing in a negative direction, and V_r changes polarity. A_1 continues to slew until it just exceeds the negatively polarized V_r. The comparator output and V_r then return to their original state, and A_1 again slews toward the positive V_r. The cycle will then repeat.

The capacitor that is alternately positively and negatively charged during each cycle is the 30 pF internal MOS frequency-compensating capacitor in the second stage of the μA776. The positive ramp exists for approximately 41% of the cycle and the negative ramp exists for approximately 59% of the cycle, due to an asymmetry in the positive and negative current sources charging the MOS capacitor. For applications requiring perfect symmetry, the output can be fed to a divide-by-two flip-flop triggered by either the positive-going or negative-going edge of V_{OUT}.

The high input impedance μA740 is used for the comparator to prevent loading of the μA776 output at low bias current settings. The μA776 output impedance increases markedly when the set current is in the ≤1 nA region. For audio frequency applications, the μA740 is replaced with another μA776 running at a full 50 μA set current, or is replaced with a μA741.

Inserting a 2N3687 FET between pin 8 and ground changes the circuit into a voltage-controlled oscillator (VCO) covering the entire five decades of frequency range as the input voltage varies between 0 volts and the pinch-off voltage of the FET (approximately −0.5 volts).

A light-controlled oscillator (LCO) results from replacing the FET with a FPT100 phototransistor. For an audio range LCO, an opaque enclosure with a small aperture should be used to bias the oscillator at the high end of the audio band. Since indoor lighting normally flickers at 120 Hz, a 4 μF capacitor from pin 8 to ground will eliminate unwanted power line modulation of the oscillator frequency due to ambient lighting.

The graph shown in Figure 6 gives typical output frequencies as a function of set current for the component values shown. Decreasing the ratio of R_2 to R_1, or decreasing the supply voltages, or both, will result in a slight upward shift in the frequency range of the oscillator since either of these changes reduces the amplitude of the output ramp of A_1.

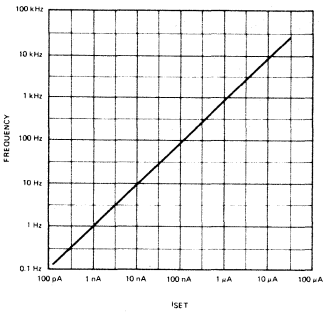


Fig. 6. Frequency versus set current

MULTIPLEXING AND SIGNAL CONDITIONING WITHOUT FETS

Multiplexing bipolar analog signals usually requires buffer amplifiers, FET switches, and extra positive and negative supply voltages sufficiently larger than the peak signal amplitude to insure that the FETs turn on and off completely.

The μA776 operational amplifier eliminates the need for the FET switches entirely, as demonstrated in Figure 7. The voltage requirement for the multiplex switches is a logic signal referenced to ground and coming from either a TTL or DTL device. Switching is accomplished by utilizing the external master bias current setting feature of μA776. By supplying or denying a 70 μA master bias, the amplifier is either fully on or shut off to the 2 nA I_{cbo} limit of the 2N5962 driving transistor shown.

The isolation between an ON amplifier and a signal fed to the input of another OFF amplifier for the circuit shown here is 80 dB at 50 kHz. Settling time of the output from one multiplex position to the next is limited only by the 5.0 V/μs slew rate of the amplifier.

PHASE SHIFTER

The normally encountered phase shift circuit consists of a group of resistors, inductors and capacitors arranged to provide a given amount of phase shift at a single frequency. Unfortunately, for any deviation from the center frequency the amplitude and phase angle at the output of the RLC circuit changes. The circuit shown in Figure 8 gives a constant phase shift and constant amplitude at the output for a range of input frequencies from 1 kHz to 10 kHz. The phase shift can

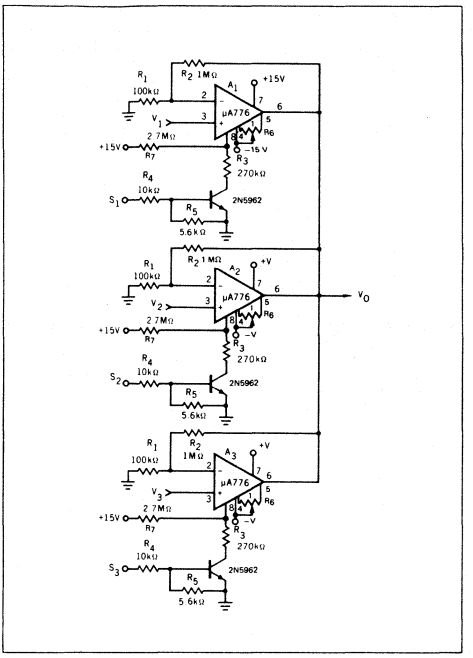


Fig. 7. Multiplexing and signal conditioning without FET's

be set from -30° to -85° and will not vary by more than 1° over the given range of input frequency.

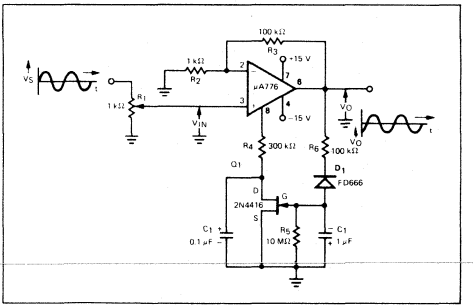


Fig. 8. Phase shifter

The circuit is basically a X100 amplifier which uses the variable internal roll-off characteristic of the μA776 to achieve a constant phase shift. Diode D_1, resistor R_5 and capacitor C_1 form a peak voltage detector. When the peak voltage at the amplifier output is approximately equal to the $V_{GS_{off}}$ voltage of Q_1, the FET will begin shutting off the current fed to the master bias set terminal of the operational amplifier. This will cause the amplifier roll-off frequency (bandwidth) to decrease. Any attempt to further increase the output voltage by

increasing the input voltage will cause the f_o roll-off frequency of the amplifier to continue to decrease, but the output voltage will remain constant. The transfer function of the circuit is:

$$\frac{V_o}{V_{in}} = \frac{100}{1 + j\frac{f}{f_o}} \qquad \text{eq. 1}$$

where:

V_o = output voltage
V_{in} = input voltage
f = frequency of the input voltage
f_o = roll-off frequency of the operational amplifier

The output voltage is now held constant, and for a given setting of R_1 the input voltage is a constant. Therefore, to maintain the equality in the case of a varying input frequency f, the internal f_o roll-off frequency will track the input frequency. Writing Equation 1 in polar form:

$$\left|\frac{V_o}{V_{in}}\right| \angle\theta = \left|\frac{100}{\sqrt{1+\left(\frac{f}{f_o}\right)^2}}\right| \angle -\arctan\frac{f}{f_o} \qquad \text{eq. 2}$$

demonstrates that the phase angle θ between input and output must remain constant regardless of the input frequency. Solving for the phase shift using the relationship between the magnitudes yields:

$$\frac{f}{f_o} = \sqrt{\left(\frac{100}{\frac{V_o}{V_{in}}}\right)^2 - 1}$$

$$\theta = -\arctan\left[\sqrt{\left(\frac{100\,V_{in}}{V_o}\right)^2 - 1}\right] \qquad \text{eq. 3}$$

If for example V_o/V_{in} were equal to 0.707(100) the phase shift from input to output would be:

$$\theta = -\arctan(2-1)$$
$$\theta = -45^\circ$$

as long as the peak input voltage remained constant. The circuit shown in Figure 8 would then apply a gain of 70.7 and a phase shift of -45° to the input waveform for any frequency in its range for this particular setting of R_1.

600 NANOWATT AMPLIFIER (QUIESCENT POWER DRAIN)

The amplifier shown in Figure 9 provides an example of the μA776 used as a low-voltage, low-power gain block. Since a power drain of 15 microwatts or less does not impair the shelf life of a mercury cell, this circuit can be powered by two mercury cells for a period of time equal to the shelf-life of the batteries. The power drawn from each supply is 240 nanoamperes times 1.2 volts, or 288 nanowatts. The 1.2-volt figure is used in the circuit to guarantee dependable end-of-life operation for battery-powered applications.

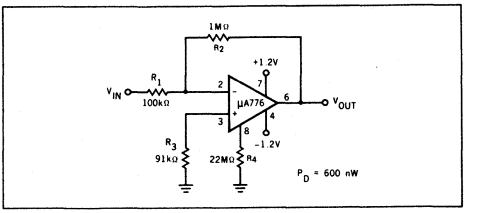


Fig. 9. 600 nanowatt amplifier

The small-signal f_2 or turnover frequency shown on the response curve of Figure 10 is 55 Hz. The maximum peak-to-peak output signal amplitude is 1.2 volts. The 30 nanoampere set current yields a maximum slew rate of 0.7 volts per millisecond. Combining this slew rate with the 1.2/2 or 0.6-volt peak output amplitude gives a large-signal f_2 of 185 Hz. Therefore, for this application, the response is limited only by the small-signal f_2 and is independent of output amplitude.

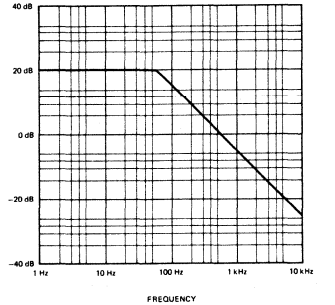


Fig. 10. Gain versus frequency for a low-power amplifier

Load resistors of less than 40 kΩ attached to the output of the amplifier will reduce the peak-to-peak output signal amplitude below the 1.2-volt level.

LOW COST SAMPLE AND HOLD

Operational amplifiers in sample and hold circuits should ideally have high slew rates for fast acquistion times and extremely low input bias currents for long hold periods. These characteristics can usually be obtained using a FET input op amp, but at the expense of increased voltage drift with temperature. A closer look at the problem reveals that the high slew rate requirement exists only during the sample period, while the low input bias requirement is of consequence only during the hold period of the cycle. The low cost programmable μA776 operational amplifier allows switching from a high slew rate op amp requiring a 50 nA input bias current to a holding amplifier mode requiring only a 750 pA input bias current (which is the order of magnitude stated for FET input op amps). The sample and hold circuit shown in

Figure 11 demonstrates this application.

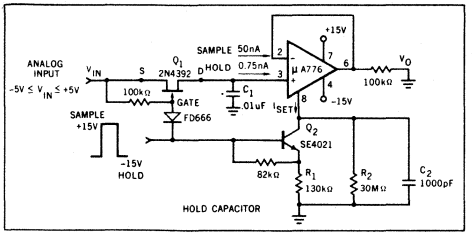


Fig. 11. Low cost sample and hold

During the sample period, FET Q_1 is on and the hold capacitor C_1 charges to a voltage equal to the analog input voltage. The same +15 V sample voltage which turned on Q_1 also turns on the emitter follower composed of transistor Q_2 and resistor R_1. This causes approximately 100 μA of I_{SET} current to flow into pin 8 of the op amp raising the slew rate to about 5 V/μs. When the logic input swings to the −15 V hold level, Q_1 and Q_2 switch off. This causes the voltage on the hold capacitor to be isolated from changes in the analog input voltage and reduces the I_{SET} current to the programmable op amp to a standby level of 0.5 μA determined by resistor R_2. Since the input bias current is almost directly proportional to the set current, the input bias current drops from 50 nA down to 750 pico-amps. Although the slew rate also decreases proportionately, this has no effect on circuit operation during the hold period of the cycle. Capacitor C_2 isolates the amplifier from Q_2's switching transient.

CONCLUSION

The μA776 monolithic operational amplifier is an exceptionally adaptable device capable of operating from ±18-volt sources, or from a pair of batteries at their worst-case 1.2-volt end-of-life potential. As discussed in the text, the master bias control allows the user to choose the bandwidth, slew rate, and power dissipation of the device.

μA7800 SERIES

THREE - TERMINAL POSITIVE VOLTAGE REGULATORS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

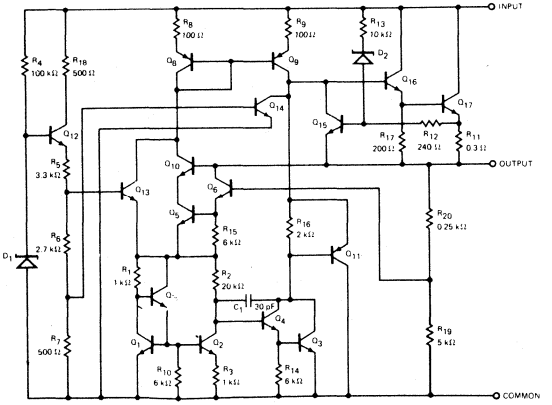
GENERAL DESCRIPTION – The μA7800 series of Three-Terminal Positive Voltage Regulators are constructed using the Fairchild Planar* epitaxial process. These regulators employ internal current limiting, thermal shutdown and safe-area compensation making them essentially blow-out proof. If adequate heat sinking is provided, they can deliver over 1A output current. They are intended as fixed-voltage regulators in a wide range of applications including local, on-card regulation for elimination of noise and distribution problems associated with single point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents and as the power pass element in precision regulators.

- **OUTPUT CURRENT IN EXCESS OF 1 AMP**
- **NO EXTERNAL COMPONENTS**
- **INTERNAL THERMAL OVERLOAD PROTECTION**
- **INTERNAL SHORT CIRCUIT CURRENT LIMITING**
- **OUTPUT TRANSISTOR SAFE-AREA COMPENSATION**
- **AVAILABLE IN THE PLASTIC TO-220 AND THE METAL TO-3 PACKAGE**

ABSOLUTE MAXIMUM RATINGS

Input Voltage (5 V through 18 V)	35 V
(24 V)	40 V
Internal Power Dissipation (Note 1)	Internally Limited
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	0°C to +125°C
Lead Temperature (Soldering, 60 second time limit) TO-3 Package	300°C
(Soldering, 10 second time limit) TO-220 Package	230°C

EQUIVALENT CIRCUIT

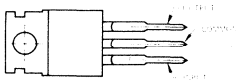


Note on following page.

VOLTAGE RANGE

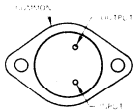
μA7805	5 V
μA7806	6 V
μA7808	8 V
μA7812	12 V
μA7815	15 V
μA7818	18 V
μA7824	24 V

CONNECTION DIAGRAMS
TO-220 PLASTIC POWER PACKAGE
(TOP VIEW)



ORDER PART NOS: UGH7805393, UGH7806393, UGH7808393, UGH7812393, UGH7815393, UGH7818393, UGH7824393

TO-3 PACKAGE
(TOP VIEW)



ORDER PART NOS: UGJ7805393, UGJ7806393, UGJ7808393, UGJ7812393, UGJ7815393, UGJ7818393, UGJ7824393

*Planar is a patented Fairchild process.

μA7805

ELECTRICAL CHARACTERISTICS (V_{IN} = 10 V, I_{OUT} = 500 mA, 0°C < T_J < 125°C, unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Voltage	T_J = 25°C	4.8	5.0	5.2	V
Line Regulation	T_J = 25°C, I_{OUT} = 100 mA				
	7 V ≤ V_{IN} ≤ 25 V		7.0	50	mV
	8 V ≤ V_{IN} ≤ 12 V		2.0	25	mV
	T_J = 25°C, I_{OUT} = 500 mA				
	7 V ≤ V_{IN} ≤ 25 V		35	100	mV
	8 V ≤ V_{IN} ≤ 12 V		8.0	50	mV
Load Regulation	T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 1.5 A		11	100	mV
	250 mA ≤ I_{OUT} ≤ 750 mA		4.0	50	mV
Output Voltage	7 V ≤ V_{IN} ≤ 20 V, 5 mA ≤ I_{OUT} ≤ 1.0 A P ≤ 15 W	4.75		5.25	V
Quiescent Current	T_J = 25°C		4.3	8.0	mA
Quiescent Current Change	7 V ≤ V_{IN} ≤ 25 V			1.3	mA
	5 mA ≤ I_{OUT} ≤ 1.5 A			0.5	mA
Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz		40		μV
Long Term Stability				20	mV
Ripple Rejection	I_{OUT} = 20 mA, f = 120 Hz		70		dB
Dropout Voltage	I_{OUT} = 1A, T_J = 25°C		2.0		V
Output Resistance			30		mΩ
Short Circuit Current Limit	T_J = 25°C		750		mA
Average Temperature Coefficient of Output Voltage	I_{OUT} = 5 mA, 0°C ≤ T_A ≤ 125°C		−1.3		mV/°C

μA7806

ELECTRICAL CHARACTERISTICS (V_{IN} = 11 V, I_{OUT} = 500 mA, 0°C < T_J < 125°C, unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Voltage	T_J = 25°C	5.75	6.0	6.25	V
Line Regulation	T_J = 25°C, I_{OUT} = 100 mA				
	8 V ≤ V_{IN} ≤ 25 V		9.0	60	mV
	9 V ≤ V_{IN} ≤ 13 V		3.0	30	mV
	T_J = 25°C, I_{OUT} = 500 mA				
	8 V ≤ V_{IN} ≤ 25 V		43	120	mV
	9 V ≤ V_{IN} ≤ 13 V		10	60	mV
Load Regulation	T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 1.5 A		13	120	mV
	250 mA ≤ I_{OUT} ≤ 750 mA		5.0	60	mV
Output Voltage	8 V ≤ V_{IN} ≤ 21 V, 5 mA ≤ I_{OUT} ≤ 1.0 A P ≤ 15 W	5.7		6.3	V
Quiescent Current	T_J = 25°C		4.3	8.0	mA
Quiescent Current Change	8 V ≤ V_{IN} ≤ 25 V			1.3	mA
	5 mA ≤ I_{OUT} ≤ 1.5 A			0.5	mA
Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz		45		μV
Long Term Stability				24	mV
Ripple Rejection	I_{OUT} = 20 mA, f = 120 Hz		65		dB
Dropout Voltage	I_{OUT} = 1 A, T_J = 25°C		2.0		V
Output Resistance	I_{OUT} = 500 mA		35		mΩ
Short Circuit Current Limit	T_J = 25°C		550		mA
Average Temperature Coefficient of Output Voltage	I_{OUT} = 5 mA, 0°C ≤ T_A ≤ 125°C		−1.0		mV/°C

NOTE 1. Thermal resistance without a heat sink for junction to case temperature is 4.0°C/W for TO-3 package, 2.0°C/W for TO-220 package; ambient to case temperature is 35°C/W for TO-3 package and 50°C/W for TO-220 package.

μA7808

ELECTRICAL CHARACTERISTICS (V_{IN} = 14 V, I_{OUT} = 500 mA, 0°C < T_J < 125°C, unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Voltage	T_J = 25°C	7.7	8.0	8.3	V
Line Regulation	T_J = 25°C, I_{OUT} = 100 mA				
	10.5 V ≤ V_{IN} ≤ 25 V		12	80	mV
	11 V ≤ V_{IN} ≤ 17 V		5.0	40	mV
	T_J = 25°C, I_{OUT} = 500 mA				
	10.5 V ≤ V_{IN} ≤ 25 V		50	160	mV
	11 V ≤ V_{IN} ≤ 17 V		22	80	mV
Load Regulation	T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 1.5 A		26	160	mV
	250 mA ≤ I_{OUT} ≤ 750 mA		9.0	80	mV
Output Voltage	10.5 V ≤V_{IN}≤ 23 V, 5 mA ≤I_{OUT} ≤ 1.0 A, p ≤ 15 W	7.6		8.4	V
Quiescent Current	T_J = 25°C		4.3	8.0	mA
Quiescent Current Change	10.5 V ≤ V_{IN} ≤ 25 V			1.0	mA
	5 mA ≤ I_{OUT} ≤ 1.5 A			0.5	mA
Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz		52		μV
Long Term Stability				32	mV
Ripple Rejection	I_{OUT} = 20 mA, f = 120 Hz		62		dB
Dropout Voltage	I_{OUT} = 1 A, T_J = 25°C		2.0		V
Output Resistance	I_{OUT} = 500 mA		40		mΩ
Short Circuit Current Limit	T_J = 25°C		450		mA
Average Temperature Coefficient of Output Voltage	I_{OUT} = 5 mA, 0°C ≤ T_A ≤ 125°C		1.0		mV/°C

μA7812

ELECTRICAL CHARACTERISTICS (V_{IN} = 19 V, I_{OUT} = 500 mA, 0°C < T_J < 125°C, unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Voltage	T_J = 25°C	11.5	12.0	12.5	V
Line Regulation	T_J = 25°C, I_{OUT} = 100 mA				
	14.5 V ≤ V_{IN} ≤ 30 V		13	120	mV
	16 V ≤ V_{IN} ≤ 22 V		6.0	60	mV
	T_J = 25°C, I_{OUT} = 500 mA				
	14.5 V ≤ V_{IN} ≤ 30 V		55	240	mV
	16 V ≤ V_{IN} ≤ 22 V		24	120	mV
Load Regulation	T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 1.5 A		46	240	mV
	250 mA ≤ I_{OUT} ≤ 750 mA		17	120	mV
Output Voltage	14.5 V ≤ V_{IN} ≤ 27 V, 5 mA ≤ I_{OUT} ≤ 1.0 A, p ≤ 15 W			12.6	V
Quiescent Current	T_J = 25°C		4.4	8.0	mA
Quiescent Current Change	14.5 V ≤ V_{IN} ≤ 30 V			1.0	mA
	5 mA ≤ I_{OUT} ≤ 1.5 A			0.5	mA
Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz		75		μV
Long Term Stability				48	mV
Ripple Rejection	I_{OUT} = 20 mA, f = 120 Hz		61		dB
Dropout Voltage	I_{OUT} = 1 A, T_J = 25°C		2.0		V
Output Resistance	I_{OUT} = 500 mA		75		mΩ
Short Circuit Current Limit	T_J = 25°C		350		mA
Average Temperature Coefficient of Output Voltage	I_{OUT} = 5 mA, 0°C ≤ T_A ≤ 125°C		−2.0		mV/°C

μA7815

ELECTRICAL CHARACTERISTICS (V_{IN} = 23 V, I_{OUT} = 500 mA, 0°C ≤ T_J ≤ 125°C, unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Voltage	T_J = 25°C	14.4	15.0	15.6	V
Line Regulation	T_J = 25°C, I_{OUT} = 100 mA				
	17.5 V ≤ V_{IN} ≤ 30 V		14	150	mV
	20 V ≤ V_{IN} ≤ 26 V		6.0	75	mV
	T_J = 25°C, I_{OUT} = 500 mA				
	17.5 V ≤ V_{IN} ≤ 30 V		57	300	mV
	20 V ≤ V_{IN} ≤ 26 V		27	150	mV
Load Regulation	T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 1.5 A		68	300	mV
	250 mA ≤ I_{OUT} ≤ 750 mA		25	150	mV
Output Voltage	17.5 V ≤ V_{IN} ≤ 30 V, 5 mA ≤ I_{OUT} ≤ 1.0 A, P ≤ 15 W	14.25		15.75	V
Quiescent Current	T_J = 25°C		4.4	8.0	mA
Quiescent Current Change	17.5 V ≤ V_{IN} ≤ 30 V			1.0	mA
	5 mA ≤ I_{OUT} ≤ 1.5 A			0.5	mA
Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz		90		μV
Long Term Stability				60	mV
Ripple Rejection	I_{OUT} = 20 mA, f = 120 Hz		60		dB
Dropout Voltage	I_{OUT} = 1 A, T_J = 25°C		2.0		V
Output Resistance	I_{OUT} = 500 mA		95		mΩ
Short Circuit Current Limit	T_J = 25°C		230		mA
Average Temperature Coefficient of Output Voltage	I_{OUT} = 5 mA, 0°C ≤ T_A ≤ 125°C		−2.0		mV/°C

μA7818

ELECTRICAL CHARACTERISTICS (V_{IN} = 27 V, I_{OUT} = 500 mA, 0°C ≤ T_J ≤ 125°C, unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Voltage	T_J = 25°C	17.3	18.0	18.7	V
Line Regulation	T_J = 25°C, I_{OUT} = 100 mA				
	21 V ≤ V_{IN} ≤ 33 V		25	180	mV
	24 V ≤ V_{IN} ≤ 30 V		10	90	mV
	T_J = 25°C, I_{OUT} = 500 mA				
	21 V ≤ V_{IN} ≤ 33 V		90	360	mV
	24 V ≤ V_{IN} ≤ 30 V		50	180	mV
Load Regulation	T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 1.0 A		110	360	mV
	250 mA ≤ I_{OUT} ≤ 750 mA		55	180	mV
Output Voltage	21 V ≤ V_{IN} ≤ 33 V, 5 mA ≤ I_{OUT} ≤ 1.0 A, P ≤ 15 W	17.1		18.9	V
Quiescent Current	T_J = 25°C		4.5	8.0	mA
Quiescent Current Change	21 V ≤ V_{IN} ≤ 33 V			1.0	mA
	5 mA ≤ I_{OUT} ≤ 1.0 A			0.5	mA
Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz		110		μV
Long Term Stability				72	mV
Ripple Rejection	I_{OUT} = 20 mA, f = 120 Hz		59		dB
Dropout Voltage	I_{OUT} = 1 A, T_J = 25°C		2.0		V
Output Resistance	I_{OUT} = 500 mA		110		mΩ
Short Circuit Current Limit	T_J = 25°C		200		mA
Average Temperature Coefficient of Output Voltage	I_{OUT} = 5 mA, 0°C ≤ T_A ≤ 125°C		−1.0		mV/°C

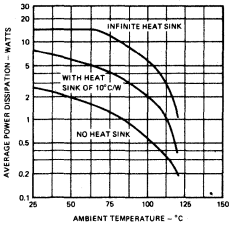
μA7824

ELECTRICAL CHARACTERISTICS (V_{IN} = 33 V, I_{OUT} = 500 mA, 0°C < T_J < 125°C, unless otherwise specified)

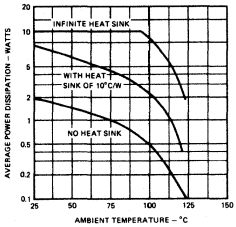
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Voltage	T_J = 25°C	23.0	24.0	35.0	V
Line Regulation	T_J = 25°C, I_{OUT} = 100 mA				
	27 V ≤ V_{IN} ≤ 38 V		31	240	mV
	30 V ≤ V_{IN} ≤ 36 V		14	120	mV
	T_J = 25°C, I_{OUT} = 500 mA				
	27 V ≤ V_{IN} ≤ 38 V		118	480	mV
	30 V ≤ V_{IN} ≤ 36 V		70	240	mV
Load Regulation	T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 1.0 A		150	480	mV
	250 mA ≤ I_{OUT} ≤ 750 mA		85	240	mV
Output Voltage	27 V ≤ V_{IN} ≤ 38 V, 5 mA ≤ I_{OUT} ≤ 1.0 A	22.8		25.2	V
	P ≤ 15 W				
Quiescent Current	T_J = 25°C		4.6	8.0	mA
Quiescent Current Change	27 V ≤ V_{IN} ≤ 38 V			1.0	mA
	5 mA ≤ I_{OUT} ≤ 1.0 A			0.5	mA
Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz		170		μV
Long Term Stability				96	mV
Ripple Rejection	I_{OUT} =20 mA, f = 120 Hz		56		dB
Dropout Voltage	I_{OUT} = 1 A, T_J = 25°C		2.0		V
Output Resistance	I_{OUT} = 500 mA		150		mΩ
Short Circuit Current Limit	T_J = 25°C		150		mA
Average Temperature Coefficient of Output Voltage	I_{OUT} = 5 mA, 0°C ≤ T_A ≤ 125°C		−1.0		mV/°C

TYPICAL PERFORMANCE CURVES

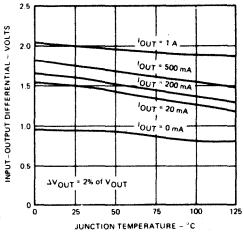
MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-3 PACKAGE)



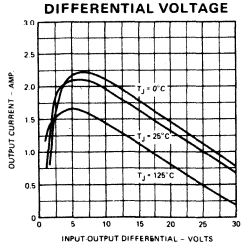
MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-220 PACKAGE)



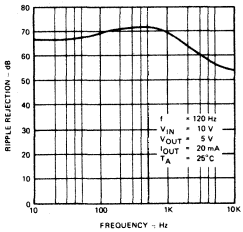
DROPOUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



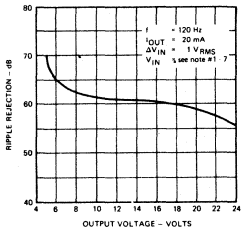
PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE



RIPPLE REJECTION AS A FUNCTION OF FREQUENCY

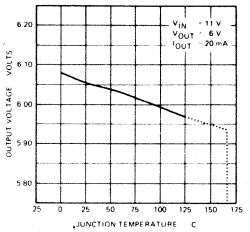


RIPPLE REJECTION AS A FUNCTION OF OUTPUT VOLTAGES

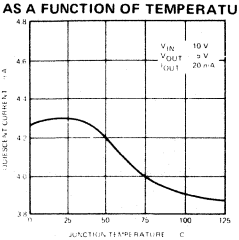


TYPICAL PERFORMANCE CURVES (cont'd)

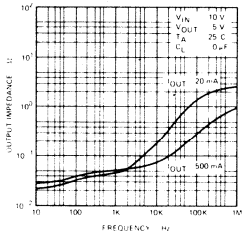
OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



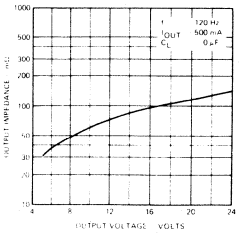
QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE



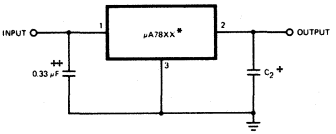
OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY



OUTPUT IMPEDANCE AS A FUNCTION OF OUTPUT VOLTAGE

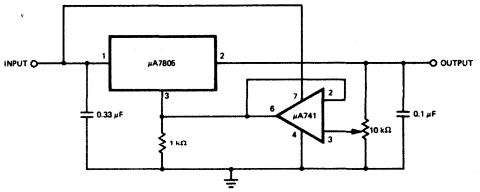


APPLICATIONS



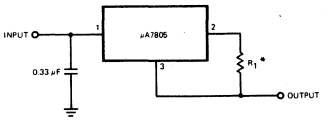
NOTES:
*To specify an output voltage, substitute voltage value for "XX".
+Although no output capacitor is needed for stability, it does improve transient response.
++Required if regulator is located an appreciable distance from power supply filter.

FIXED OUTPUT REGULATOR



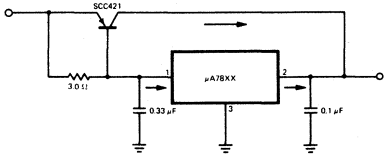
V_{OUT}, 7 V to 20 V
$V_{IN} - V_{OUT} \geq 2$ V

ADJUSTABLE OUTPUT REGULATOR – HIGH LINE REGULATION



*R_1 determines output current.

CURRENT REGULATOR



HIGH CURRENT VOLTAGE REGULATOR

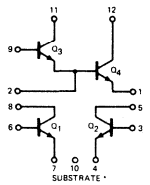
CA3018·CA3018A·CA3019·CA3026·CA3036
CA3039·CA3045·CA3046·CA3054·CA3086

TRANSISTOR AND DIODE ARRAYS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

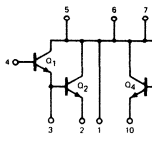
GENERAL DESCRIPTION – Fairchild transistor and diode arrays consist of general purpose integrated circuit devices constructed on a single substrate, using the Fairchild Planar* epitaxial process. These arrays are arranged to offer maximum flexibility in circuit design for applications from D.C. to 120 MHz. Excellent transistor and diode matching and temperature tracking allow circuit techniques unavailable when using discrete devices. Multiple devices in one package permit a greater packing density and cost savings than with individual packaged transistors.

- **PRECISION MONOLITHIC MATCHING**
- **DESIGN FLEXIBILITY**
- **CUSTOM APPLICATIONS**

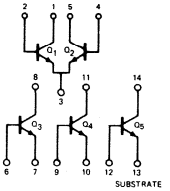


ORDER PART NO.
CA3018/CA3018A
PACKAGE: 5G

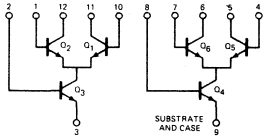
CASE



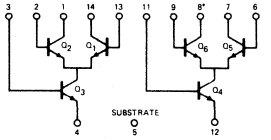
ORDER PART NO.
CA3036
PACKAGE: 5E



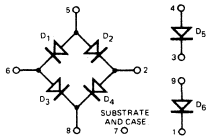
ORDER PART NOS.
CA3045/3046/3086
PACKAGE: 6A



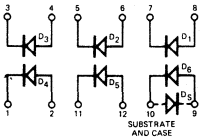
ORDER PART NO.
CA3026
PACKAGE: 5G



ORDER PART NO.
CA3054
PACKAGE: 6A



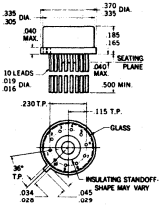
ORDER PART NO.
CA3019
PACKAGE: 5E



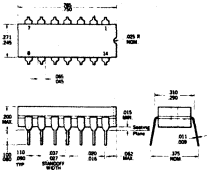
ORDER PART NO.
CA3039
PACKAGE: 5G

PHYSICAL DIMENSIONS

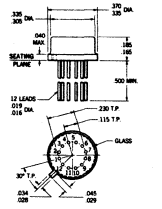
PACKAGE 5E



PACKAGE 6A



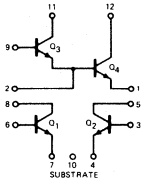
PACKAGE 5G



*Planar is a patented Fairchild process.

- **MATCHED MONOLITHIC GENERAL PURPOSE TRANSISTORS**
- **h_{FE} MATCHED ±10%**
- **V_{BE} MATCHED ±2 mV CA3018A (±5 mV CA3018)**
- **OPERATION FROM DC TO 120 MHz**
- **WIDE OPERATING CURRENT RANGE**
- **CA3018A PERFORMANCE CHARACTERISTICS CONTROLLED FROM 10 μA TO 10 mA**
- **LOW NOISE FIGURE – 3.2 dB TYPICAL AT 1 kHz**
- **FULL MILITARY TEMPERATURE RANGE CAPABILITY (–55 TO +125°C)**

EQUIVALENT CIRCUIT



APPLICATIONS

- General Use in Signal Processing Systems in DC Through VHF Range
- Custom Designed Differential Amplifiers
- Temperature Compensated Amplifiers

ABSOLUTE MAXIMUM RATINGS

	CA3018	CA3018A
Power Dissipation (Note 1)		
Any One Transistor	300 mW	300 mW
Total Package	450 mW	450 mW
Temperature Range		
Operating Temperature	–55°C to +125°C	–55°C to +125°C
Storage Temperature	–65°C to +200°C	–65°C to +200°C
The following ratings apply for each transistor in the device:		
Collector-to-Emitter Voltage, V_{CEO}	15 V	15 V
Collector-to-Base Voltage, V_{CBO}	20 V	30 V
Collector-to-Substrate Voltage, V_{CIO} (Note 2)	20 V	40 V
Emitter-to-Base Voltage, V_{EBO}	5 V	5 V
Collector Current, I_C	50 mA	50 mA

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

PARAMETER		CONDITIONS	MIN.	TYP.	MAX.	MIN.	TYP.	MAX	UNITS
				CA3018			CA3018A		
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0		0.002	100		0.002	40	nA
Collector-Cutoff Current	I_{CEO}	V_{CE} = 10 V, I_B = 0		See Curve	5		See Curve	0.5	μA
Collector-Cutoff Current Darlington Pair	I_{CEOD}	V_{CE} = 10 V, I_B = 0						5	μA
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	15	24		15	24		V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	20	60		30	60		V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	5	7		5	7		V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_{CI} = 0	20	60		40	60		V
Collector-to-Emitter Saturation Voltage	V_{CES}	I_B = 1 mA, I_C = 10 mA		0.23			0.23	0.5	V
Static Forward Current Transfer Ratio	h_{FE}	V_{CE} = 3 V, I_C = 10 mA		100		50	100		
		V_{CE} = 3 V, I_C = 1 mA	30	100		60	100		
		V_{CE} = 3 V, I_C = 10 μA		54		30	54		
Magnitude of Static-Beta Ratio (Isolated Transistors Q_1 and Q_2)		V_{CE} = 3 V, I_{C1} = I_{C2} = 1 mA	0.9	0.97		0.9	0.97		
Static Forward Current Transfer Ratio Darlington Pair (Q_3 & Q_4)	h_{FED}	V_{CE} = 3 V, I_C = 1 mA	1500	5400		2000	5400		
		V_{CE} = 3 V, I_C = 100 μA				1000	2800		
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3 V, I_E = 1 mA		0.715		0.600	0.715	0.800	V
		V_{CE} = 3 V, I_E = 10 mA		0.800			0.800	0.900	
Input Offset Voltage	$\lvert V_{BE_1} - V_{BE_2} \rvert$	V_{CE} = 3 V, I_E = 1 mA		0.48	5		0.48	2	mV
Temperature Coefficient: Base-to-Emitter Voltage Q_1, Q_2	$\frac{\lvert \Delta V_{BE} \rvert}{\Delta T}$	V_{CE} = 3 V, I_E = 1 mA		–1.9			–1.9		mV/°C
Base (Q_3)-to-Emitter (Q_4) Voltage-Darlington Pair	V_{BED} ($V_{9,1}$)	V_{CE} = 3 V, I_E = 10 mA		1.46			1.46	1.60	V
		V_{CE} = 3 V, I_E = 1 mA		1.32		1.10	1.32	1.50	
Temperature Coefficient: Base-to-Emitter Voltage Darlington Pair-Q_3,Q_4	$\frac{\lvert \Delta V_{BED} \rvert}{\Delta T}$	V_{CE} = 3 V, I_E = 1 mA		4.4			4.4		mV/°C
Temperature Coefficient of Input-Offset Voltage	$\frac{\lvert V_{BE_1} - V_{BE_2} \rvert}{\Delta T}$	V_{CC} = +6 V, V_{EE} = –6 V,		10			10		μV/°C

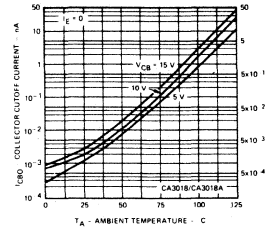
NOTES
1. Derate at 5 mW/°C for $T_A > 85°C$.
2. Substrate must be connected to the most negative voltage to maintain normal operation.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

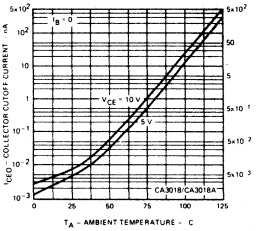
PARAMETER		CONDITIONS	MIN.	TYP.	MAX.	UNITS
Low Frequency Noise Figure	NF	f = 1 kHz, V_{CE} = 3 V, I_C = 100 μA Source resistance = 1 kΩ		3.25		dB
Low-Frequency, Small-Signal Equivalent Circuit Characteristics:						
Forward Current-Transfer Ratio	h_{fe}	f = 1 kHz, V_{CE} = 3 V, I_C = 1 mA		110		
Short-Circuit Input Impedance	h_{ie}			3.5		k Ω
Open-Circuit Output Impedance	h_{oe}			15.6		μmho
Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}			1.8×10^{-4}		
Admittance Characteristics:						
Forward Transfer Admittance	Y_{fe}	f = 1 MHz, V_{CE} = 3 V, I_C = 1 mA		31−j 1.5		mmho
Input Admittance	Y_{ie}			0.3+j 0.04		mmho
Output Admittance	Y_{oe}			0.001+j 0.03		mmho
Reverse Transfer Admittance	Y_{re}			See Curve		mmho
Gain-Bandwidth Product	f_T	V_{CE} = 3 V, I_C = 3 mA	300	500		MHz
Emitter-to-Base Capacitance	C_{eb}	V_{EB} = 3 V, I_E = 0		0.6		pF
Collector-to-Base Capacitance	C_{cl}	V_{CB} = 3 V, I_C = 0		0.58		pF
Collector-to-Substrate Capacitance	C_{cl}	V_{CI} = 3 V, I_C = 0		2.8		pF

TYPICAL PERFORMANCE CURVES

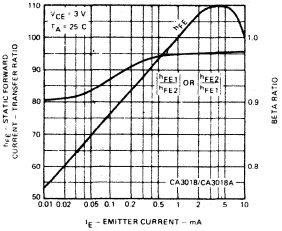
COLLECTOR-TO-BASE CUTOFF CURRENT VERSUS AMBIENT TEMPERATURE FOR EACH TRANSISTOR



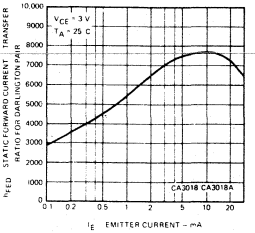
COLLECTOR-TO-EMITTER CUTOFF CURRENT VERSUS AMBIENT TEMPERATURE FOR EACH TRANSISTOR



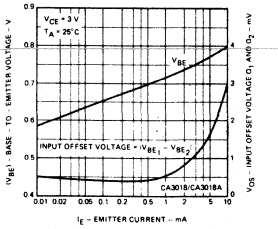
STATIC FORWARD CURRENT-TRANSFER AND BETA RATIO FOR TRANSISTORS Q_1, Q_2 VERSUS EMITTER CURRENT



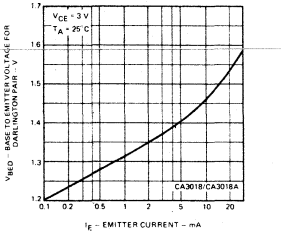
STATIC FORWARD CURRENT-TRANSFER RATIO FOR DARLINGTON CONNECTED TRANSISTORS Q_3, Q_4 VERSUS EMITTER CURRENT



STATIC BASE-TO-EMITTER VOLTAGE AND INPUT OFFSET VOLTAGE FOR Q_1, Q_2 VERSUS EMITTER CURRENT

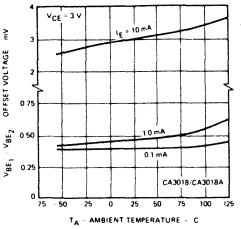


STATIC INPUT VOLTAGE FOR DARLINGTON PAIR Q_3, Q_4 VERSUS EMITTER CURRENT

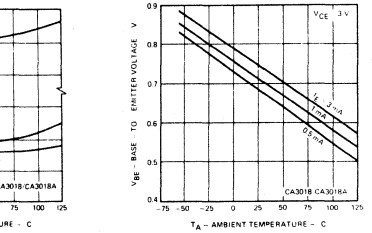


TYPICAL PERFORMANCE CURVES

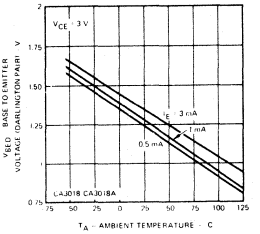
OFFSET VOLTAGE CHARACTERISTIC VERSUS AMBIENT TEMPERATURE



BASE-TO-EMITTER VOLTAGE CHARACTERISTIC FOR EACH TRANSISTOR VERSUS AMBIENT TEMPERATURE

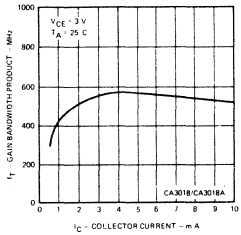


STATIC INPUT VOLTAGE FOR DARLINGTON PAIR (Q_3, Q_4) VERSUS AMBIENT TEMPERATURE

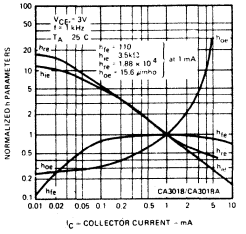


TYPICAL DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

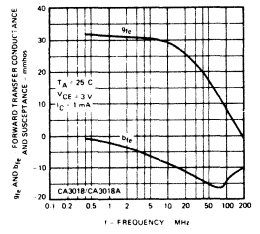
GAIN-BANDWIDTH PRODUCT (f_T) VERSUS COLLECTOR CURRENT



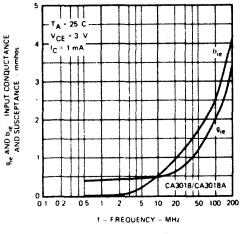
NORMALIZED h PARAMETERS VERSUS COLLECTOR CURRENT



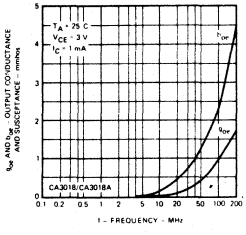
FORWARD TRANSFER ADMITTANCE (Y_{fe}) VERSUS FREQUENCY



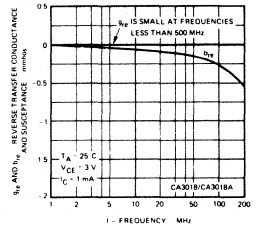
INPUT ADMITTANCE (Y_{ie}) VERSUS FREQUENCY



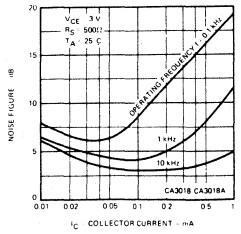
OUTPUT ADMITTANCE (Y_{oe}) VERSUS FREQUENCY



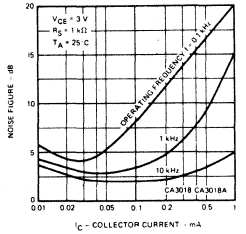
REVERSE TRANSFER ADMITTANCE (Y_{re}) VERSUS FREQUENCY



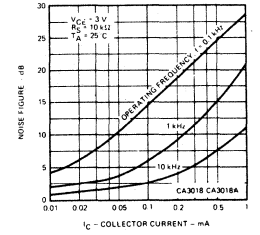
NOISE FIGURE VERSUS COLLECTOR CURRENT, R_S = 500 Ω



NOISE FIGURE VERSUS COLLECTOR CURRENT, R_S = 1 kΩ

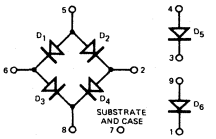


NOISE FIGURE VERSUS COLLECTOR CURRENT, R_S = 10 kΩ



- **EXCELLENT DIODE MATCHING – 1 mV TYP.**
- **LOW REVERSE LEAKAGE CURRENT – 5 mA TYP.**

EQUIVALENT CIRCUIT



APPLICATIONS
- Modulator
- Mixer
- Balanced Modulator
- Analog Switch
- Diode Gate for Chopper-Modulator Applications

ABSOLUTE MAXIMUM RATINGS

Power Dissipation	
For each Diode	20 mW
Total For Device	120 mW
Temperature Range	
Storage Temperature	−65°C to +200°C
Operating Temperature	−55°C to +125°C
Voltage (Note 1)	18 V

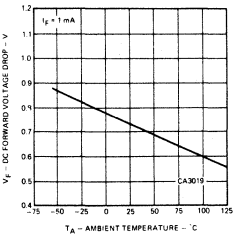
ELECTRICAL CHARACTERISTICS (For each diode, T_A = 25°C unless otherwise specified)

PARAMETER		CONDITIONS	MIN.	TYP.	MAX.	UNITS
DC Forward Voltage Drop	V_F	DC Forward Current, I_F = 1 mA		0.73	0.78	V
DC Reverse Breakdown Voltage	$V_{(BR)R}$	DC Reverse Current, I_R = −10 μA	4.0	6.0		V
DC Reverse Breakdown Voltage Between any Diode Unit and Substrate	$V_{(BR)R}$	DC Reverse Current, I_R = −10 μA	25	80		V
DC Reverse (Leakage) Current	I_R	DC Reverse Voltage, V_R = −4 V		0.0055	10	μA
DC Reverse (Leakage) Current Between any Diode Unit and Substrate	I_R	DC Reverse Voltage, V_R = −4 V		0.010	10	μA
Magnitude of Diode Offset Voltage (Difference in DC Forward Voltage Drops of any Two Diode Units)	$\lvert V_{F_1} - V_{F_2} \rvert$	DC Forward Current, I_F = 1 mA		1.0	5.0	mV
Single Diode Capacitance	C_D	Frequency, f = 1 MHz DC Reverse Voltage, V_R = −2 V		1.8		pF
Diode Quad-to-Substrate Capacitance	C_{DQ-1}	Frequency, f = 1 MHz DC Reverse Voltage, V_R between Pins 2,5,6, or 8 of Diode Quad and Pin 7 (Substrate) = −2 V				
		Pin 2 or 6 to Pin 7		4.4		pF
		Pin 5 or 8 to Pin 7		2.7		pF
Series Gate Switching Pedestal Voltage	V_S			10		mV

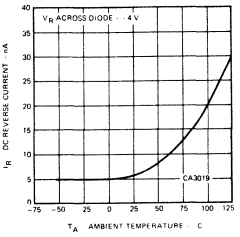
NOTE
1. Substrate (Pin 7) must be connected to the most negative potential.

TYPICAL PERFORMANCE CURVES

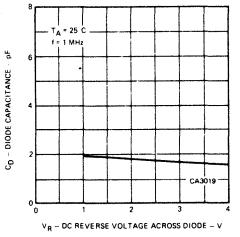
DC FORWARD VOLTAGE DROP (EACH DIODE) VERSUS TEMPERATURE



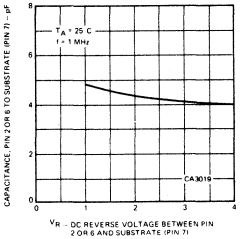
REVERSE (LEAKAGE) CURRENT (EACH DIODE) VERSUS TEMPERATURE



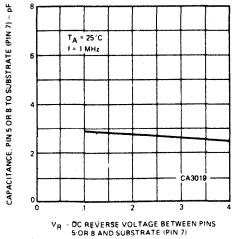
DIODE CAPACITANCE (EACH DIODE) VERSUS REVERSE VOLTAGE



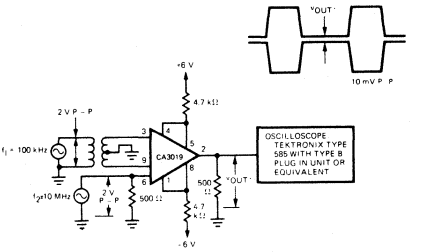
DIODE QUAD-TO-SUBSTRATE CAPACITANCE VERSUS REVERSE VOLTAGE



DIODE QUAD-TO-SUBSTRATE CAPACITANCE VERSUS REVERSE VOLTAGE

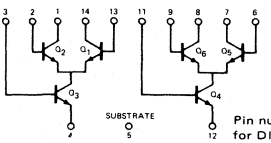


SERIES GATE SWITCHING TEST SETUP



- **LOW INPUT OFFSET VOLTAGE – ±5 mV**
- **WIDEBAND OPERATION**
- **INDEPENDENTLY ACCESSIBLE INPUTS AND OUTPUTS**
- **TWO MATCHED DIFFERENTIAL AMPLIFIERS**

EQUIVALENT CIRCUIT



Pin numbers shown for DIP only.

APPLICATIONS

- Dual Sense Amplifiers
- Dual Schmitt Triggers
- Multifunction Combinations – RF/Mixer/Oscillator; Converter/IF
- IF Amplifiers (Differential and/or Cascode)
- Product Detectors
- Doubly Balanced Modulators and Demodulators
- Balanced Quadrature Detectors
- Cascade Limiters
- Synchronous Detectors
- Pairs of Balanced Mixers
- Synthesizer Mixers
- Balanced (Push-Pull) Cascode Amplifiers

ABSOLUTE MAXIMUM RATINGS (For Each Transistor)

	CA3026	CA3054
Power Dissipation (Note 1)		
Any One Transistor	300 mW	300 mW
Total Package	600 mW	750 mW
Temperature Range		
Operating Temperature	−55°C to +125°C	0°C to +85°C
Storage Temperature	−65°C to +200°C	−25°C to +85°C
The following ratings apply for each transistor in the device		
Collector-to-Emitter Voltage, V_{CEO}		15 V
Collector-to-Base Voltage, V_{CBO}		20 V
Collector-to-Substrate Voltage, V_{CIO} (Note 2)		20 V
Emitter-to-Base Voltage, V_{EBO}		5 V
Collector Current, I_C		50 mA

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) CA3026 and CA3054

PARAMETER		CONDITIONS	MIN.	TYP.	MAX.	UNITS
For Each Differential Amplifier						
Input Offset Voltage	V_{IO}			0.45	5	mV
Input Offset Current	I_{IO}	V_{CB} = 3 V		0.3	2	μA
Input Bias Current	I_I			10	24	μA
Quiescent Operating Current Ratio	$I_{C(Q_1)}$ or $I_{C(Q_5)}$ / $I_{C(Q_2)}$ $I_{C(Q_6)}$	$I_{E(Q_3)} = I_{E(Q_4)}$ = 2 mA		0.98 to 1.02		
Temperature Coefficient Magnitude of Input-Offset Voltage	$\frac{\Delta\lvert V_{IO}\rvert}{\Delta T}$			1.1		μV/°C
For Each Transistor						
DC Forward Base-to-Emitter Voltage	V_{BE}	V_{CB} = 3 V I_C = 50 μA		0.630	0.700	V
		1 mA		0.715	0.800	
		3 mA		0.750	0.850	
		10 mA		0.800	0.900	
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CB} = 3 V, I_C = 1 mA		−1.9		mV/°C
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0		0.002	100	nA
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	15	24		V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	20	60		V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_{CI} = 0	20	60		V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	5	7		V

NOTES

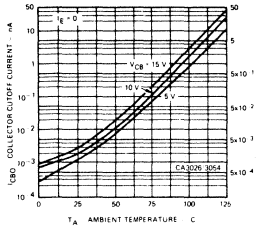
1. For $T_A > 55°C$; CA3026 derates at 5 mW/°C and CA3054 at 6.67 mW/°C
2. The collector of each transistor of the CA3026 and CA3054 is isolated from the substrate by an integral diode. Substrate must be connected to the most negative voltage to maintain normal operation.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) CA3026 and CA3054 (Continued)

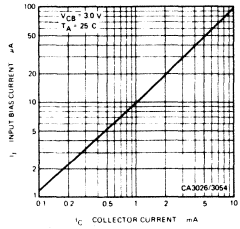
PARAMETER		CONDITIONS	MIN.	TYP.	MAX.	UNITS
Common-Mode Rejection Ratio for Each Amplifier	CMR	V_{CC} = 12 V		100		dB
AGC Range, One Stage	AGC	V_{EE} = −6 V		75		dB
Voltage Gain, Single Stage Double-Ended Output	A	V_X = −3.3 V		32		dB
AGC Range, Two Stage	AGC	f = 1 kHz		105		dB
Voltage Gain, Two Stage Double-Ended Output	A			60		dB
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics: (for Single Transistor)						
Forward Current-Transfer Ratio	h_{fe}			110		
Short-Circuit Input Impedance	h_{ie}	f = 1 kHz, V_{CE} = 3 V,		3.5		kΩ
Open-Circuit Output Impedance	h_{oe}	I_C = 1 mA		15.6		μmho
Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}			$1.8x10^{-4}$		
1/f Noise Figure (for Single Transistor)	NF	f = 1 kHz, V_{CE} = 3 V		3.25		dB
Gain-Bandwidth Product (for Single Transistor)	f_T	V_{CE} = 3 V, I_C = 3 mA		550		MHz
Admittance Characteristics; Differential Circuit Configuration: (for Each Amplifier)						
Forward Transfer Admittance	y_{21}	V_{CB} = 3 V		−20+j 0		mmho
Input Admittance	y_{11}	Each Collector		0.22+j 0.1		mmho
Output Admittance	y_{22}	$I_C \approx$ 1.25 mA		0.01+j 0		mmho
Reverse Transfer Admittance	y_{12}	f = 1 MHz		−0.003+j 0		mmho
Admittance Characteristics; Cascode Circuit Configuration: (for Each Amplifier)						
Forward Transfer Admittance	y_{21}	V_{CB} = 3 V		68-j 0		mmho
Input Admittance	y_{11}	Total Stage		0.55+j 0		mmho
Output Admittance	y_{22}	$I_C \approx$ 2.5 mA		0+j 0.02		mmho
Reverse Transfer Admittance	y_{12}	f = 1 MHz		0.004-j 0.005		μmho
Noise Figure	NF	f = 100 MHz		8		dB

TYPICAL PERFORMANCE CURVES

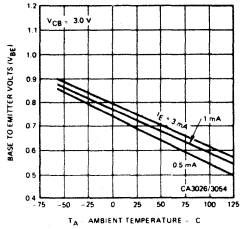
COLLECTOR-TO-BASE CUTOFF CURRENT VERSUS AMBIENT TEMPERATURE FOR EACH TRANSISTOR



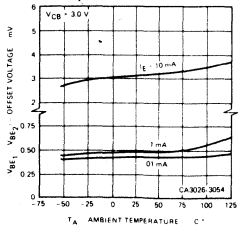
INPUT BIAS CURRENT CHARACTERISTIC VERSUS COLLECTOR CURRENT FOR EACH TRANSISTOR



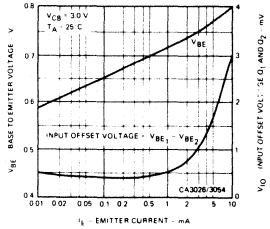
BASE-TO-EMITTER VOLTAGE CHARACTERISTIC FOR EACH TRANSISTOR VERSUS AMBIENT TEMPERATURE



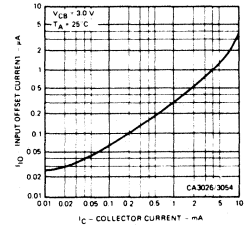
OFFSET VOLTAGE CHARACTERISTIC VERSUS AMBIENT TEMPERATURE FOR DIFFERENTIAL PAIRS



STATIC BASE-TO-EMITTER VOLTAGE CHARACTERISTIC AND INPUT OFFSET VOLTAGE FOR DIFFERENTIAL PAIRS VS EMITTER CURRENT

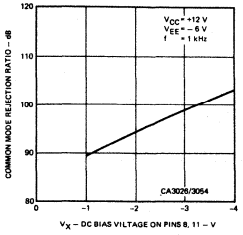


INPUT OFFSET CURRENT FOR MATCHED DIFFERENTIAL PAIRS VERSUS COLLECTOR CURRENT

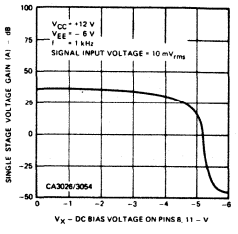


TYPICAL PERFORMANCE CURVES

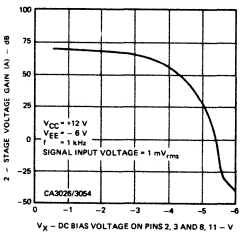
COMMON MODE REJECTION RATIO

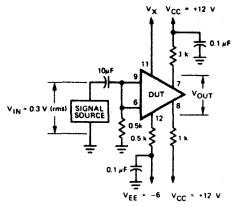


SINGLE STAGE VOLTAGE GAIN

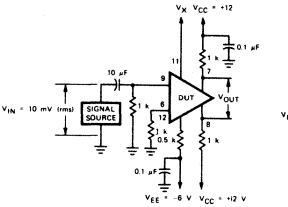


TWO-STAGE VOLTAGE GAIN

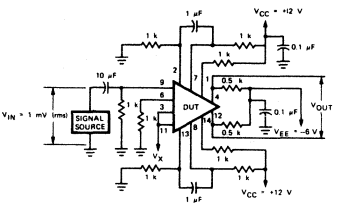




Test setup



Test setup

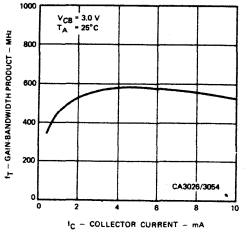


Test setup

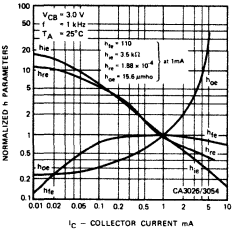
Pin numbers are shown for CA3054 (DIP) only.

TYPICAL DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

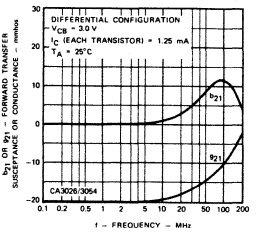
GAIN BANDWIDTH PRODUCT (f_T) VERSUS COLLECTOR CURRENT



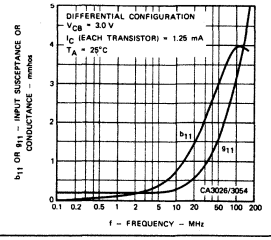
NORMALIZED h PARAMETER VERSUS COLLECTOR CURRENT FOR EACH TRANSISTOR



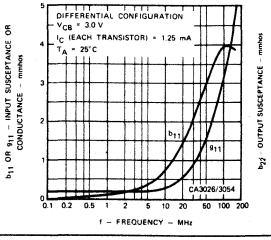
FORWARD TRANSFER ADMITTANCE (Y_{21}) VERSUS FREQUENCY



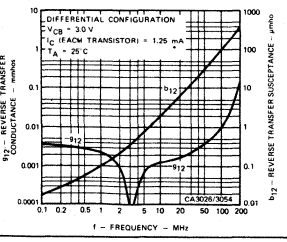
INPUT ADMITTANCE (Y_{11}) VERSUS FREQUENCY



OUTPUT ADMITTANCE (Y_{22}) VERSUS FREQUENCY

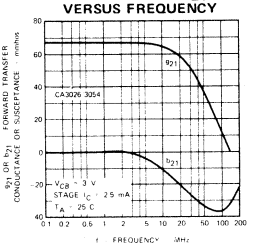


REVERSE TRANSFER ADMITTANCE (Y_{12}) VERSUS FREQUENCY

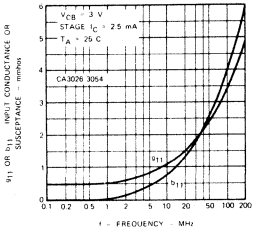


TYPICAL DYNAMIC CHARACTERISTICS FOR EACH CASCODE AMPLIFIER

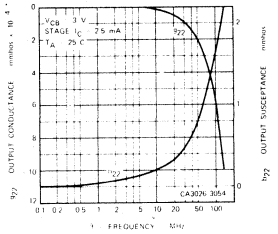
FORWARD TRANSFER ADMITTANCE (Y_{21}) VERSUS FREQUENCY



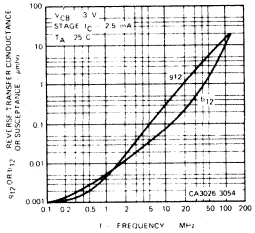
INPUT ADMITTANCE (Y_{11}) VERSUS FREQUENCY



OUTPUT ADMITTANCE (Y_{22}) VERSUS FREQUENCY



REVERSE TRANSFER ADMITTANCE (Y_{12}) VERSUS FREQUENCY

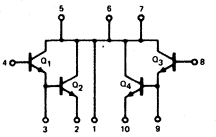


- **MATCHED TRANSISTOR PERFORMANCE**
- **LOW NOISE PERFORMANCE**
- **200 MHz GAIN BANDWIDTH PRODUCT**

APPLICATIONS
- Stereo Phonograph Preamplifiers
- Low-level Stereo and Single Channel Amplifier Stages
- Low-noise, Emitter-follower Differential Amplifiers
- Operational Amplifier Drivers

EQUIVALENT CIRCUIT

CASE



ABSOLUTE MAXIMUM RATINGS (For Each Transistor)

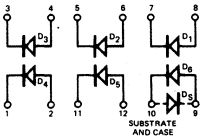
Power Dissipation	
Any One Transistor	300 mW
Total For Array	300 mW
Temperature Range	
Operating Temperature	−55°C to +125°C
Storage Temperature	−65°C to +200°C
The following ratings apply for each transistor in the array	
Collector-to-Emitter Voltage, V_{CEO}	15 V
Collector-to-Base Voltage, V_{CBO}	30 V
Emitter-to-Base Voltage, V_{EBO}	5 V
Collector Current, I_C	50 mA

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

PARAMETER		CONDITIONS	MIN.	TYP.	MAX.	UNITS
For Each Transistor (Q_1, Q_2, Q_3, Q_4)						
Collector-Cutoff Current	I_{CBO}	V_{CB} = 5 V, I_E = 0			0.5	μA
Collector-Cutoff Current	I_{CEO}	V_{CE} = 15 V, I_B = 0			5.0	μA
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	15	20		V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	30	44		V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	5.0	6.0		V
For Either Input Transistor (Q_1 or Q_3)						
Static Forward Current-Transfer Ratio	h_{FE}	I_{C1} or I_{C3} = 1 mA	30	82		
For Either Darlington Pair (Q_1, Q_2 or Q_3, Q_4)						
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO(D)}$	I_{E2} or I_{E4} = 10 μA	10	12.6		V
Static Forward Current-Transfer Ratio	$h_{FE(D)}$	$I_{C1} + I_{C2}$ or $I_{C3} + I_{C4}$ = 1 mA	1000	4540		
For Each Input Transistor (Q_1 or Q_3)						
Short-Circuit Forward Current-Transfer Ratio	h_{fe}			82		
Short-Circuit Input Impedance	h_{ie}	f = 1 kHz		2.6		kΩ
Open-Circuit Output Admittance	h_{oe}	I_{C1} or I_{C3} = 1 mA		7.0		μmho
Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}			9.8×10^{-5}		
For Either Darlington Pair (Q_1, Q_2 or Q_3, Q_4)						
Short-Circuit Forward Current-Transfer Ratio	$h_{fe(D)}$	f = 1 kHz		1300		
Short-Circuit Input Impedance	$h_{ie(D)}$	$I_{C1} + I_{C2}$ or $I_{C3} + I_{C4}$ = 1 mA		82		kΩ
Open-Circuit Output Admittance	$h_{oe(D)}$			108		μmho
Open-Circuit Reverse Voltage-Transfer Ratio	$h_{re(D)}$			2.7×10^{-3}		
Noise Voltage	E_N	f = 100 Hz		0.2	3.0	$\frac{\mu V\ (rms)}{\sqrt{f(Hz)}}$
		f = 1 kHz		0.05	0.3	
		f = 10 kHz		0.012	0.1	
For Either Input Transistor (Q_1 or Q_3)						
Forward Transfer Admittance	Y_{fe}			0.68 + j 7.9		mmho
Input Admittance (Output Short-Circuited)	Y_{ie}	f = 50 MHz		4.4 + j 5.95		mmho
Output Admittance (Input Short-Circuited)	Y_{oe}	I_{C1} or I_{C3} = 2 mA		1.94 + j 2.64		mmho
Reverse Transfer Admittance (Input Short-Circuited)	Y_{re}			Negligible		mmho
For Either Darlington Pair (Q_1, Q_2, or Q_3, Q_4)						
Input Admittance (Output Short-Circuited)	$Y_{ie(D)}$	f = 50 MHz		1.71 + j 2.8		mmho
Output Admittance (Input Short-Circuited)	$Y_{oe(D)}$	$I_{C1} + I_{C2}$ or $I_{C3} + I_{C4}$ = 2 mA		3.96 + j 2.6		mmho
Gain-Bandwidth Product	$f_T(D)$		150	200		MHz

- **EXCELLENT DIODE MATCHING – 1 mV TYP.**
- **REVERSE RECOVERY TIME – 1 ns TYP.**
- **LOW DIODE CAPACITANCE – 0.65 pF @ V_R = –2 V**

EQUIVALENT CIRCUIT



APPLICATIONS

- Balanced Modulators or Demodulators
- Ring Modulators
- High Speed Diode Gates
- Analog Switches

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (See note)	
Any One Diode Unit	100 mW
Total for Device	600 mW
Temperature Range	
Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +200°C
Voltages and Currents	
Peak Inverse Voltage, PIV for: D_1 - D_5	5 V
D_6	0.5 V
Peak Diode-to-Substrate Voltage, V_{DI} for D_1 - D_5 (term. 1,4,5,8 or 12 to term. 10)	+20, - 1 V
DC Forward Current, I_F	25 mA
Peak Recurrent Forward Current, I_f	100 mA
Peak Forward Surge Current, I_f (surge)	100 mA

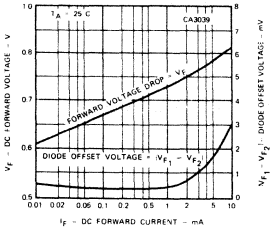
ELECTRICAL CHARACTERISTICS (For each diode unit, T_A = 25°C unless otherwise specified)

PARAMETER		CONDITIONS	MIN.	TYP.	MAX.	UNITS
DC Forward Voltage Drop	V_F	I_F = 50 μA		0.65	0.69	V
		1 mA		0.73	0.78	V
		3 mA		0.76	0.80	V
		10 mA		0.81	0.90	V
DC Reverse Breakdown Voltage	$V_{(BR)R}$	I_R = –10 μA	5.0	7.0		V
DC Reverse Breakdown Voltage Between any Diode Unit and Substrate	$V_{(BR)R}$	I_R = –10 μA	20			V
DC Reverse (Leakage) Current	I_R	V_R = –4 V		0.016	100	nA
DC Reverse (Leakage) Current Between any Diode Unit and Substrate	I_R	V_R = –10 V		0.022	100	nA
Magnitude of Diode Offset Voltage (Difference in DC Forward Voltage Drops of any Two Diode Units)	$\lvert V_{F_1} - V_{F_2} \rvert$	I_F = 1 mA		0.5	5.0	mV
Temperature Coefficient of $\lvert V_{F_1} - V_{F_2} \rvert$	$\frac{\Delta \lvert V_{F_1} - V_{F_2} \rvert}{\Delta T}$	I_F = 1 mA		1.0		μV/°C
Temperature Coefficient of Forward Drop	$\frac{\Delta V_F}{\Delta T}$	I_F = 1 mA		–1.9		mV/°C
DC Forward Voltage Drop for Anode-to-Substrate Diode (D_S)	V_F	I_F = 1 mA		0.65		V
Reverse Recovery Time	t_{rr}	I_F = 10 mA, I_R = 10 mA		1.0		ns
Diode Resistnace	R_D	f = 1 kHz, I_F = 1 mA	25	30	45	Ω
Diode Capacitance	C_D	V_R = –2 V, I_F = 0		0.65		pF
Diode-to-Substrate Capacitance	C_{DI}	V_{DI} = +4 V, I_F = 0		3.2		pF

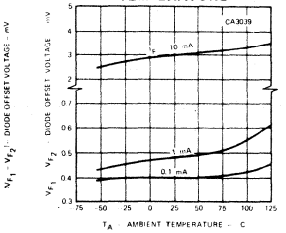
NOTE: Derate at 5.7 mW/°C for $T_A > 55°C$.

TYPICAL PERFORMANCE CURVES

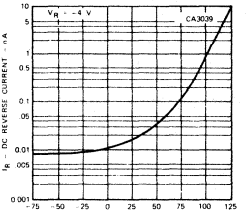
DC FORWARD VOLTAGE DROP (ANY DIODE) AND DIODE OFFSET VOLTAGE VERSUS DC FORWARD CURRENT



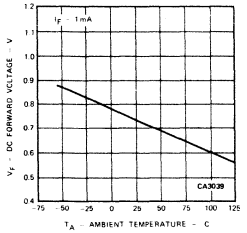
DIODE OFFSET VOLTAGE (ANY DIODE) VERSUS TEMPERATURE



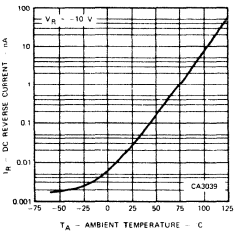
DC REVERSE (LEAKAGE) CURRENT (DIODES 1, 2, 3, 4, 5) VERSUS TEMPERATURE



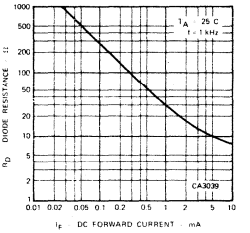
DC FORWARD VOLTAGE DROP (ANY DIODE) VERSUS TEMPERATURE



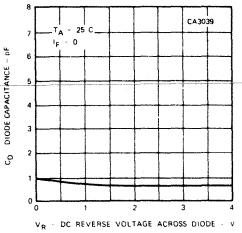
DC REVERSE (LEAKAGE) CURRENT BETWEEN DIODES (1, 2, 3, 4, 5) AND SUBSTRATE VERSUS TEMPERATURE



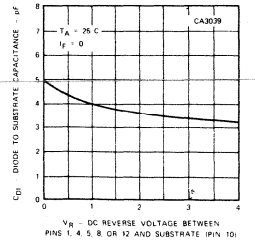
DIODE RESISTANCE (ANY DIODE) VERSUS DC FORWARD CURRENT



DIODE CAPACITANCE (DIODES 1, 2, 3, 4, 5) VERSUS REVERSE VOLTAGE



DIODE-TO-SUBSTRATE CAPACITANCE VERSUS REVERSE VOLTAGE

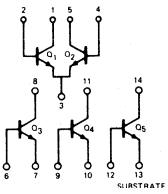


- **LOW INPUT OFFSET VOLTAGE**
- **WIDEBAND OPERATION**
- **LOW NOISE**

APPLICATIONS

- General Use in all Types of Signal Processing Systems Operating Anywhere in the Frequency Range From DC to VHF
- Custom Designed Differential Amplifiers
- Temperature Compensated Amplifiers

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS (For Each Transistor)

	CA3045		CA3046/3086	
Power Dissipation (Note 1)	**Each Transistor**	**Total Package**	**Each Transistor**	**Total Package**
At T_A = 25°C	300 mW	750 mW	300 mW	750 mW
At T_A = 25°C to 55°C			300 mW	750 mW
At T_A = 25°C to 75°C	300 mW	750 mW		
Voltages and Currents				
Collector-to-Emitter Voltage, V_{CEO}	15 V		15 V	
Collector-to-Base Voltage, V_{CBO}	20 V		20 V	
Collector-to-Substrate Voltage, V_{CIO} (Note 2)	20 V		20 V	
Emitter-to-Base Voltage, V_{EBO}	5 V		5 V	
Collector Current, I_C	50 mA		50 mA	
Temperature Range				
Operating Temperature	−55°C to +125°C		(CA3046) 0°C to +85°C (CA3086) −40°C to +85°C −55°C to +125°C	
Storage Temperature	−65°C to +200°C			

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

PARAMETER		CONDITIONS	CA3045, CA3046 MIN.	CA3045, CA3046 TYP.	CA3045, CA3046 MAX.	CA3086 MIN	CA3086 TYP	CA3086 MAX	UNITS
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	20	60		20	60		V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	15	24		15	24		V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_{CI} = 0	20	60		20	60		V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	5.0	7.0		5.0	7.0		V
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0		0.002	40		0.002	100	nA
Collector-Cutoff Current	I_{CEO}	V_{CE} = 10 V, I_B = 0		See curve	0.5		See curve	5.0	μA
Static Forward Current-Transfer Ratio (Static Beta)	h_{FE}	V_{CE} = 3 V, I_C = 10 mA		100			100		
		V_{CE} = 3 V, I_C = 1 mA	40	100		40	100		
		V_{CE} = 3 V, I_C = 10 μA		54			54		
Input Offset Current for Matched Pair Q_1 and Q_2 $\lvert I_{IO_1} - I_{IO_2} \rvert$		V_{CE} = 3 V, I_C = 1 mA		0.3	2.0				μA
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3 V, I_E = 1 mA		0.715			0.715		V
		V_{CE} = 3 V, I_E = 10 mA		0.800			0.800		
Magnitude of Input Offset Voltage for Differential Pair $\lvert V_{BE_1} - V_{BE_2} \rvert$		V_{CE} = 3 V, I_C = 1 mA		0.45	5.0				mV
Magnitude of Input Offset Voltage for Isolated Transistors $\lvert V_{BE_3} - V_{BE_4} \rvert$, $\lvert V_{BE_4} - V_{BE_5} \rvert$, $\lvert V_{BE_5} - V_{BE_3} \rvert$		V_{CE} = 3 V, I_C = 1 mA		0.45	5.0				mV
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CE} = 3 V, I_C = 1 mA		−1.9			1.9		mV/°C
Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$	I_B = 1 mA, I_C = 10 mA		0.23			0.23		V
Temperature Coefficient of Input-Offset Voltage	$\frac{\Delta V_{IO}}{\Delta T}$	V_{CE} = 3 V, I_C = 1 mA		1.1					μV/°C

NOTES

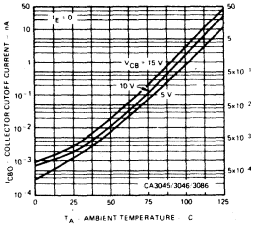
1. CA3046 and CA3086 derate at 6.67 mW/°C for T_A > 55°C, CA3045 at 8 mW/°C for T_A > 75°C.
2. Substrate (Pin 10) must be connected to the most negative voltage to maintain normal operation.

ELECTRICAL CHARACTERISTICS (T_A = 25° C unless otherwise specified) (Continued)

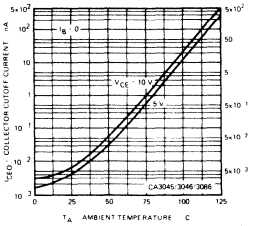
PARAMETER		CONDITIONS	MIN.	TYP.	MAX.	UNITS
Low-Frequency Noise Figure	NF	f = 1 kHz, V_{CE} = 3 V, I_C = 100 μA, R_S = 1 kΩ		3.25		dB
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:						
Forward Current-Transfer Ratio	h_{fe}	f = 1 kHz, V_{CE} = 3 V, I_C = 1 mA		110 (CA3045, CA3046)		
Forward Current-Transfer Ratio	h_{fe}			110 (CA3086)		
Short-Circuit Input Impedance	h_{ie}			3.5		kΩ
Open-Circuit Output Impedance	h_{oe}			15.6		μmho
Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}			1.8×10^{-4}		
Admittance Characteristics:						
Forward Transfer Admittance	Y_{fe}	f = 1 MHz, V_{CE} = 3 V, I_C = 1 mA		31 - j 1.5		
Input Admittance	Y_{ie}			0.3+j 0.04		
Output Admittance	Y_{oe}			0.001+j 0.03		
Reverse Transfer Admittance	Y_{re}			See curve		
Gain-Bandwidth Product	f_T	V_{CE} = 3 V, I_C = 3 mA	300	550		
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = 3V, I_E = 0		0.6		pF
Collector-to-Base Capacitance	C_{CB}	V_{CB} = 3 V, I_C = 0		0.58		pF
Collector-to-Substrate Capacitance	C_{CI}	V_{CS} = 3 V, I_C = 0		2.8		pF

TYPICAL PERFORMANCE CURVES

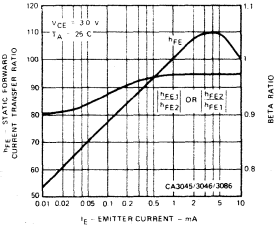
COLLECTOR-TO-BASE CUTOFF CURRENT VERSUS AMBIENT TEMPERATURE FOR EACH TRANSISTOR



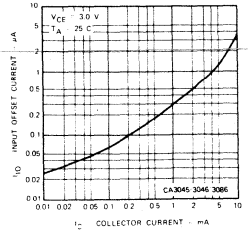
COLLECTOR-TO-EMITTER CUTOFF CURRENT VERSUS AMBIENT TEMPERATURE FOR EACH TRANSISTOR



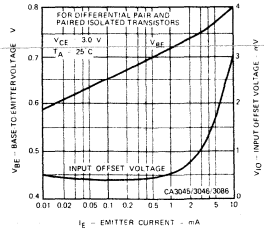
STATIC FORWARD CURRENT-TRANSFER AND BETA RATIO FOR TRANSISTORS Q_1, Q_2 VERSUS EMITTER CURRENT



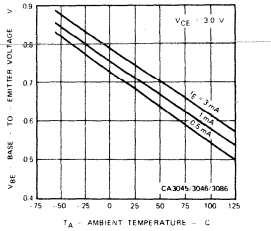
INPUT OFFSET CURRENT FOR MATCHED TRANSISTOR PAIR Q_1, Q_2 VERSUS COLLECTOR CURRENT



STATIC BASE-TO-EMITTER VOLTAGE AND INPUT OFFSET VOLTAGE VERSUS EMITTER CURRENT

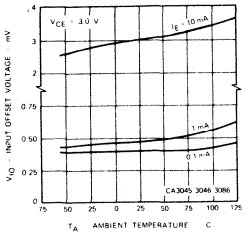


BASE-TO-EMITTER VOLTAGE CHARACTERISTIC VERSUS AMBIENT TEMPERATURE FOR EACH TRANSISTOR

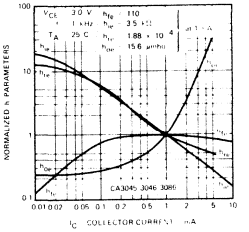


TYPICAL PERFORMANCE CURVES

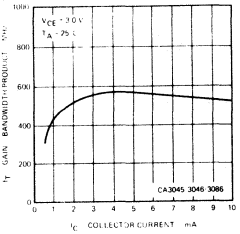
INPUT OFFSET VOLTAGE FOR DIFFERENTIAL PAIR AND PAIRED ISOLATED TRANSISTORS VERSUS AMBIENT TEMPERATURE



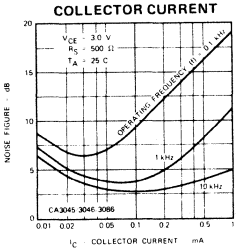
NORMALIZED h PARAMETERS VERSUS COLLECTOR CURRENT



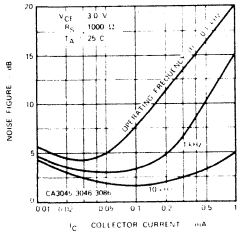
GAIN-BANDWIDTH PRODUCT VERSUS COLLECTOR CURRENT



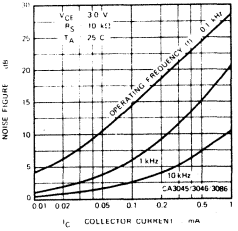
NOISE FIGURE VERSUS COLLECTOR CURRENT



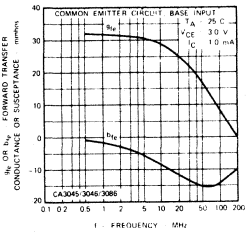
NOISE FIGURE VERSUS COLLECTOR CURRENT



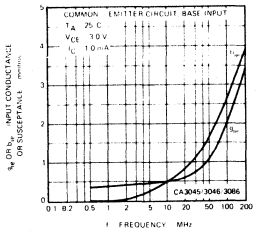
NOISE FIGURE VERSUS COLLECTOR CURRENT



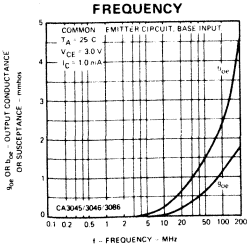
FORWARD TRANSFER ADMITTANCE VERSUS FREQUENCY



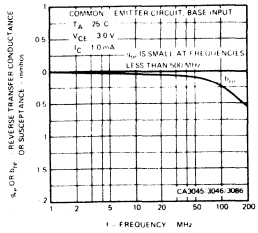
INPUT ADMITTANCE VERSUS FREQUENCY



OUTPUT ADMITTANCE VERSUS FREQUENCY



REVERSE TRANSFER ADMITTANCE VERSUS FREQUENCY



SN75450

DUAL PERIPHERAL DRIVER

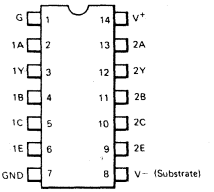
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The SN75450 is a versatile general purpose dual interface driver circuit that employs TTL or DTL logic. The SN75450 features two standard series 74 TTL gates and two uncommitted, high current, high voltage transistors offering the system designer the flexibility to tailor the circuit to his application. The SN75450 is useful in high speed logic buffers, power drivers, lamp drivers, relay drivers, line drivers, MOS drivers, clock drivers and memory drivers.

- **HIGH SPEED**
- **300 mA CURRENT CAPABILITY**
- **HIGH VOLTAGE CAPABILITY**
- **UNCOMMITTED OUTPUT DEVICES**
- **TTL OR DTL INPUT COMPATIBILITY**

CONNECTION DIAGRAMS
(TOP VIEW)

14 LEAD DIP

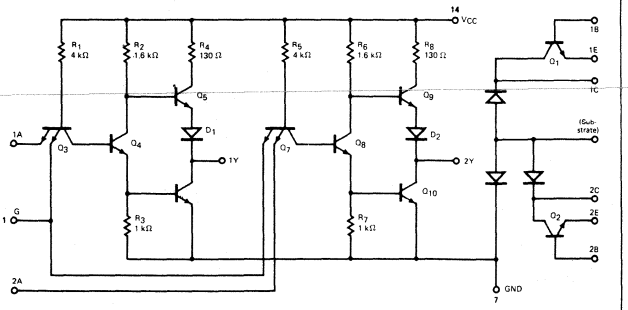


ORDER PART NO.
SN75450J

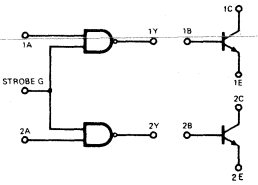
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 1)	+7 V
Internal Power Dissipation (Note 2)	800 mW
Input Voltage (Note 3)	5.5 V
V_{CC} to Substrate or Collector to Substrate Voltage	35 V
Collector to Base Voltage	35 V
Emitter To Base Voltage	5 V
Collector to Base Voltage (Note 4)	30 V
Continuous Collector Current	300 mA
Operating Temperature Range	0°C to + 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering, 60 seconds)	300°C

EQUIVALENT CIRCUIT



BLOCK DIAGRAM



Notes on following page.

ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $T_A = 25°C$ for typical values, unless otherwise specified.) (Note 5)

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
TTL Gate					
Input HIGH Voltage	$V^+ = 4.75$ V	2.0			V
Input LOW Voltage	$V^+ = 4.75$ V			0.8	V
Output HIGH Voltage	$V^+ = 4.75$ V, $V_{IN} = 0.8$ V, $I_{OUT} = -400\ \mu A$	2.4	3.3		V
Output LOW Voltage	$V^+ = 4.75$ V, $V_{IN} = 2$ V, $I_{SINK} = 16$ mA		0.22	0.40	V
Low Level Input Current	$V^+ = 5.25$ V, $V_{IN} = 0.4$ V				
Input A				−1.6	mA
Input B				−3.2	mA
High Level Input Current					
Input A	$V^+ = 5.25$ V, $V_{IN} = 2.4$ V			40	μA
Input B				80	μA
Input A	$V^+ = 5.25$ V, $V_{IN} = 5.5$ V			1.0	mA
Input B				2.0	mA
Short Circuit Output Current (Note 7)	$V^+ = 5.25$ V	−18		−55	mA
Output LOW Supply Current	$V^+ = 5$ V, All Inputs HIGH		6.0	11	mA
Output HIGH Supply Current	$V^+ = 5$ V, All Inputs LOW		2.0	4.0	mA
Output Transistor					
Collector to Base Breakdown Voltage	$I_C = 100\ \mu A$, $I_E = 0$	35	48		V
Emitter to Base Breakdown Voltage	$I_E = 100\ \mu A$, $I_C = 0$	5.0	6.0		V
Collector to Emitter Breakdown Voltage	$I_C = 100\ \mu A$, $R_{BE} = 500\ \Omega$	30			V
*Collector Substrate Breakdown Voltage	$I_{CS} = 100\ \mu A$	35	50		V
Static Forward Current Transfer Ratio	$V_{CE} = 2$ V, $I_C = 100$ mA, $T_A = 25°C$	25			
(Note 6)	$V_{CE} = 2$ V, $I_C = 300$ mA, $T_A = 25°C$	30			
	$V_{CE} = 2$ V, $I_C = 100$ mA, $T_A = 0°C$	20			
	$V_{CE} = 2$ V, $I_C = 300$ mA, $T_A = 0°C$	25			
Saturated Base to Emitter Forward Voltage	$I_C = 100$ mA, $I_B = 10$ mA		0.85	1.00	V
(Note 6)	$I_C = 300$ mA, $I_B = 30$ mA		1.05	1.2	V
Collector to Emitter Saturated Voltage	$I_C = 100$ mA, $I_B = 10$ mA		0.25	0.40	V
(Note 6)	$I_C = 300$ mA, $I_B = 30$ mA		0.50	0.70	V

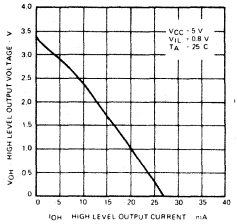
AC CHARACTERISTICS – $V^+ = +5$ V, $T_A = 25°C$, $C_L = 15$ pF, $R_L = 400\ \Omega$

TTL Gate					
Turn Off Delay Input to Output, t_{PLH}	Figure 1		12	22	ns
Turn On Delay Input to Output, t_{PHL}			8.0	15	ns
Output Transistor	$I_C = 200$ mA, $I_B{}^+ = 20$ mA, $I_B{}^- = 40$ mA				
Delay Time, t_d	Figure 2		8.0	15	ns
Rise Time, t_r			12	20	ns
Storage Time, t_s			7.0	15	ns
Fall Time, t_f			6.0	15	ns
Combined Gate and Transistor	$I_C = 200$ mA, $I_B = I_{OS}$, $C_L = 15$ pF				
Turn Off Delay Time, t_{PLH}	Figure 3		17		ns
Turn On Delay Time, t_{PHL}			16		ns
Turn Off Transistion Time, t_{TLH}			7.0		ns
Turn On Transistion Time, t_{THL}			9.0		ns

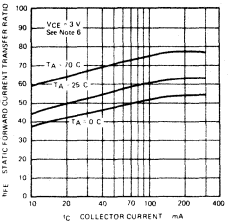
NOTES:
1. All voltage values are with respect to device ground terminal.
2. Rating applies for ambient temperatures to 70°C.
3. Input voltage should be zero or positive with respect to device ground terminal.
4. Applies for $R_{BE} < 500\ \Omega$
5. The substrate pin must always be tied to the most negative voltage for proper operation.
6. These parameters must be measured using pulse techniques. $t_w = 300\ \mu s$, duty cycle = 2%.
7. Not more than one output should be shorted at a time.

TYPICAL CHARACTERISTICS

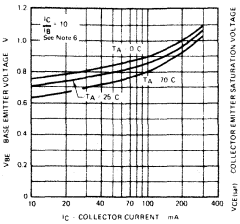
TTL GATE HIGH-LEVEL OUTPUT VOLTAGE VERSUS HIGH-LEVEL OUTPUT CURRENT



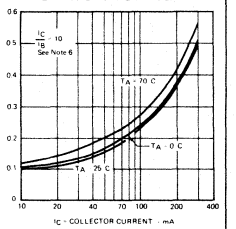
TRANSISTOR STATIC FORWARD CURRENT TRANSFER RATIO VERSUS COLLECTOR CURRENT



TRANSISTOR BASE TO EMITTER VOLTAGE VERSUS COLLECTOR CURRENT

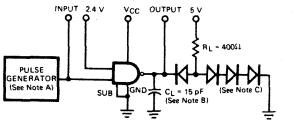


TRANSISTOR COLLECTOR TO EMITTER SATURATION VOLTAGE VERSUS COLLECTOR CURRENT

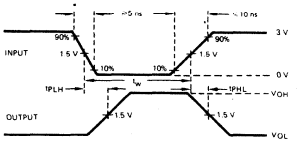


SWITCHING CHARACTERISTICS

PROPAGATION DELAY TIMES, EACH GATE



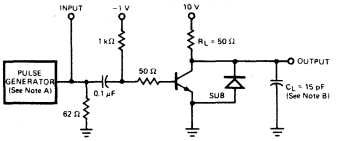
TEST CIRCUIT



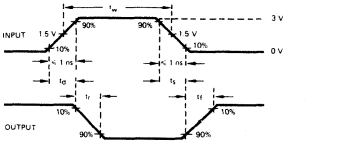
VOLTAGE WAVEFORMS

NOTES:
A. The pulse generator has the following characteristics: t_w = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L include probe and jig capacitance.
C. All diodes are 1N3064.

SWITCHING TIMES, EACH TRANSISTOR



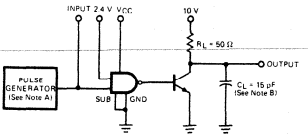
TEST CIRCUIT



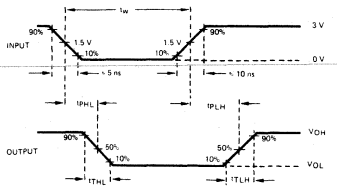
VOLTAGE WAVEFORMS

NOTES:
A. The pulse generator has the following characteristics: t_w = 0.3 μs, duty cycle ≤ 1%, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

SWITCHING TIMES, GATE AND TRANSISTOR



TEST CIRCUIT



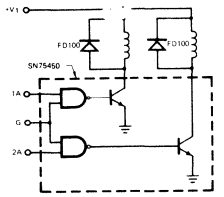
VOLTAGE WAVEFORMS

NOTES:
A. The pulse generator has the following characteristics: t_w = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

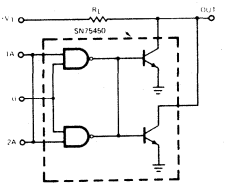
Y

TYPICAL APPLICATIONS

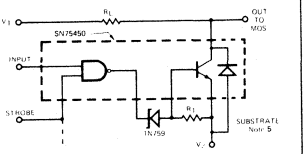
DUAL RELAY DRIVER



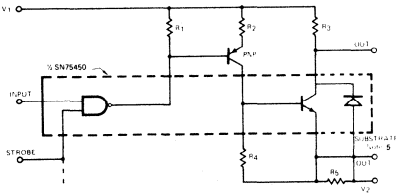
300 mA SINK DRIVER



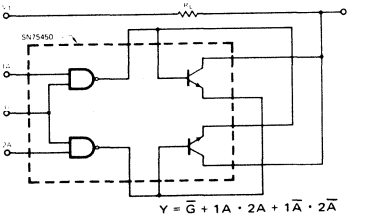
MOS DRIVER



FLOATING SWITCH

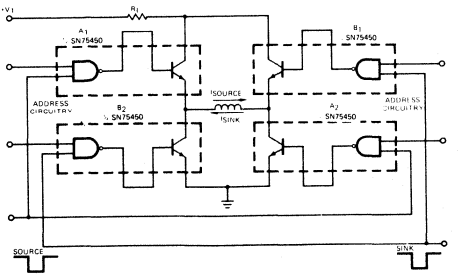


GATED COMPARATOR

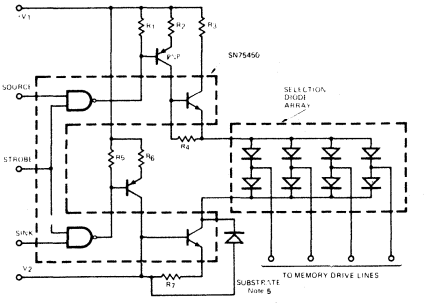


$$Y = \overline{G} + 1A \cdot 2A + 1\overline{A} \cdot 2\overline{A}$$

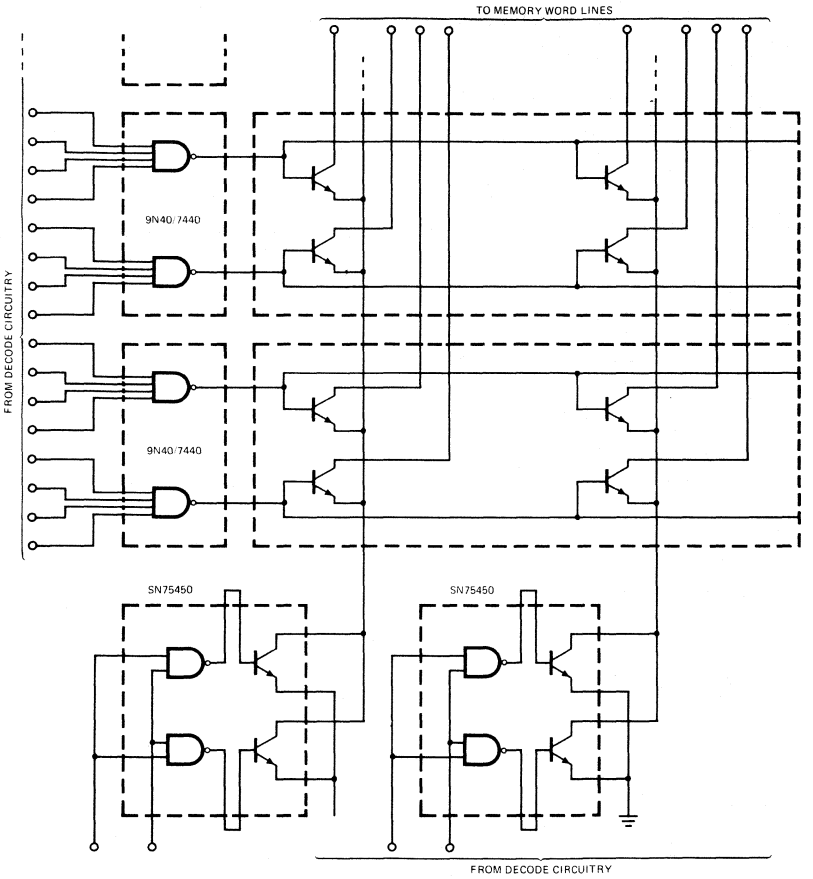
FILM MEMORY DIGIT DRIVER



CORE MEMORY DRIVER



APPLICATIONS (cont'd)



WORD LINE MEMORY DRIVER USING SN75450

SN75450 CIRCUIT APPLICATIONS

- Dual Lamp Driver
- Dual Relay Driver
- Gated Comparator
- Floating Switch
- Dual MOS-to-TTL Driver
- Dual TTL-to-MOS Driver
- 500 mA Sink Driver
- Dual Linear Amplifier
- Dual Photo Switch (TTL Compatible Output)
- NAND Gate Schmitt (Timed Relay or Lamp Control)
- High Input Impedance Low Speed Schmitt with TTL Output
- Dual High-Speed Gate
- Square Wave Generator
- SCR Gate Driver
- Super TTL Gate with 250 mA Sinking Ability
- Dual-Channel Single-Ended Line Driver
- Memory System Current Sink
- Memory System Current Source
- Film Memory Digit Driver
- Core Memory Driver
- Phase Detector
- DC to AC Converter
- Dwell Meter Driver
- Tachometer
- MOS Memory Write Driver

TBA550 †

TV SIGNAL PROCESSING CIRCUIT

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The TBA550 is a TV signal Processing Circuit constructed on a single silicon chip using the Fairchild Planar* Epitaxial process. This device serves as a central processing and distribution circuit for the video, AGC, noise, and synchronization signals for both monochrome and color TV systems including receivers, monitors and cameras. Other applications are in raster-scan alpha-numeric displays, video tape recorders and studio and broadcast equipment.

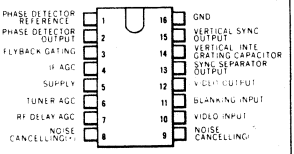
- **VIDEO PREAMPLIFIER WITH EMITTER FOLLOWER OUTPUT**
- **GATED AGC DETECTOR SUPPLYING CONTROL VOLTAGES FOR VIDEO I.F. AGC AND TUNER DELAYED AGC**
- **AUTOMATIC FREQUENCY CONTROL VOLTAGE FOR HORIZONTAL OSCILLATOR**
- **VERTICAL SYNC PULSE SEPARATOR**
- **VIDEO BLANKING FACILITY**
- **NOISE CANCELLATION IN AGC AND SYNC CIRCUITS**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 1)		16 V
Power Dissipation (Note 2)		730 mW
Operating Temperature Range		−25° C to +125° C
Storage Temperature Range	Ceramic DIP	−65° C to +150° C
Lead Temperature (Soldering)	Ceramic DIP, 60 Seconds	300° C

CONNECTION DIAGRAM

(TOP VIEW)



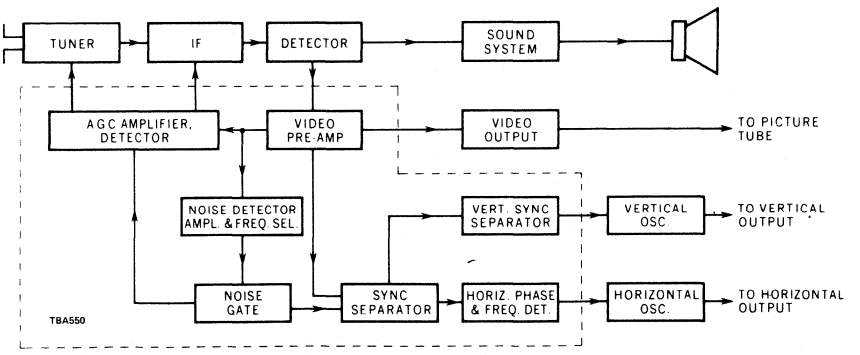
ORDERING INFORMATION

Ceramic Dual-in-line	**TBA550/6B**
Ceramic Quad-in-line	**TBA550/7H***

*Available on special request.

†Formerly referred to as μA785/TAA700

BLOCK DIAGRAM



Notes on following page.

*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_S = + 12 V, Test Circuit 1, unless otherwise specified)

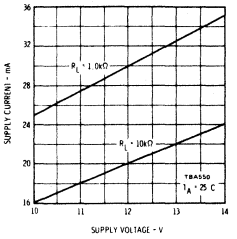
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, I_5	$R_L = \infty$, $V_{10} = 0$		19	25	mA
	R_L = 1 kΩ, $V_{10} = 0$		30		mA
VIDEO PREAMPLIFIER					
Voltage Gain			3.0		V/V
Input Resistance, R_{10}			2.7		kΩ
Input Capacitance, C_{10}				1.0	pF
Bandwidth	-3dB	5.0	14		MHz
Black Level at Video Output	$V_{10} = 2V_{P-P}$, Direct Coupled		5.0		V
Video DC Output Voltage, V_{12}	$V_{10} = 0$	8.5	9.8	10.6	V
Tracking of Video Output Voltage with Supply Variation, $\frac{\Delta V_{12}}{\Delta V_5}$	$V_{10} = 0$		0.7		V/V
Peak Video Output Current	(Note 3)		14		mA
Required Video Blanking Input Voltage Pulse, V_{11}	(Note 4)	1.0			V
Required Video Blanking Input Current Pulse, I_{11}	(Note 4)	1.0			mA
Required Flyback Gating Voltage Pulse, V_3	(Note 4)	1.0			V
Required Flyback Gating Current Pulse, I_3	(Note 4)	1.0			mA
AGC CIRCUIT					
Control Voltage at IF AGC Terminal, V_4	$V_{10} = 0V$		0		V
	$V_{10} = -2.5\ V_{DC}$		8.0		V
Control Voltage at Tuner AGC Terminal, V_6	$V_{10} = 0V$		0		V
	$V_{10} = -2.5V_{DC}$		7.0		V
SYNCHRONIZATION CIRCUIT					
AFC Operating Reference Voltage, V_2	$V_1 = 3V_{DC}$, $V_2 = 7\ V_{P-P}$, (Note 5)		7.0		V_{DC}
Vertical Sync Pulse Output, V_{15}		10	11.5		V_{P-P}
Vertical Sync Output Resistance			2.0		kΩ
Slicing Level (Percentage Below Top of Sync Pulse)	(Note 6)		30		%
NOISE GATE					
Amplitude of Noise Pulses Above Sync Tips to Activate Noise Gate	(Note 7)		0.9		V
Minimum Frequency of Noise Pulses to Activate Noise Gate	(Note 7)		3.5		MH_z
Video Input Level to reduce V_8 to 10 V			3.3		V_{PEAK}

NOTES

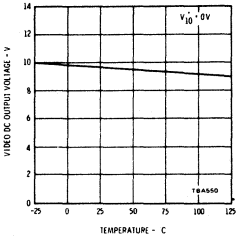
1. Rating permissible during warm-up; however, continuous maximum supply voltage is 14 volts.
2. Derate linearly at 9.1 mW/°C for ambient temperatures above 70°C.
3. Operation with R_L less than 430 Ω is not recommended.
4. The TBA550 may be operated ungated if pin 3 is connected to the positive supply line via a resistor of a suitable value (e.g. 10 kΩ). However, the following precaution should be taken: The decoupling capacitors at the i.f. and tuner control points must be larger to prevent ripple voltages due to the vertical sync pulses. As a consequence the AGC will not follow fast input signal fluctuations (airplane flutter). Since the horizontal phase detector is designed to be gated, ungated operation will result in the phase detector not operating as a frequency detector when the horizontal oscillator is out of sync. This considerably decreases the pull-in range.
5. These values apply for an oscillator-reactance stage having a control sensitivity of 400 Hz/V. This yields a hold-in range of about ±1000 Hz. If the phase detector is gated a pull-in range of about ±700 Hz is obtained without affecting the noise immunity.
6. The slicing level is independent of the video input level.
7. The noise detector of the TBA550 is frequency and amplitude selective, i.e., frequencies and noise levels above the values given will turn off the sync and AGC detectors.

TYPICAL PERFORMANCE CURVES
(TEST CIRCUIT 1 UNLESS OTHERWISE SPECIFIED)

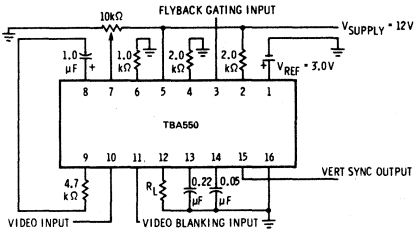
SUPPLY CURRENT VS. SUPPLY VOLTAGE



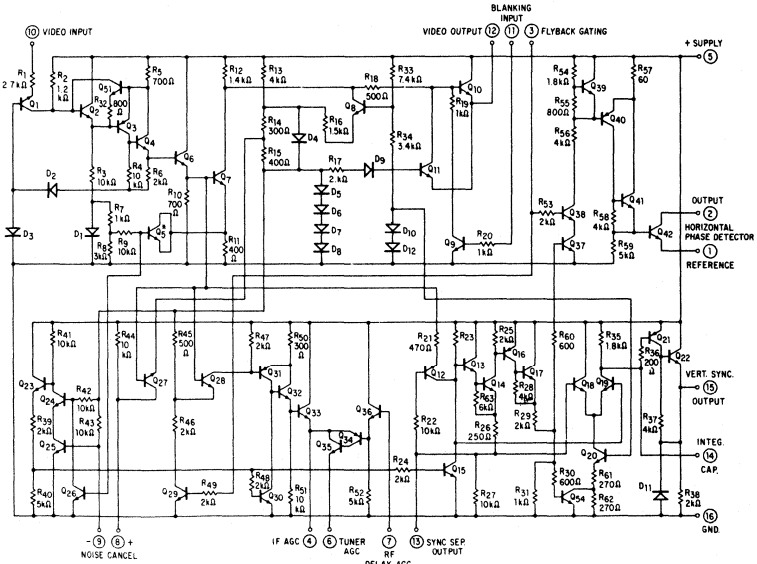
VIDEO DC OUTPUT VOLTAGE VS. TEMPERATURE



TEST CIRCUIT 1

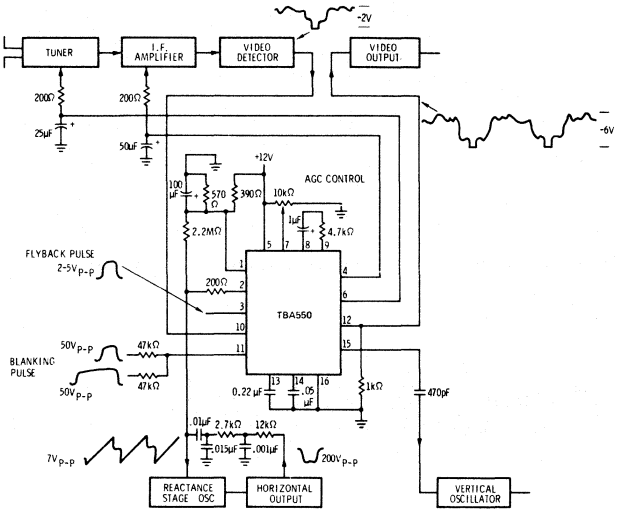


EQUIVALENT CIRCUIT



* NOTE: Q_5 IS A REVERSE BIASED E-B JUNCTION, USED AS A 5pF CAPACITOR.

TYPICAL TV RECEIVER APPLICATION



Planned New Products

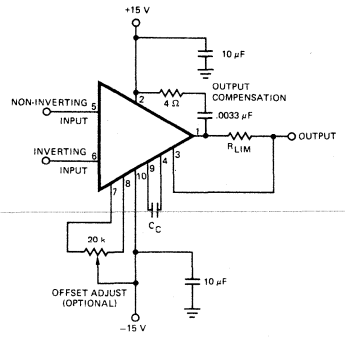
Consumer Products
Interface Elements
Voltage Comparators
Operational Amplifiers

µA791
HIGH POWER OPERATIONAL AMPLIFIER

DESCRIPTION – The µA791 is a high performance monolithic operational amplifier intended for use in a wide variety of applications including audio amplifiers, servo amplifiers, and power supplies. The high gain and high output power capability provide superior performance wherever an operational amplifier/power booster combination is required.

- **CURRENT OUTPUT TO 1 AMP**
- **SHORT CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **NO LATCH-UP**
- **LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGES**

BLOCK DIAGRAM



TBA 641B
AUDIO AMPLIFIER

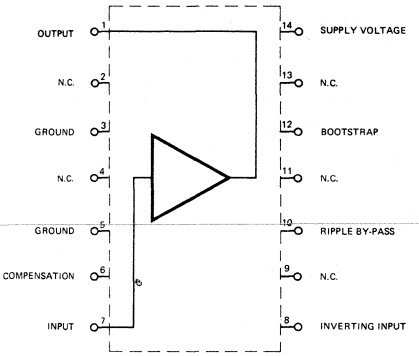
DESCRIPTION – The TBA 641B is a monolithic integrated circuit particularly designed for use as audio power amplifier in car radio and television receivers and in industrial applications which require high output power, low distortion and high reliability performance.

Special features of the circuit include a low quiescent current, self centering bias for operation at supply voltage ranging from 6 V to 16 V, direct coupling of the input.

The circuit requires a minimum number of external components.

- **OUTPUT POWER 4.5 W (14 V – 4 Ω)**
- **LOW DISTORTION**
- **LOW QUIESCENT CURRENT**
- **SELF CENTERING BIAS**
- **HIGH INPUT IMPEDANCE**
- **LOW SUPPLY VOLTAGE RANGE EXCELLENT FOR CAR RADIO APPLICATION**

BLOCK DIAGRAM



CA3075
FM IF AMPLIFIER-LIMITER, DETECTOR, AND AUDIO PREAMPLIFIER

DESCRIPTION – The CA3075 is an integrated circuit which provides, in a single monolithic chip, an FM IF subsystem for Communications and High-Fidelity Receivers. This device, consists of a multistage IF amplifier-limiter section with a Zener regulated power supply, an FM detector stage, and an AF preamplifier section.

The three-stage, emitter-follower-coupled IF amplifier section provides a 60 dB typical voltage gain at an operating frequency of 10.7 MHz and features, because of its transistor constant-current sink, an output stage with exceptionally good limiting characteristics.

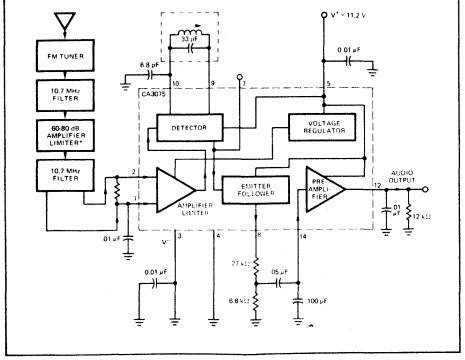
The FM detector section, which utilizes a differential-peak-detection circuit, requires only a single coil in the associated outboard detector circuit; hence, tuning the detector circuit is a simple procedure.

The audio preamplifier circuit provides a 21 dB voltage gain with low output impedance for driving subsequent audio amplifier stages.

The CA3075 utilizes a 14-lead dual in-line package.

- **GOOD SENSITIVITY: INPUT LIMITING VOLTAGE (KNEE) = 250 μV TYPICAL AT 10.7 MHz**
- **EXCELLENT AM REJECTION: 55 dB TYPICAL AT 10.7 MHz**
- **INTERNAL ZENER DIODE REGULATION FOR THE IF AMPLIFIER SECTION**
- **LOW HARMONIC DISTORTION**
- **DIFFERENTIAL PEAK DETECTION: PERMITS SIMPLIFIED SINGLE-COIL TUNING**
- **AUDIO PREAMPLIFIER VOLTAGE GAIN: 21 dB TYPICAL**
- **MINIMUM NUMBER OF EXTERNAL PARTS REQUIRED**
- **FM IF AMPLIFIER APPLICATIONS UP TO 20 MHz**

BLOCK DIAGRAM



CA3076
HIGH-GAIN WIDE-BAND IF AMPLIFIER-LIMITER

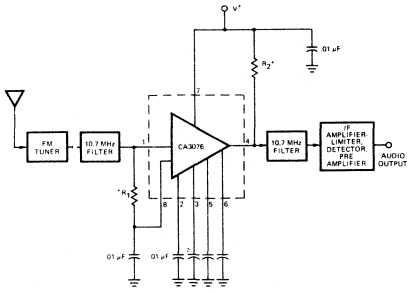
DESCRIPTION – The CA3076 monolithic integrated circuit is a high-gain wide-band amplifier-limiter for use in the IF sections of Communications and High-Fidelity FM Receivers. The CA3076 consists of a four stage IF amplifier-limiter section with a voltage regulator section.

The four-stage emitter-follower-coupled IF amplifier section provides an 80 dB voltage gain with a 2 kΩ load at a frequency of 10.7 MHz. The output stage has exceptionally good limiting characteristics because of its transistor constant-current sink. The voltage regulator section provides zener-regulated, decoupled voltages for the IF amplifier.

The CA3076 utilizes an hermetically-sealed 8-lead TO-5 type package.

- **EXCEPTIONALLY GOOD SENSITIVITY: INPUT LIMITING VOLTAGE (KNEE) = 50 μV TYPICAL AT 10.7 MHz**
- **HIGH GAIN: 80 dB WITH 2 kΩ LOAD**
- **INTERNAL VOLTAGE SUPPLY REGULATOR**
- **WIDE FREQUENCY CAPABILITY: >20 MHz**

BLOCK DIAGRAM



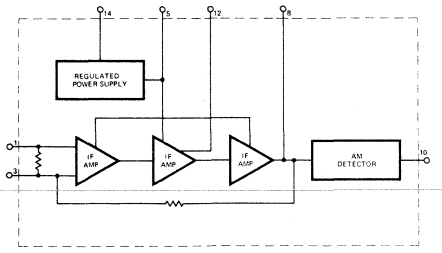
*R_1, R_2 selected for proper filter matching.

ULN2131
FM IF AMPLIFIER

DESCRIPTION – The type ULN-2131 FM Gain Block linear monolithic integrated circuit is designed for use in communications and high fidelity FM receivers. This device consists of a three-stage limiting amplifier section, a regulated power supply, an AM detector and 330 Ω input and output terminations with 7 pF shunting capacitance required for 10.7 MHz ceramic filters. Gain can be adjusted without effect on input and output conditions by addition of a fixed resistor between pins 5 and 12. The device is housed in an eight pin Mini DIP, ideally suited for saving space in the receiver.

- **THREE-STAGE LIMITING AMPLIFIER**
- **HIGH VOLTAGE GAIN**
- **REGULATED POWER SUPPLY**
- **AM DETECTOR**

BLOCK DIAGRAM

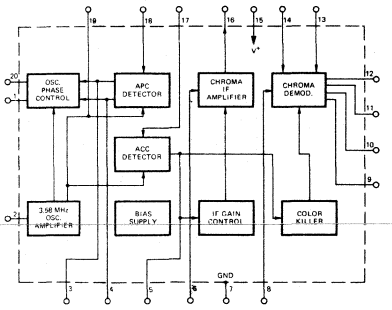


μA782
COLOR TV CHROMA PROCESSOR

DESCRIPTION – The μA782 monolithic integrated circuit performs the entire chroma processing function in a color TV receiver and provides four (4) demodulated chroma outputs. With a resistor matrix added externally to the outputs to obtain the R-Y, B-Y and G-Y signals the outputs may be used to drive direct coupled a color difference output amplifier or an RGB type output amplifier.

- **CHROMA DEMODULATION**
- **COLOR KILLING**
- **GAIN CONTROLLED CHROMA IF AMPLIFICATION**
- **SYNCHRONOUS ACC DETECTION**
- **PHASE LOCKED 3.58 MHz OSCILLATOR**
- **SYNCHRONOUS APC DETECTION**
- **BURST GATING PLUS OSCILLATOR OUTPUT BLANKING**
- **INTERNAL BIASING**
- **EXTERNAL COMPONENT COUNT GREATLY REDUCED**

BLOCK DIAGRAM



CA3066/CA3067
TELEVISION CHROMA SYSTEM

DESCRIPTION – The CA3066 and CA3067 are monolithic silicon integrated circuits that constitute a complete chroma system for color television receivers. The CA3066 provides subcarrier regeneration and total chroma signal processing prior to demodulation; the CA3067 performs the demodulation and tint control functions. Each device utilizes a 16-lead quad-in-line plastic package.

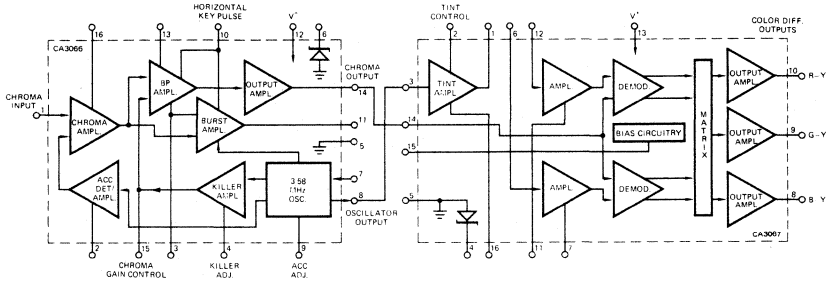
CA3066

- COMPLETE COLOR SYNC CIRCUIT
- BLANKED CHROMA AMPLIFIER
- CHROMA BAND-PASS AMPLIFIER
- LOW OUTPUT IMPEDANCE CHROMA DRIVER
- ACC DETECTOR-AMPLIFIER
- KILLER DETECTOR-AMPLIFIER
- DC CHROMA GAIN CONTROL
- ZENER DIODE FOR REGULATED VOLTAGE REFERENCE
- SHORT-CIRCUIT PROTECTION ON ALL TERMINALS

CA3067

- BALANCED CHROMA DEMODULATORS
- COLOR DIFFERENCE MATRIX
- DC TINT CONTROL
- THREE LOW OUTPUT IMPEDANCE DRIVERS FOR DIRECT COUPLING
- REFERENCE SUBCARRIER LIMITER
- ZENER DIODE FOR REGULATED VOLTAGE REFERENCE
- INTERNAL RF FILTERING

BLOCK DIAGRAM



CA3068
TELEVISION VIDEO IF SYSTEM

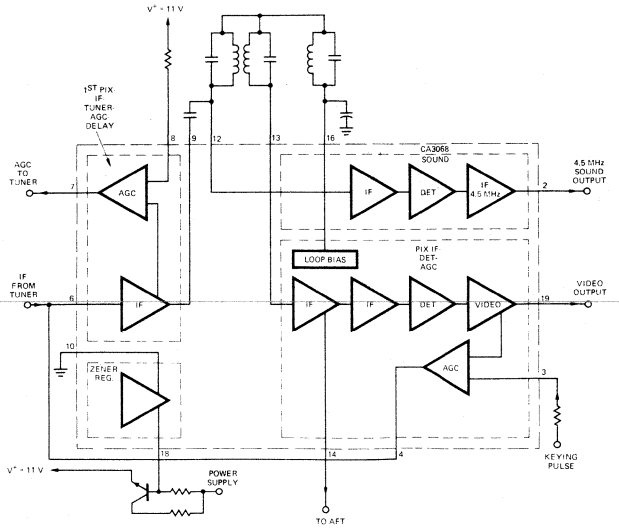
DESCRIPTION – The CA3068 is a monolithic integrated circuit that incorporates an entire video TV-IF subsystem on a single chip. Circuit innovations make it ideally suited for use in color and black-and-white TV receivers.

The primary functions performed by the IF subsystem are video IF amplification, linear detection, video output amplification, AGC from a keyed supply, AGC delay for tuner, sound carrier detection, sound carrier amplification, and a buffered AFT output. The advanced circuit design of the CA3068 also includes secondary functions for improved noise immunity and minimal airplane flutter. An isolated zener reference diode, incorporated in the IC, provides a convenient and economical means for controlling the regulated voltage supply. The inherent wide bandwidth capability (10-70 MHz) and high overall gain (87 dB) make the CA3068 suitable for other AM IF applications whose frequencies range within this bandwidth.

The CA3068 utilizes a unique 20-lead quad in-line plastic package. This package also includes a wrap-around shield that serves to minimize interlead capacitances.

- **HIGH-GAIN WIDE-BAND IF AMPLIFIER: 75 dB TYPICAL AT 45 MHz**
- **GAIN REDUCTION WITH EXCELLENT STABILITY: 50 dB TYPICAL AT 45 MHz**
- **VIDEO DETECTOR WITH LINEAR CHARACTERISTICS**
- **VIDEO AMPLIFIER; 12 dB GAIN**
- **IMPULSE NOISE LIMITER**
- **KEYED AGC WITH NOISE IMMUNITY CIRCUITS**
- **DELAYED AGC FOR TUNER**
- **BUFFERED AFT OUTPUT**
- **SEPARATE SOUND IF INTERCARRIER AMPLIFICATION**
- **SOUND CARRIER DETECTOR**
- **4.5 MHz SOUND CARRIER AMPLIFIER**
- **ISOLATED ZENER REFERENCE DIODE FOR REGULATED VOLTAGE SUPPLY**

BLOCK DIAGRAM

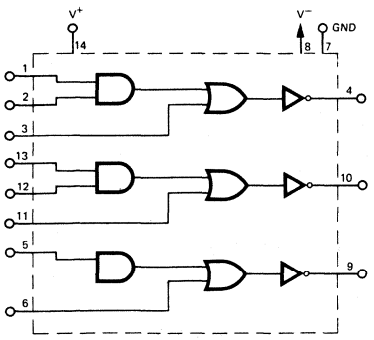


µA9616
TRIPLE EIA RS-232-C LINE DRIVER

DESCRIPTION – The µA9616 is a Triple EIA RS-232-C Line Driver which meets the specifications of EIA RS-232-C and CCIT V.24. External capacitors have been eliminated by internal slew rate limiting. All outputs are protected against RS-232-C fault conditions. A true inhibit function as required by the user has been provided. All inputs including the inhibit function are TTL compatible.

- **THREE CHANNELS PER PACKAGE**
- **NO EXTERNAL CAPACITORS REQUIRED FOR SLEW RATE LIMITING**
- **MEETS ALL RS-232-C SPECIFICATIONS**
- **TRUE INHIBIT FUNCTION**
- **MULTIPLE INPUTS**
- **MEETS CCITT V-24 SPECIFICATIONS**

BLOCK DIAGRAM

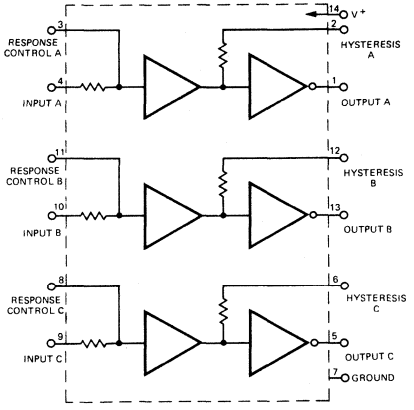


µA9617
TRIPLE EIA RS-232-C LINE RECEIVER

DESCRIPTION – The µA9617 is a triple line receiver designed to meet the terminator electrical requirements of EIA RS-232-C and CCITT V.24. It receives line signals produced by the µA9616, an EIA/CCIT driver, and converts them to TTL compatible logic levels. The inputs have a resistance between 3 kΩ and 7 kΩ and can withstand ±25 V. Each receiver can operate in either hysteresis or non-hysteresis (slicing) modes, and each receiver provides fail-safe operation as defined by Section 2.5 of RS-232-C. Noise immunity may be increased by connecting a capacitor between the response control pin and ground.

- **MEETS ALL EIA RS-232-C AND CCITT V.24 SPECIFICATIONS**
- **FAIL-SAFE OPERATION**
- **HYSTERESIS OR NON-HYSTERESIS MODE**
- **INDIVIDUAL RESPONSE CONTROLS**
- **TTL COMPATIBLE OUTPUT**
- **SINGLE +5 V SUPPLY**

BLOCK DIAGRAM

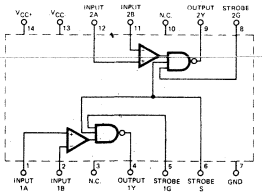


SN55/75107
SN55/75108
DUAL LINE RECEIVERS

DESCRIPTION – The SN55/75107 and SN55/75108 are high-speed, two channel line receivers with common voltage supply and ground terminals. They are designed to detect input signals of 25 mV (or greater) amplitude and convert the polarity of the signal into appropriate TTL-compatible output logic levels. They feature high input impedance and low input currents which induce very little loading on the transmission line making these devices ideal for use in party line systems. The receiver input common mode voltage range is ±3 V but can be increased to ±15 V by the use of input attenuators. Separate or common strobes are available. The SN55/75107 circuit features an active pull-up (totem pole output). The SN55/75108 circuit features an open collector output configuration that permits wired-OR connections. The receivers are designed to be used with the SN55/75109 and SN55/75110 line drivers. The SN55/75107 and SN75108 line receivers are useful in high-speed balanced, unbalanced and party line transmission systems and as data comparators.

- **HIGH SPEED**
- **STANDARD SUPPLY VOLTAGES**
- **DUAL CHANNELS**
- **HIGH COMMON-MODE REJECTION RATIO**
- **HIGH INPUT IMPEDANCE**
- **HIGH INPUT SENSITIVITY**
- **INPUT COMMON-MODE VOLTAGE RANGE OF ±3 V**
- **SEPARATE OR COMMON STROBES**
- **TTL OR DTL DRIVE CAPABILITY**
- **WIRED-OR OUTPUT CAPABILITY**
- **HIGH D-C NOISE MARGINS**

BLOCK DIAGRAM



SN55/75109
SN55/75110
DUAL LINE DRIVERS

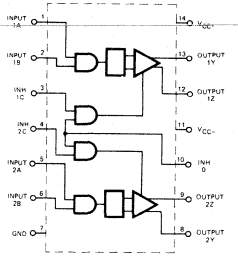
DESCRIPTION – The SN55/75109 and SN55/75110 are dual line drivers featuring independent channels with common voltage supply and ground terminals. The significant difference between the two drivers is in the output-current specification. The driver circuits feature a constant output current that is switched to either of two output terminals by the appropriate logic levels at the input terminals. The output current can be switched off (inhibited) by appropriate logic levels on the inhibit inputs. The otuput current is nominally 6 mA for the SN55/75109 and 12 mA for the SN55/75110. System design determines which driver is best suited to a particular application.

The inhibit feature is provided so the circuits can be used in party-line or data-bus applications. A strobe or inhibitor, common to both drivers, is included for increased driver-logic versatility. The output current in the inhibited mode, $I_{O(off)}$, is specified so that minimum line loading is induced when the driver is used in a party-line system with other drivers. The otuput impedance of the driver in the inhibited mode is very high—the output impedance of a transistor biased to cutoff.

The driver otuputs have a common-mode voltage range of −3 volts to +10 volts, allowing common-mode voltage on the line without affecting driver performance.

- **HIGH SPEED**
- **STANDARD SUPPLY VOLTAGES**
- **DUAL CHANNELS**
- **TTL INPUT COMPATIBILITY**
- **CURRENT-MODE OUTPUT (6 mA or 12 mA TYPICAL)**
- **HIGH OUTPUT IMPEDANCE**
- **HIGH COMMON-MODE OUTPUT VOLTAGE RANGE (−3 V TO 10 V)**
- **INHIBITOR AVAILABLE FOR DRIVER SELECTION**

BLOCK DIAGRAM



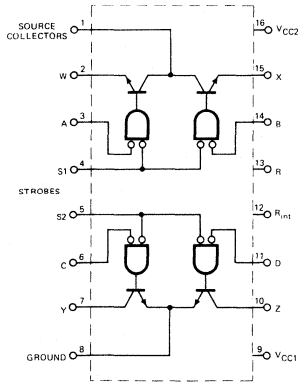
SN75325
MEMORY DRIVER

DESCRIPTION - The SN77325 is a monolithic integrated circuit memory driver with logic inputs and is designed for use with magnetic memories.

The devices contain two 600 mA source-switch pairs and two 600 mA sink-switch pairs. Source selection is determined by one of two logic inputs, and source turn-on is determined by the source strobe. Likewise, sink selection is determined by one of two logic inputs, and sink turn-on is determined by the sink strobe. This arrangement allows selection of one of the four switches and its subsequent turn-on with minimum time skew of the output current rise.

- **600 mA OUTPUT CAPABILITY**
- **FAST SWITCHING TIMES**
- **OUTPUT SHORT-CIRCUIT PROTECTION**
- **DUAL SINK AND DUAL SOURCE OUTPUTS**
- **MINIMUM TIME SKEW BETWEEN ADDRESS AND OUTPUT CURRENT RISE**
- **24 VOLT OUTPUT CAPABILITY**
- **SOURCE BASE DRIVE EXTERNALLY ADJUSTABLE**
- **TTL OR DTL COMPATIBILITY**
- **INPUT CLAMPING DIODES**
- **TRANSFORMER COUPLING ELIMINATED**
- **RELIABILITY INCREASED**
- **DRIVE-LINE LENGTHS REDUCED**
- **USE OF EXTERNAL COMPONENTS MINIMIZED**

LOGIC DIAGRAM



SN75451
DUAL PERIPHERAL DRIVERS

DESCRIPTION – The SN75451 is a versatile general purpose dual interface driver circuit that employs TTL or DTL logic. The SN75451 features two standard series 74 TTL gates and two high current, high voltage transistors which offer the system designer the flexibility to tailor the circuit to his application. The power output transistor is internally connected to the TTL gate but the collector remains uncommitted for high voltage applications. The SN75451 is useful in high speed logic buffers, power drivers, lamp drivers, relay drivers, line drivers, MOS drivers, clock drivers and memory drivers. The SN75451 is offered in a low cost mini-DIP package.

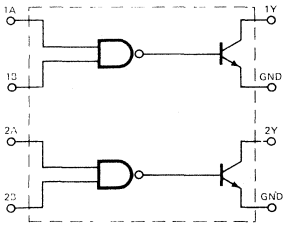
- **HIGH SPEED**
- **300 mA CURRENT CAPABILITY**
- **HIGH VOLTAGE CAPABILITY**
- **TTL OR DTL INPUT COMPATIBILITY**

TRUTH TABLE

A	B	Y
L	L	L (on state)
L	H	L (on state)
H	L	L (on state)
H	H	H (off state)

H = High Level, L = Low Level

LOGIC DIAGRAM

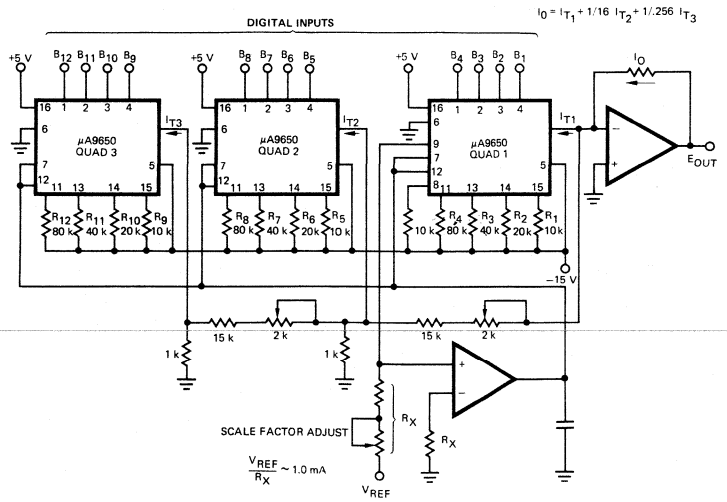


µA9650
4-BIT D/A AND A/D CURRENT SOURCE

DESCRIPTION – The µA9650 is a high speed, 4-bit precision current source, intended for use in D/A and A/D converters with up to 12-bit accuracy. It consists of a reference transistor and 4 logic operated precision current sources connected to a single output summing line. Logic inputs are fully TTL compatible.

- **200 ns SETTLING TIME (12 ± 1/2 LSB)**
- **STANDARD SUPPLY LEVELS**
- **VARIABLE BIT CURRENTS**
- **REFERENCE COMPENSATION**
- **TTL COMPATIBLE**

TYPICAL 12-BIT DIGITAL-TO-ANALOG CONVERTER



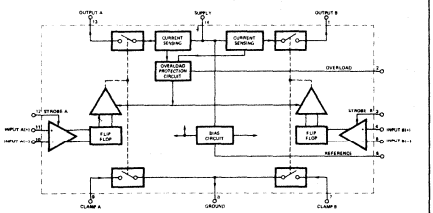
μA750
DUAL HIGH CURRENT COMPARATOR

DESCRIPTION – The μA750 is a dual high current comparator. The two comparators function completely independent; each has strobing capability, built-in hysteresis for positive switching, output current sinking capability and a high current source. The dual comparator operates over a wide supply range, has a separate reference voltage available for external circuitry bias and has adjustable excess current and chip temperature protection.

The device is designed for systems requiring dual comparator functions such as air conditioners, two-direction position controls and window detectors. Although primarily intended for systems with high load currents, the device will reduce package count in all systems using more than one comparator. Both comparator and strobe inputs are TTL compatible.

- **HIGH OUTPUT SOURCING CURRENT CAPABILITY**
- **POSITIVE SWITCHING BY MEANS OF BUILT-IN HYSTERESIS**
- **OUTPUT CURRENT SINKING CAPABILITY**
- **THERMAL AND EXCESS-CURRENT PROTECTIVE SHUT-DOWN, RESETTABLE BY INTERRUPTING SUPPLY CURRENT**
- **WIDE SUPPLY VOLTAGE RANGE**
- **REFERENCE VOLTAGE OUTPUT FOR ADDED CONVENIENCE**
- **OPERATES FROM SINGLE SUPPLY**

BLOCK DIAGRAM

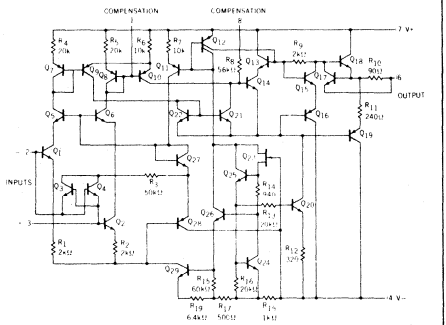


LM108/108A SERIES
HIGH PRECISION OPERATIONAL AMPLIFIER

DESCRIPTION – The LM108 series are high-precision operational amplifiers. Extremely high input impedance coupled with low noise input offsets and temperature drift are made possible through use of high-beta processing, making the device suitable for applications requiring high accuracy and low drift performance. The LM108A series is specially selected for extremely low offset voltage and drift, and high common mode rejection, making possible superior performance in applications where offset nulling is undesirable. Increased slew rate without performance compromise is available through use of feedforward compensation techniques, maximizing performance in high speed sample-and-hold circuits and precision high speed summing amplifiers, while the wide supply range and excellent supply voltage rejection assure maximum flexibility in voltage follower, summing, and general feedback applications.

- **GUARANTEED LOW INPUT CHARACTERISTICS**
- **HIGH INPUT IMPEDANCE**
- **LOW OFFSET CURRENT – 400 pA MAXIMUM**
- **LOW BIAS CURRENTS – 3.0 nA MAXIMUM**
- **OPERATION OVER WIDE SUPPLY RANGE**

EQUIVALENT CIRCUIT



Dice

LINEAR INTEGRATED CIRCUIT DICE POLICY

General Information

Fairchild Linear Integrated Circuits is proud to offer the most complete line of circuits in dice form in the industry. All are constructed using the Fairchild Planar* Epitaxial process. The chips are identical to those used in standard Fairchild assembled products.

These linear dice can be conveniently used in hybrid or module designs where size and cost savings are required.

Electrical Characteristics

Each chip is electrically tested at 25°C to DC parameters as evidenced by the probe marks on the bonding pads.

Quality Assurance

All Fairchild linear dice are visually inspected and conform to MIL-STD-883 Method 2010.1 Condition B as a minimum to a quality control level of 1-1/2% AQL.

As an aid to die attach, each die is gold backed. For protection in handling and assembly, each die has a glassivated coating over the metalization. Only the bonding pads are exposed.

Chip geometries and manufacturing processes may be improved periodically. However, such changes will not affect the electrical characteristics of the circuits.

Shipping Packages

Linear dice are packaged in containers with an anti-static sheet inserted between the lid and the dice. This anti-static sheet guards against electrostatic damage during shipment and storage.

The clear plastic carrier allows visual inspection of all the packaged dice. Each carrier is heat sealed within a transparent bag. A small piece of dehydrator paper with humidity indicating color is inserted in each bag prior to sealing.

Ordering Information

Minimum order quantity is 100 chips. All orders above 100 peices must be in 100 piece multiples.

Each Linear Integrated Circuit chip has its own 10 digit product code which completely describes the family, device type, and device number. The meaning of the digits and their position are as follows:

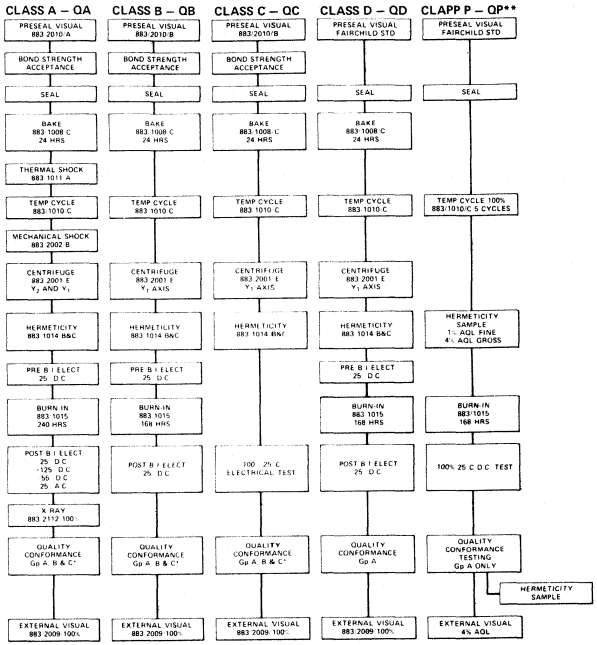
1. Generic Device Type – UXX7741XXD – Microcircuit
2. Microcircuit Family – UXX7741XXD – Linear Device
3. Device Number – UXX7741XXD – Device Type
4. Dice Indicator – UXX7741XXD – Dice

Note: The XX designation replaces the package type and temperature range.

*Planar is a patented Fairchild process.

Hi-Rel Unique 38510

PROCESS SUMMARY



* Group "B" is performed by generic type every 6 weeks.
Group "C" is performed by generic type every 12 weeks.

** "QP" devices are essentially Fairchild Standard product with 168 hr burn-in.
Fine leak is performed to an LTPD of "10" and gross leak is performed to an LTPD of "3". Flatpak have the following additional processing: Bake 883/1008/C 24 hrs and Centrifuge 883/2001/E.

The UNIQUE 38510 Program is written in accordance with MIL-M-38510 and MIL-STD-883. The Program establishes quality and reliability screening requirements to match the particular screening level required by the application.

The UNIQUE 38510 General Specification establishes the controls and reliability assurance levels for product screening. Five levels – QA, QB, QC, QD, and QP – of product screening are available.

Detailed electrical and specific device characteristics are specified for each family of devices in the Detail Specification.

FAMILY	DETAIL SPECIFICATION
Operational Amplifier	UNIQUE 38510/A1
Comparators	UNIQUE 38510/A2
Voltage Regulators	UNIQUE 38510/A3
Interface Circuits	UNIQUE 38510/12

The UNIQUE 38510 General Specification and Detail Specification are available upon request.

Devices available on the Program and marking are detailed on Page 302. For other LIC products that can be processed per the UNIQUE 38510 Program, check with your local Fairchild Sales Office.

QB and QP processed product is stocked for immediate delivery. Check with your local Fairchild Distributor or Fairchild Sales Office for delivery.

Qualified Products Code:

1st	Digit	Q	Indicates Qualified Line
2nd	Digit	A	Indicates Class A part
		B	Indicates Class B part
		C	Indicates Class C part
		D	Indicates Class D part (see para. 6.5)
		P	Indicates Class D Part (see para 6.5.1)
3rd	Digit	X	Part of four-digit code indicating die type
4th	Digit	X	
5th	Digit	X	
6th	Digit	X	

Number Options: These options apply to operations performed on each unit delivered:

OPTION 1	Lead form to dimensions in detail specification, followed by hermetic seal tests.
OPTION 2	Hot solder dip finish
OPTION 3	Read and record critical parameters before and after burn-in.
OPTION 4	Initial qualification, Group B&C quality conformance not required.
OPTION 5	Radiographic inspection shall be performed on all devices.
OPTION 6	Special marking required.
OPTION 7	Non-conforming variation—refer to procurement documents for details (must be negotiated with factory).

Letter Options: These options apply once per Purchase Order or line item and are considered Test Charges:

OPTION A	Group B testing shall be performed on customer's parts.
OPTION B	Group C testing shall be performed on customer's parts.
OPTION C	Generic data to be supplied from the latest completed lot.
OPTION D	UNIQUE 38510 program plan, pertinent to the device family being purchased, shall be supplied.

Ordering Information

DEVICE	PACKAGE See outline drawing section.	ORDER NUMBER			
		0°C to +70°C	−55°C to +125°C	−20°C to +85°C	DICE (+25°C)
μA702	3F		U3F7702312		
	5B	U5B7702393	U5B7702312		
	6A	U6A7702393	U6A7702312		
	DICE				UXX7703XXD
μA703	5Z	U5Z7703394			
	DICE				UXX7703XXD
μA709	3F		U3F7709311 U3F7709312		
	5B	U5B7709393	U5B7709311 U5B7709312		
	6A	U6A7709393	U6A7709311 U6A7709312		
	DICE				UXX7709XXD
μA710	3F		U3F7710312		
	5B	U5B7710393	U5B7710312		
	6A	U6A7710393	U6A7710312		
	DICE				UXX7710XXD
μA711	3F		U3F7711312		
	5F	U5F7711393	U5F7711312		
	6A	U6A7711393	U6A7711312		
	DICE				UXX7711XXD
μA715	5F	U5F7715393	U5F7715312		
	6A	U6A7715393	U6A7715312		
	DICE				UXX7715XXD
μA716	5B	U5B7716393			
	DICE				UXX7716XXD
μA722	3M			U3M7722333 U3M7722334	
	DICE				UXX7722XXD
μA723	5R	U5R7723393	U5R7723312		
	6A	U6A7723393	U6A7723312		
	9A	U9A7723393			
	DICE				UXX7723XXD

DEVICE	PACKAGE See outline drawing section.	0°C to +70°C	−55°C to +125°C	−20°C to +85°C	DICE (+25°C)
μA725	5T	U5T7725393	U5T7725312	U5T7725333	
	6A	U6A7725393	U6A7725312	U6A7725333	
	DICE				UXX7725XXD
		(0° TO +85°C)			
μA726	5U	U5U7726323	U5U7726312		
	DICE				UXX7726XXD
μA727	5U		U5U7727312	U5U7727333	
	DICE				UXX7727XXD
μA729	6A	U6A7729394			
	DICE				UXX7729XXD
μA730	5B	U5B7730393	U5B7730312		
	DICE				UXX7730XXD
μA732	6A	U6A7732394			
	DICE				UXX7732XXD
μA733	3F		U3F7733312		
	5F	U5F7733393	U5F7733312		
	6A	U6A7733393	U6A7733312		
	DICE				UXX7733XXD
μA734	5F	U5F7734393	U5F7734312		
	6A	U6A7734393	U6A7734312		
	9A	U9A7734393			
	9T	U9T7734393			
	DICE				UXX7734XXD
μA739	6A	U6A7739393			
	DICE				UXX7739XXD
μA740	5B	U5B7740393	U5B7740312		
μA741	3F		U3F7741312		
	5B	U5B7741393	U5B7741312		
	6A	U6A7741393	U6A7741312		
	9A	U9A7741393			
	9T	U9T7741391			
	DICE				UXX7741XXD
μA742	6A	U6A7742393			
μA746	5E	U5E7746394			
	6A	U6A7746394			
	DICE				UXX7746XXD
μA747	5F	U5F7747393	U5F7747312		
	7A	U7A7747393	U7A7747312		
	DICE				UXX7747XXD
μA748	3F		U3F7748312		
	5B	U5B7748393	U5B7748312		
	6A	U6A7748393	U6A7748312		
	9T	U9T7748393			
	DICE				UXX7748XXD

DEVICE	PACKAGE See outline drawing section.	ORDER NUMBER			
		0°C to +70°C	−55°C to +125°C	−20°C to +85°C	DICE (+25°C)
μA749	5B 6A DICE	U5B7749394 U6A7749393	U6A7749312		UXX7749XXD
μA754	5E 6A DICE	U5E7754394 U6A7754394			UXX7754XXD
μA757	6A DICE	U6A7757393	U6A7757312		UXX7757XXD
μA760	5B 6A 9T DICE	U5B7760393 U6A7760393 U9T7760393	U5B7760312 U6A7760312		UXX77603XXD
μA767	6A	U6A7767394			
μA776	5B 6A	U5B7776393 U6A7776393	U5B7776312 U6A7776312		
μA777	5B 6A 9T DICE	U5B7777393 U6A7777393 U9T7777393	U5B7777312 U6A7777312		UXX7777XXD
μA780	6B DICE	U6B7780394			UXX7780XXD
μA781	6A DICE	U6A7781394			UXX7781XXD
μA795	6A	U6A7795393			
μA796	5E 6A DICE	U5E7796393 U6A7796393	U5E7796312 U6A7796312		UXX7796XXD
μA7805	GH GJ	UGH7805393 UGJ7805393			
μA7806	GH GJ	UGH7806393 UGJ7806393			
μA7808	GH GJ	UGH7808393 UGJ7808393			
μA7812	GH GJ	UGH7812393 UGJ7812393			
μA7815	GH GJ	UGH7815393 UGJ7815393			
μA7818	GH GJ	UGH7818393 UGJ7818393			
μA7824	GH GJ	UGH7824393 UGJ7824393			

DEVICE	PACKAGE See outline drawing section,	0°C to +75°C	−55°C to +125°C	−40°C to +85°C	DICE (+25°C)
μA9614	4L 7B DICE	U4L961459X U7B961459X	U4L961451X U7B961451X		UXX9614XXD
μA9615	4L 7B DICE	U4L961559X U7B961559X	U4L961551X U7B961551X		UXX9615XXD
μA9620	3I 6A DICE	U3I962059X U6A962059X	U3I962051X U6A962051X		UXX9620XXD
μA9621	3I 6A DICE	U3I962159X U6A962159X	U3I962151X U6A962151X		UXX9621XXD
μA9622	3I 6A DICE	U3I962259X U6A962259X	U3I962251X U6A962251X		UXX9622XXD
μA9624	3I 6A DICE	U3I962459X U6A962459X	U3I962451X U6A962451X		UXX9624XXD
μA9625	3I 6A DICE	U3I962559X U6A962559X	U3I962551X U6A962551X		UXX9625XXD
μA9644	7B	U7B964459X	U7B964451X		

DEVICE	PACKAGE See outline drawing section,	0°C to +70°C	−55°C to +125°C	−40°C to +85°C	DICE (+25°C)
CA3018	5G DICE		CA3018		UXX7018XXD
CA3018A	5G		CA3018A		
CA3019	5E DICE		CA3019		UXX7019XXD
CA3026	5G DICE		CA3026		UXX7026XXD
CA3036	5E DICE		CA3036		UXX7036XXD
CA3039	5G DICE		CA3039		UXX7039XXD
CA3045	6A DICE		CA3045		UXX7045XXD

DEVICE	PACKAGE See outline drawing section,	0°C to +70°C	−55°C to +125°C	−40°C to +85°C	DICE (+25°C)
CA3046	6A	CA3046			
CA3054	6A DICE	CA3054			UXX7054XXD
CA3064	5A			CA3064/5A	
CA3065	7F			CA3065/7F	
LM101D	6A		LM101D		
LM101H	5B		LM101H		
LM101AD	6A		LM101AD		
LM101AF	3F		LM101AF		
LM101AH	5B		LM101AH		
LM201D	6A	LM201D			
LM201H	5B	LM201H			

DEVICE	PACKAGE See outline drawing section,	0°C to +70°C	−55°C to +125°C	−20°C to +85°C	DICE (+25°C)
LM201AD	6A			LM201AD	
LM201AF	3F			LM201AF	
LM201AH	5B			LM201AH	
LM301A	DICE				UXX7101XXD
LM301AD	6A	LM301AD			
LM301AH	5B	LM301AH			
LM301AN	9T	LM301AN			
LM109K	GJ		LM109K		
LM209K	GJ			LM209K	
LM309K	GJ	LM309K			
SN7524J	7B	SN7524J			
SN7525	DICE				UXX7525XXD
SN7525J	7B	SN7525J			
SN75450J	6A	SN75450J			
TAA630 (Formerly μA786)	6A 7F	TAA630/6A TAA630/7F			
TAA640 (Formerly μA784)	6A 7F	TAA640/6A TAA640/7F			
TBA550 (Formerly μA785/TAA700)	6B 7H	TBA550/6B TBA550/7H			

Glossary

FAIRCHILD LINEAR INTEGRATED CIRCUIT GLOSSARY

ABSOLUTE ERROR – The worst-case deviation from a straight line drawn through zero and the 25°C value of the full-scale output current.

ACC DETECTOR SENSITIVITY – The ratio of the incremental differential DC voltage change at the ACC Detector Output Terminals to the incremental change in peak-to-peak voltage at the ACC Detector Input Terminal for a specified burst input level, with the local oscillator locked.

ACQUISTION TIME – The time from change of input until last time output exceeds specified percent of final value.

APC DETECTOR SENSITIVITY – The ratio of the incremental differential DC voltage change at the APC Detector Output Terminals to the incremental change in relative phase at the APC Detector Input Terminal for a specified burst input level.

AVERAGE INPUT OFFSET CURRENT DRIFT – The change in input offset current divided by the change in ambient temperature producing it.

AVERAGE INPUT OFFSET VOLTAGE DRIFT – The change in input offset voltage divided by the change in ambient temperature producing it.

AVERAGE TEMPERATURE COEFFICIENT OF INPUT OFFSET CURRENT – The ratio of the change in Input Offset Current over the operating temperature range to the temperature range.

AVERAGE TEMPERATURE COEFFICIENT OF INPUT OFFSET VOLTAGE – The ratio of the change in Input Offset Voltage over the operating temperature range to the temperature range.

AVERAGE TEMPERATURE COEFFICIENT OF OUTPUT VOLTAGE – The percentage change in output voltage for a specified change in ambient temperature.

BANDWIDTH – The frequency at which the differential gain is 3 dB below its low frequency value.

CLOSED LOOP VOLTAGE GAIN ERROR – Deviation from the theoretical closed loop voltage gain due to finite open loop voltage gain and input resistance, and non-zero output resistance.

COLOR-DIFFERENCE DEMODULATION ANGLE – A color-difference demodulation angle is defined as the instantaneous phase of the (+) Chroma input signal which produces the most positive voltage at the respective color-difference output with the phase of Reference "A" taken at 3 degrees and the phase of Reference "B" taken at 106 degrees.

(+) CHROMA INPUT – A composite chroma signal containing the burst at a phase of 180 degrees is demodulated to produce specified color-difference demodulation angles when applied to the (+) Chroma input.

(–) CHROMA INPUT – A composite chroma signal containing the burst at a phase of 0 degrees is demodulated to produce specified color-difference demodulation angles when applied to the (–) Chroma input.

COMMON MODE FIRING VOLTAGE – The CM input voltage that exceeds the dynamic range of the inputs with strobe enabled resulting in the output switching states.

COMMON MODE GAIN – A ratio of the differential output voltage to the change in applied input common mode voltage.

COMMON MODE INPUT RESISTANCE – The resistance looking into both inputs tied together.

COMMON MODE RECOVERY TIME – The time from the turn off of the CM signal to the analog input threshold of the earliest sense line pulse signal that can be processed normally. Processed normally refers to bi-polar signals greater than or less than the input threshold with a corresponding proper output.

DIFFERENTIAL INPUT VOLTAGE RANGE – The range of voltage between the input terminals for which operation within specifications is assured.

DIFFERENTIAL LOAD REJECTION – The ratio of the change in input offset voltage to the change in differential load current producing it.

DIFFERENTIAL INPUT RESISTANCE – The resistance looking into either input terminal with the other grounded.

DIFFERENTIAL OUTPUT VOLTAGE SWING – The peak differential output swing that can be obtained without clipping.

DIFFERENTIAL VOLTAGE GAIN – The ratio of the change in differential output voltage to the change in differential input voltage producing it.

DROPOUT VOLTAGE – The input-output voltage differential at which the circuit ceases to regulate against further reductions in input voltage.

EQUIVALENT INPUT COMMON MODE NOISE VOLTAGE – The change in input offset voltage due to common mode input noise.

EQUIVALENT INPUT RIPPLE VOLTAGE – The change in input offset voltage due to ripple on the applied supply voltage.

FULL SCALE OUTPUT CURRENT – The output current for all bits turned on.

GAIN MAXIMUM AVAILABLE (GMA) – This gain figure is the theoretical maximum power gain of an amplifier with conjugate matching at both the input and the output terminals and assumes no reverse transadmittance (feedback component) in the amplifier.

GAIN MAXIMUM STABLE (GMS) – This gain figure gives the maximum possible gain based on stability criteria only. This gain figure does not necessarily represent the realizable power gain of an amplifier. For unneutralized amplifiers, the maximum power gain realizable based on normal circuit tolerance is either (GMS - 6.0 dB) or GMA, whichever is smaller.

INPUT BIAS CURRENT – The average of the two input currents.

INPUT CAPACITANCE – The capacitance looking into either input terminal with the other grounded.

INPUT COMMON MODE REJECTION RATIO – The ratio of the input voltage range to the maximum change in input offset voltage over this range.

INPUT NOISE VOLTAGE – The square root of the mean square narrow-band noise voltage at the output divided by the measurement system gain with low source resistance.

INPUT OFFSET CURRENT – The difference in the currents into the two input terminals with the output at zero volts.

INPUT OFFSET VOLTAGE – That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT-OUTPUT VOLTAGE DIFFERENTIAL – The range of voltage difference between the supply voltage and the regulated output voltage over which the regulator will operate.

INPUT RESISTANCE – The resistance looking into either input terminal with the other grounded.

INPUT VOLTAGE RANGE – The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

LARGE-SIGNAL VOLTAGE GAIN – The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

LINEARITY ERROR – The deviation from the theoretical response.

LINE REGULATION – The percentage change in output voltage for a specified change in input voltage.

LOAD REGULATION – The percentage change in output voltage for a specified change in load current.

LOGIC INPUT HIGH VOLTAGE – The minimum voltage allowed at a bit control gate to hold the bit off.

LOGIC INPUT LOW VOLTAGE – The maximum voltage allowed at a bit control gate to hold the bit on.

LONG TERM STABILITY – Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and power dissipation.

MAXIMUM POWER DISSIPATION – The maximum total device dissipation for which the regulator will operate within specifications.

NEGATIVE OUTPUT LEVEL – The DC output voltage in the negative direction with the input voltage equal to or greater than a minimum specified amount.

NEGATIVE SUPPLY CURRENT – The current required from the negative power supply to operate the device with no load.

OSCILLATOR CONTROL SENSITIVITY – The ratio of the incremental change in oscillator free running frequency to the incremental change in the differential DC voltage at the APC Detector Output Terminals.

OUTPUT COMMON MODE VOLTAGE – The average of the voltages at the two output terminals.

OUTPUT OFFSET VOLTAGE – The difference between the voltages at the two output terminals with the inputs grounded.

OUTPUT NOISE VOLTAGE – The rms output noise voltage with constant load and no input ripple.

OUTPUT RESISTANCE – The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

OUTPUT SHORT-CIRCUIT CURRENT – The maximum output current available from the amplifier with the output shorted to ground or to either supply.

OUTPUT SINK CURRENT – The maximum negative current that can be delivered by the comparator.

OUTPUT VOLTAGE RANGE – The range of output voltage over which the regulator will operate.

OUTPUT VOLTAGE SWING – The peak output swing, referred to zero, that can be obtained without clipping.

PEAK OUTPUT CURRENT – The maximum current that may flow into the output load without causing damage to the comparator.

POSITIVE OUTPUT LEVEL – The DC output voltage in the positive direction with the input voltage equal to or greater than a minimum specified amount.

POSITIVE SUPPLY CURRENT – The current required from the positive power supply to operate the device with no load.

POWER CONSUMPTION – The DC power required to operate the amplifier with the output at zero and with no load current.

PROPAGATION DELAY – The interval between the application of an input voltage step and its arrival at either output, measured at 50% of the final value.

QUIESCENT CURRENT – That part of input current to the regulator that is not delivered to the load.

REFERENCE VOLTAGE – The output of the reference amplifier measured with respect to the negative supply.

RESPONSE TIME – The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage overdrive.

RIPPLE REJECTION – The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

RISE TIME – The time required for an output voltage step to change from 10% to 90% of its final value.

SENSE VOLTAGE – The voltage between current sense and current limit terminals necessary to cause current limiting.

SETTING TIME – The time from output first reaching final value until last time output exceeds specified percent of final value.

SHORT CIRCUIT CURRENT LIMIT – The output current of the regulator with the output shorted to the negative supply.

SLEW RATE – The maximum rate of change of output under large signal condition.

STANDBY CURRENT DRAIN – The supply current drawn by the regulator with no output load and no reference voltage load.

STROBE CURRENT – The maximum current drawn by the strobe terminals when it is at the zero logic level.

STROBE DELAY – The time delay measured from strobe to output threshold with a signal present exceeding the input threshold.

STROBE RELEASE TIME – The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from the zero to the one logic level. Appropriate input conditions are assumed.

STROBED OUTPUT LEVEL – The DC output voltage, independent of input voltage, with the voltage on the strobe terminal equal to or less than a minimum specified amount.

SUPPLY CURRENT – The current required from the power supply to operate the amplifier with no load and the output at zero.

SUPPLY REGULATION – The change in voltage at the Supply Terminal for a specified change in the V^+ voltage.

SUPPLY VOLTAGE REJECTION RATIO – The ratio of the change in input offset voltage to the change in supply voltage producing it.

SWITCHING SPEED – The time required to turn on the least significant bit.

TEMPERATURE STABILITY OF VOLTAGE GAIN – The maximum variation of the voltage gain over the specified temperature range.

THRESHOLD UNCERTAINTY – With all sense amps sharing the same input threshold less the uncertainty as a "0". This includes unit to unit, power supply and temperature variations.

THRESHOLD VOLTAGE – The typical referred to input voltage which determines whether an input is a "1" or a "0". A signal whose magnitude is greater than the threshold level is sensed as a logic "1" and a signal whose magnitude is less as a "0".

TOTAL HARMONIC DISTORTION – The ratio of the sum of the amplitudes of all signals harmonically related to the fundamental, and the amplitude of the fundamental signal.

ZERO SCALE OUTPUT CURRENT – The output current for all bits turned off.

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